EUROPEAN PATENT OFFICE
U.S. PATENT AND TRADEMARK OFFICE

CPC NOTICE OF CHANGES 1928

DATE: AUGUST 1, 2026

PROJECT RP12864

The following classification changes will be effected by this Notice of Changes:

Action	**Subclass**	**Group(s)**
SCHEME:		
Symbols Deleted:	H10W	70/093
Titles Changed:	H10W	70/092
	H10W	72/01212
Warnings New:	H10W	70/095, 70/096, 70/097, 70/098
Warnings Modified:	H10H	29/962
	H10W	70/05, 70/092
	H10W	72/20, 72/90
	H10W	90/00, 90/701
Notes Modified:	H10W	SUBCLASS
DEFINITIONS:		
Definitions New:	H10W	SUBCLASS
	H10W	10/00, 10/20
	H10W	15/00
	H10W	20/00, 20/20, 20/40, 20/42, 20/46, 20/49
	H10W	40/00
	H10W	42/00
	H10W	44/20
	H10W	46/00
	H10W	70/00, 70/60, 70/62, 70/63
	H10W	72/00, 72/20, 72/29, 72/30, 72/50, 72/60, 72/90
	H10W	74/00
	H10W	76/00, 76/42, 76/48
	H10W	78/00
	H10W	80/00
	H10W	90/00
	H10W	95/00

No other subclasses/groups are impacted by this Notice of Changes.

This Notice of Changes includes the following *[Check the ones included]:*

1. CLASSIFICATION SCHEME CHANGES

☒ A. New, Modified or Deleted Group(s)

☒ B. New, Modified or Deleted Warning(s)

- ☒ C. New, Modified or Deleted Note(s)
- ☐ D. New, Modified or Deleted Guidance Heading(s)

2. DEFINITIONS
   - ☒ A. New or Modified Definitions (Full definition template)
   - ☐ B. Modified or Deleted Definitions (Definitions Quick Fix)
3. ☒ REVISION CONCORDANCE LIST (RCL)
4. ☒ CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)
5. ☐ CHANGES TO THE CROSS-REFERENCE LIST (CRL)

CPC NOTICE OF CHANGES 1928

DATE: AUGUST 1, 2026

PROJECT RP12864

1. CLASSIFICATION SCHEME CHANGES

A. New, Modified or Deleted Group(s)

SUBCLASS H10W – GENERIC PACKAGES, INTERCONNECTIONS, CONNECTORS OR OTHER CONSTRUCTIONAL DETAILS OF DEVICES COVERED BY CLASS H10

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	H10W 70/092	3	{Adapting interconnections, e.g. making engineering changes, repairing}	
D	H10W 70/093	3	*{Connecting or disconnecting other interconnections thereto or therefrom, e.g. connecting bond wires or bumps}*	< administrative transfer to H10W 70/099>
M	H10W 72/01212	3	{at a different location than on the final device, e.g. forming solder preforms}	
C	H10W 90/00	0	Package configurations	H10B 80/00, H10D 80/00, H10D 80/20, H10D 80/211, H10D 80/213, H10D 80/215, H10D 80/231, H10D 80/251, H10D 80/30, H10F 39/90, H10F 39/95, H10H 29/20, H10H 29/24, H10H 29/30, H10H 29/32, H10H 29/34, H10H 29/345, H10H 29/352, H10H 29/362, H10H 29/37, H10H 29/39, H10H 29/41, H10H 29/45, H10H 29/49, H10H 29/962, H10K 19/901, H10K 39/601, H10K 39/621, H10K 59/90, H10K 59/95, H10K 65/00, H10N 19/00, H10N 19/101, H10N 39/00, H10N 59/00, H10N 69/00, H10N 79/00, H10N 89/00, H10N 89/02, H10W 90/00, H10W 90/10, H10W 90/15, H10W 90/155, H10W 90/20, H10W 90/22, H10W 90/231, H10W 90/24, H10W 90/26, H10W 90/271, H10W 90/275, H10W90/28, H10W 90/284, H10W 90/288, H10W 90/291, H10W 90/293, H10W 90/295, H10W 90/701, H10W 90/721, H10W 90/722,

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
				H10W 90/723, H10W 90/724, H10W 90/725, H10W 90/726, H10W 90/727, H10W 90/728, H10W 90/729, H10W 90/731, H10W 90/732, H10W 90/733, H10W 90/734, H10W 90/735, H10W 90/736, H10W 90/737, H10W 90/738, H10W 90/739, H10W 90/751, H10W 90/752, H10W 90/753, H10W 90/754, H10W 90/755, H10W 90/756, H10W 90/757, H10W 90/758, H10W 90/759, H10W 90/761, H10W 90/762, H10W 90/763, H10W 90/764, H10W 90/765, H10W 90/766, H10W 90/767, H10W 90/768, H10W 90/769, H10W 90/791, H10W 90/792, H10W 90/794, H10W 90/796, H10W 90/798, H10W 90/811
C	H10W 90/701	1	{characterised by the relative positions of pads or connectors relative to package parts}	H10W 90/701, H10W72/20 - H10W72/709, H10W 72/90 - H10W72/987, H10W 90/724, H10W 90/725, H10W 90/7295, H10W 90/754, H10W 90/755, H10W 90/764, H10W 90/765

*N = new entries where reclassification into entries is involved; C = entries with modified file scope where reclassification of documents from the entries is involved; Q = new entries which are firstly populated with documents via administrative transfers from deleted (D) entries. Afterwards, the transferred documents into the Q entry will either stay or be moved to more appropriate entries, as determined by intellectual reclassification; T= existing entries with enlarged file scope, which receive documents from C or D entries, e.g. when a limiting reference is removed from the entry title; M = entries with no change to the file scope (no reclassification); D = deleted entries; F = frozen entries will be deleted once reclassification of documents from the entries is completed; U = entries that are unchanged.

NOTES:

- **No {curly brackets} are used for titles in CPC only subclasses, e.g. C12Y, A23Y; 2000 series symbol titles of groups found at the end of schemes (orthogonal codes); or the Y section titles. The {curly brackets} are used for 2000 series symbol titles found interspersed throughout the main trunk schemes (breakdown codes).

- U groups: it is obligatory to display the required “anchor” symbol (U group), i.e. the entry immediately preceding a new group or an array of new groups to be created (in case new groups are not clearly subgroups of C-type groups). Always include the symbol, indent level and title of the U group in the table above.
- All entry types should be included in the scheme changes table above for better understanding of the overall scheme change picture. Symbol, indent level, and title are required for all types.
- “Transferred to” column must be completed for all C, D, F, and Q type entries. F groups will be deleted once reclassification is completed.
- When multiple symbols are included in the “Transferred to” column, avoid using ranges of symbols in order to be as precise as possible.
- For administrative transfer of documents, the following text should be used: “< administrative transfer to XX>”, “<administrative transfer to XX and YY simultaneously>”, or “<administrative transfer to XX, YY, ...and ZZ simultaneously>” when administrative transfer of the same documents is to more than one place.
- Administrative transfer to main trunk groups is assumed to be the source allocation type, unless otherwise indicated.
- Administrative transfer to 2000/Y series groups is assumed to be “additional information”.
- If needed, instructions for allocation type should be indicated within the angle brackets using the abbreviations “ADD” or “INV”: <administrative transfer to XX ADD>, <administrative transfer to XX INV>, or < administrative transfer to XX ADD, YY INV, ... and ZZ ADD simultaneously>.
- In certain situations, the “D” entries of 2000-series or Y-series groups may not require a destination (“Transferred to”) symbol, however it is required to specify “<no transfer>” in the “Transferred to” column for such cases.
- For finalisation projects, the deleted “F” symbols should have <no transfer> in the “Transferred to” column.
- For more details about the types of scheme change, see CPC Guide.

B. New, Modified or Deleted Warning(s)

SUBCLASS H10W – GENERIC PACKAGES, INTERCONNECTIONS, CONNECTORS OR OTHER CONSTRUCTIONAL DETAILS OF DEVICES COVERED BY CLASS H10

Type*	Location	Old Warning	New/Modified Warning
M	H10W 70/05	Group H10W 70/05 is incomplete pending reclassification of documents from group H10W 99/00. Group H10W 70/05 is also impacted by reclassification into groups H10W 70/06, H10W 70/08, H10W 70/09, H10W 70/092, H10W 70/093, H10W 70/095, H10W 70/096, H10W 70/097 and H10W 70/098. All groups listed in this Warning should be considered in order to perform a complete search.	Group H10W 70/05 is incomplete pending reclassification of documents from group H10W 99/00. Group H10W 70/05 is also impacted by reclassification into groups H10W 70/06, H10W 70/08, H10W 70/09, H10W 70/092, H10W 70/095, H10W 70/096, H10W 70/097 and H10W 70/098. All groups listed in this Warning should be considered in order to perform a complete search.
M	H10W 70/092	Groups H10W 70/092 - H10W 70/098 are incomplete pending reclassification of documents from group H10W 70/05. Groups H10W 70/05 and H10W 70/092 - H10W 70/098 should be considered in order to perform a complete search.	Group H10W 70/092 is incomplete pending reclassification of documents from group H10W 70/05. Groups H10W 70/05 and H10W 70/092 should be considered in order to perform a complete search.
N	H10W 70/095		Group H10W 70/095 is incomplete pending reclassification of documents from group H10W 70/05. Groups H10W 70/05 and H10W 70/095 should be considered in order to perform a complete search.
N	H10W 70/096		Group H10W 70/096 is incomplete pending reclassification of documents from group H10W 70/05. Groups H10W 70/05 and H10W 70/096 should be considered in order to perform a complete search.
N	H10W 70/097		Group H10W 70/097 is incomplete pending reclassification of documents from group H10W 70/05. Groups H10W 70/05 and H10W 70/097 should be considered in order to perform a complete search.

Type*	Location	Old Warning	New/Modified Warning
N	H10W 70/098		Group H10W 70/098 is incomplete pending reclassification of documents from group H10W 70/05. Groups H10W 70/05 and H10W 70/098 should be considered in order to perform a complete search.
M	H10W 72/20	Group H10W 72/20 is incomplete pending reclassification of documents from group H10W 72/00. Group H10W 72/20 is also impacted by reclassification into groups H10W 72/221, H10W 72/222, H10W 72/223, H10W 72/224, H10W 72/225, H10W 72/227, H10W 72/228, H10W 72/231, H10W 72/232, H10W 72/234, H10W 72/235, H10W 72/237, H10W 72/241, H10W 72/242, H10W 72/244, H10W 72/245, H10W 72/247, H10W 72/248, H10W 72/251, H10W 72/252, H10W 72/253, H10W 72/255, H10W 72/257, H10W 72/2524, H10W 72/2528, H10W 72/261, H10W 72/263, H10W 72/265, H10W 72/267, H10W 72/281, H10W 72/283, H10W 72/285, H10W 72/287, H10W 72/60, H10W 72/621, H10W 72/622, H10W 72/623, H10W 72/624, H10W 72/625, H10W 72/627, H10W 72/631, H10W 72/634, H10W 72/635, H10W 72/637, H10W 72/641, H10W 72/645, H10W 72/647, H10W 72/642, H10W 72/643, H10W 72/646, H10W 72/6478, H10W 72/651, H10W 72/652, H10W 72/653, H10W 72/6528, H10W 72/655, H10W 72/657, H10W 72/681, H10W 72/683, H10W 72/685 and H10W 72/691. All groups listed in this Warning should be considered in order to perform a complete search.	Group H10W 72/20 is incomplete pending reclassification of documents from group H10W 72/00. Groups H10W 72/20 - H10W 72/709 are also incomplete pending reclassification from group H10W 90/701. Group H10W 72/20 is also impacted by reclassification into groups H10W 72/221, H10W 72/222, H10W 72/223, H10W 72/224, H10W 72/225, H10W 72/227, H10W 72/228, H10W 72/231, H10W 72/232, H10W 72/234, H10W 72/235, H10W 72/237, H10W 72/241, H10W 72/242, H10W 72/244, H10W 72/245, H10W 72/247, H10W 72/248, H10W 72/251, H10W 72/252, H10W 72/253, H10W 72/255, H10W 72/257, H10W 72/2524, H10W 72/2528, H10W 72/261, H10W 72/263, H10W 72/265, H10W 72/267, H10W 72/281, H10W 72/283, H10W 72/285, H10W 72/287, H10W 72/60, H10W 72/621, H10W 72/622, H10W 72/623, H10W 72/624, H10W 72/625, H10W 72/627, H10W 72/631, H10W 72/634, H10W 72/635, H10W 72/637, H10W 72/641, H10W 72/645, H10W 72/647, H10W 72/642, H10W 72/643, H10W 72/646, H10W 72/6478, H10W 72/651, H10W 72/652, H10W 72/653, H10W 72/6528, H10W 72/655, H10W 72/657, H10W 72/681, H10W 72/683, H10W 72/685 and H10W 72/691. All groups listed in this Warning should be considered in order to perform a complete search.
M	H10W 72/90	Group H10W 72/90 is impacted by reclassification into groups	Groups H10W 72/90 - H10W 72/987 are incomplete pending

Type*	Location	Old Warning	New/Modified Warning
		H10W 72/921, H10W 72/922, H10W 72/9223, H10W 72/9226, H10W 72/923, H10W 72/9232, H10W 72/924, H10W 72/925, H10W 72/926, H10W 72/927, H10W 72/931, H10W 72/932, H10W 72/934, H10W 72/936, H10W 72/941, H10W 72/9413, H10W 72/9415, H10W 72/942, H10W 72/944, H10W 72/9445, H10W 72/951, H10W 72/952, H10W 72/953, H10W 72/957, H10W 72/9524, H10W 72/9528, H10W 72/961, H10W 72/963, H10W 72/965, H10W 72/967, H10W 72/981, H10W 72/983, H10W 72/985 and H10W 72/987. All groups listed in this Warning should be considered in order to perform a complete search.	reclassification of documents from group H10W 90/701. Group H10W 72/90 is also impacted by reclassification into groups H10W 72/921, H10W 72/922, H10W 72/9223, H10W 72/9226, H10W 72/923, H10W 72/9232, H10W 72/924, H10W 72/925, H10W 72/926, H10W 72/927, H10W 72/931, H10W 72/932, H10W 72/934, H10W 72/936, H10W 72/941, H10W 72/9413, H10W 72/9415, H10W 72/942, H10W 72/944, H10W 72/9445, H10W 72/951, H10W 72/952, H10W 72/953, H10W 72/957, H10W 72/9524, H10W 72/9528, H10W 72/961, H10W 72/963, H10W 72/965, H10W 72/967, H10W 72/981, H10W 72/983, H10W 72/985 and H10W 72/987. All groups listed in this Warning should be considered in order to perform a complete search.
M	H10W 90/00	Group H10W90/00 is impacted by reclassification into groups H10B80/00, H10D80/00, H10D80/20, H10D80/211, H10D80/213, H10D80/215, H10D80/231, H10D80/251, H10D80/30, H10F39/90, H10F39/95, H10H29/20, H10H29/24, H10H29/30, H10H29/32, H10H29/34, H10H29/345, H10H29/352, H10H29/362, H10H29/37, H10H29/39, H10H29/41, H10H29/45, H10H29/49, H10K19/00, H10K19/10, H10K19/20, H10K19/201, H10K19/202, H10K19/80, H10K19/901, H10K39/601, H10K39/621, H10K59/90, H10K59/95, H10K65/00, H10W90/10, H10W90/15, H10W90/155, H10W90/20, H10W90/22, H10W90/231, H10W90/24, H10W90/26, H10W90/271, H10W90/275, H10W90/28, H10W90/284, H10W90/288, H10W90/291,	Group H10W90/00 is impacted by reclassification into groups H10B80/00, H10D80/00, H10D80/20, H10D80/211, H10D80/213, H10D80/215, H10D80/231, H10D80/251, H10D80/30, H10F39/90, H10F39/95, H10H29/20, H10H29/24, H10H29/30, H10H29/32, H10H29/34, H10H29/345, H10H29/352, H10H29/362, H10H29/37, H10H29/39, H10H29/41, H10H29/45, H10H29/49, H10H29/962, H10K19/00, H10K19/10, H10K19/20, H10K19/201, H10K19/202, H10K19/80, H10K19/901, H10K39/601, H10K39/621, H10K59/90, H10K59/95, H10K65/00, H10W90/10, H10W90/15, H10W90/155, H10W90/20, H10W90/22, H10W90/231, H10W90/24, H10W90/26, H10W90/271, H10W90/275, H10W90/28, H10W90/284, H10W90/288,

Type*	Location	Old Warning	New/Modified Warning
		H10W90/293, H10W90/295, H10W90/701, H10W90/721, H10W90/722, H10W90/723, H10W90/724, H10W90/725, H10W90/726, H10W90/727, H10W90/728, H10W90/729, H10W90/731, H10W90/732, H10W90/733, H10W90/734, H10W90/735, H10W90/736, H10W90/737, H10W90/738, H10W90/739, H10W90/751, H10W90/752, H10W90/753, H10W90/754, H10W90/755, H10W90/756, H10W90/757, H10W90/758, H10W90/759, H10W90/761, H10W90/762, H10W90/763, H10W90/764, H10W90/765, H10W90/766, H10W90/767, H10W90/768, H10W90/769, H10W90/791, H10W90/792, H10W90/794, H10W90/796, H10W90/798 and H10W90/811. All groups listed in this Warning should be considered in order to perform a complete search.	H10W90/291, H10W90/293, H10W90/295, H10W90/701, H10W90/721, H10W90/722, H10W90/723, H10W90/724, H10W90/725, H10W90/726, H10W90/727, H10W90/728, H10W90/729, H10W90/731, H10W90/732, H10W90/733, H10W90/734, H10W90/735, H10W90/736, H10W90/737, H10W90/738, H10W90/739, H10W90/751, H10W90/752, H10W90/753, H10W90/754, H10W90/755, H10W90/756, H10W90/757, H10W90/758, H10W90/759, H10W90/761, H10W90/762, H10W90/763, H10W90/764, H10W90/765, H10W90/766, H10W90/767, H10W90/768, H10W90/769, H10W90/791, H10W90/792, H10W90/794, H10W90/796, H10W90/798 and H10W90/811. All groups listed in this Warning should be considered in order to perform a complete search.
M	H10W 90/701	Group H10W 90/701 is incomplete pending reclassification of documents from group H10W 90/00. Group H10W 90/701 is also impacted by reclassification into groups H10W 90/724, H10W 90/725, H10W 90/7295, H10W 90/754, H10W 90/755, H10W 90/764 and H10W 90/765. All groups listed in this Warning should be considered in order to perform a complete search.	Group H10W 90/701 is incomplete pending reclassification of documents from group H10W 90/00. Group H10W 90/701 is also impacted by reclassification into groups H10W 72/20 - H10W 72/709, H10W 72/90 - H10W 72/987, H10W 90/724, H10W 90/725, H10W 90/7295, H10W 90/754, H10W 90/755, H10W 90/764 and H10W 90/765. All groups listed in this Warning should be considered in order to perform a complete search.

SUBCLASS H10H – INORGANIC LIGHT-EMITTING SEMICONDUCTOR DEVICES HAVING POTENTIAL BARRIERS

Type*	Location	Old Warning	New/Modified Warning
M	H10H 29/962	Group H10H29/962 is incomplete pending reclassification of documents from groups H10H29/14 and H10H29/142. Groups H10H29/14, H10H29/142 and H10H29/962 should be considered in order to perform a complete search.	Group H10H29/962 is incomplete pending reclassification of documents from groups H10H29/14, H10H29/142 and H10W90/00. Groups H10H29/14, H10H29/142, H10H29/962 and H10W90/00 should be considered in order to perform a complete search.

*N = new warning, M = modified warning, D = deleted warning

NOTE: The “Location” column only requires the symbol PRIOR to the location of the warning. No further directions such as “before” or “after” are required.

C. New, Modified or Deleted Note(s)

SUBCLASS H10W – GENERIC PACKAGES, INTERCONNECTIONS, CONNECTORS OR OTHER CONSTRUCTIONAL DETAILS OF DEVICES COVERED BY CLASS H10

Type *	Location	Old Note	New/Modified Note
M	H10W	1. This subclass covers: a. packages of devices and parts of such packages; b. interconnections of devices in chips, wafers, substrates or packages; c. connectors of devices in packages; d. other constructional details of devices in chips, wafers, substrates or packages, e.g. isolation regions between components of integrated devices; e. detachable holders for supporting packaged chips in operation; f. the manufacture or treatment of aspects (a)-(e); when aspects (a)-(e) are (1) applicable to devices covered by subclass H10B;(2) applicable to devices covered by subclass H10D, except for semiconductor bodies or electrodes thereof, which are covered by subgroups H10D62/00 or H10D64/00; or(3) generically applicable to devices covered by subclasses H10B, H10D, H10F, H10H, H10K or H10N. 2.{In this subclass, the periodic system used is the I to VIII group system indicated in the Periodic Table under Note (3) of section C.}	1. This subclass covers: a. packages of devices and parts of such packages; b. interconnections of devices in chips, wafers, substrates or packages; c. connectors of devices in packages; d. other constructional details of devices in chips, wafers, substrates or packages, e.g. isolation regions between components of integrated devices; e. detachable holders for supporting packaged chips in operation; f. the manufacture or treatment of aspects (a) - (e); when aspects (a) - (e) are (1) applicable to devices covered by subclass H10B; (2) applicable to devices covered by subclass H10D, except for semiconductor bodies or electrodes thereof, which are covered by subgroups H10D62/00 or H10D64/00; or (3) generically applicable to devices covered by subclasses H10B, H10D, H10F, H10H, H10K or H10N. 2. In this subclass, the periodic system used is the I to VIII group system indicated in the Periodic Table under Note (3) of section C.

*N = new note, M = modified note, D = deleted note

NOTE: The “Location” column only requires the symbol PRIOR to the location of the note. No further directions such as “before” or “after” are required.

2. A. DEFINITIONS (new)

H10W

Definition statement

This place covers:

(a) packages of devices and parts of such packages;

(b) interconnections of devices in chips, wafers, substrates or packages;

(c) connectors of devices in packages;

(d) other constructional details of devices in chips, wafers, substrates or packages, e.g. isolation regions between components of integrated devices; or

(e) detachable holders for supporting packaged chips in operation;

(f) the manufacture or treatment of aspects (a) - (e);

when aspects (a) - (e) are:

(1) applicable to devices covered by subclass H10B;

(2) applicable to devices covered by subclass H10D, except for semiconductor bodies or electrodes thereof, which are covered by groups H10D 62/00 and H10D 64/00; or

(3) generically applicable to devices covered by subclasses H10B, H10D, H10F, H10H, H10K and H10N.

Relationships with other classification places

Constructional details specially adapted for devices that are covered by subclasses H10B, H10D, H10F, H10H, H10K or H10N are classified in the subclasses in question.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Printed circuits; Casings or constructional details of electrical apparatus; Manufacture of assemblages of electrical components	H05K
Constructional details of inorganic semiconductor devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation	H10F 77/00
Constructional details of individual inorganic light-emitting semiconductor devices having potential barriers	H10H 20/80
Constructional details of integrated devices, or assemblies of multiple devices, comprising at least one light-emitting semiconductor element covered by group H10H 20/00	H10H 29/80
Constructional details, e.g. interconnections, of organic electric solid-state devices	H10K 10/80
Interconnections of integrated devices, or assemblies of multiple devices, comprising at least one organic element specially adapted for rectifying, amplifying, oscillating or switching, covered by group H10K 10/00	H10K 19/80
Constructional details of organic devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation	H10K 30/80
Interconnections of devices controlled by radiation	H10K 39/38
Constructional details of organic light-emitting devices	H10K 50/80
Constructional details of integrated devices, or assemblies of multiple devices, comprising at least one organic light-emitting element covered by group H10K 50/00	H10K 59/80
Constructional details of devices covered by H10K and not covered by groups H10K 10/80, H10K 30/80, H10K 50/80 or H10K 59/80	H10K 77/00
Constructional details of thermoelectric devices comprising a junction of dissimilar materials	H10N 10/80
Constructional details of piezoelectric or electrostrictive devices	H10N 30/80
Constructional details of magnetostrictive devices	H10N 35/80

Constructional details of galvanomagnetic devices	H10N 50/80
Constructional details of Hall-effect devices	H10N 52/80
Constructional details of superconducting devices	H10N 60/80
Generic processes or apparatus for the manufacture or treatment of devices covered by class H10	H10P

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

bipolar	refers to semiconductor technology that involves multi-carrier-type operation, i.e. which simultaneously uses both electrons and holes as charge carriers
body	the region of semiconductor (resp. solid-state) material(s) within which, or at the surface of which, the physical effects that are characteristic of the device occur, and any bordering semiconductor (resp. solid-state) material(s) that are contiguous with this region. Examples: in a field-effect transistor [FET], the physical effects occur in the channel region between the source and the drain. The semiconductor body includes the channel region, the source and drain regions, and any contiguous semiconductor material; in a light-emitting diode [LED], the physical effects occur at a junction of active semiconductor layers. The semiconductor body includes these active semiconductor layers and any contiguous semiconductor layers, such as buffer layers, possibly a growth substrate, that are between the cathode and anode electrodes; in a thermoelectric device, the solid-state body includes all solid-state materials in the path of current between the electrodes.
chip	a piece of a wafer or a substrate that has been processed to contain devices therein or thereon. The expression "diced chip" refers to the result of dicing a wafer or a substrate into a plurality

	of chips, whereas "undiced chip" refers to a chip before dicing or with no dicing.
component	an electric circuit element (e.g. diode, transistor, LED) that is one of a plurality of elements formed in or on a common substrate, e.g. in an integrated device
container	a solid construction in which (one or more) devices are placed, or which is formed around the devices, for forming packaged devices. A container requires a partial or total enclosure and it may also comprise a filling.
device	an electric circuit element (e.g. diode, transistor, LED); (depending on the context) can also refer to an integrated device (e.g. CMOS-IC, DRAM device). A device may be in the form of a bare or packaged chip.
dopant	the atoms or compounds added to a material during doping
doping	the intentional addition of a small quantity of atoms or compounds into a material to achieve a desired characteristic, e.g. to produce an n-type or p-type material.
electrode	a conductive region in or on the semiconductor body or solid-state body of a device (and other than the body itself) which exerts an electrical influence on the body, irrespective of whether or not an external electrical connection is made thereto. The term covers metallic regions which exert electrical influence on the body through an insulating region (e.g. in intentional non-parasitic capacitive coupling), or inductive coupling arrangements. In a capacitive coupling arrangement, the dielectric region is regarded as part of the electrode. The overall conductive wiring may comprise multiple portions. In such a case, only the wiring portions that exert an electrical influence on the body are considered portions of the electrode. Examples: conductive layer(s) in direct physical contact with the body; conductive region(s) exerting an inductive

	coupling onto the body; a multilayer structure which exerts influence on the body through an insulating region, e.g. in intentional non-parasitic capacitive coupling.
encapsulation	an enclosure consisting of (one or more) layers, e.g. comprising organic polymers, which at least partially enclose the (one or more) devices, thereby protecting them. An encapsulation is often used to hermetically seal devices.
FET	field-effect transistor
field-effect	refers to semiconductor technology wherein a voltage applied to a gate electrode creates an electric field that allows for control of current near the interface of the gate and the body, e.g. to create an inversion channel between the source and drain of a MOSFET
individual	refers to: an electric circuit element not being an integrated device; or a component of an integrated device. Examples of individual devices include: diodes, transistors, photovoltaic cells, Josephson-junction devices, light-emitting diodes [LED], organic LEDs, or a single LED component within an integrated device.
integrated circuit	an integrated device where all the electric circuit elements (e.g. diodes, transistors, LEDs) are formed in or on a common substrate, including interconnections between the elements
integrated device	a device consisting of a plurality of semiconductor or other solid-state electric circuit elements formed in or on a common substrate
interconnection	a conductive arrangement for conducting electric current from an electrode of a circuit element to another part of the circuit. Examples include metal wirings.
MIS	metal-insulator-semiconductor

MISFET	metal-insulator-semiconductor field-effect transistor
MOS	metal-oxide-semiconductor
package	the collection of all elements, which are external to the chip, that protect the chip or connect it to another object. Package therefore covers encapsulations, containers, package substrates, interposers, heatsinks or the like. Package does not include objects at a higher system level, like circuit boards and beyond, e.g. a housing in which the circuit board is enclosed.
TFT	thin-film transistor
unipolar	refers to semiconductor technology that primarily involves one type only of charge carrier, i.e. it involves either holes or electrons but not both
via	an electrically or thermally conductive connection that passes vertically through a layer. Examples include through-hole vias, blind vias, buried vias, and vias connecting between traces of the back-end-of-line [BEOL] metallisations.
wafer	can be one of the following: (a) a slice of semiconductor or electric solid-state active material. For example: a slice of silicon; a slice of a semiconducting compound, e.g. gallium nitride [GaN]; a slice of lithium tantalate [LiTaO3] for superconductor applications. (b) a multilayered laminate, having at least one layer of semiconductor or electric solid-state active material, the layer being meant to be processed into devices. For example: silicon-on-insulator [SOI]; silicon-on-glass [SOG]; silicon-on-sapphire [SOS]; a composite wafer comprising silicon carbide [SiC] on polycrystalline silicon [Si] support; a layer of semiconducting nanowires on glass. A wafer is typically processed by (e.g.) deposition, etching, doping or diffusion, and is then typically diced into chips.

H10W 10/00

Definition statement

This place covers:

Isolation regions that are in wafers or semiconductor bodies and that are:

- directly between components of integrated devices (e.g. in the same plane as the components); or
- in the electrical path between components of integrated devices (e.g. below the plane of the components).

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Insulating parts of interconnections within wafers or substrates, e.g. through-silicon vias [TSV]	H10W 20/20
Insulating parts of interconnections external to, wafers or substrates	H10W 20/45
Semiconductor bodies of inorganic semiconductor devices having potential barriers	H10D 62/00
Integrated devices comprising inorganic semiconductor devices	H10D 84/00 - H10D 89/00

Special Rules of classification

Buried insulating layers, e.g. buried oxide layers, of semiconductor-on-insulator substrates are covered in group H10W 10/00.

H10W 10/20

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Air gaps in insulating parts of interconnections external to wafers or substrates	H10W 20/46

H10W 15/00

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Highly-doped isolation regions in semiconductor bodies between components of integrated devices	H10W 10/00
Highly-doped interconnections within wafers or substrates	H10W 20/20
Semiconductor bodies, or regions thereof, of inorganic semiconductor devices having potential barriers	H10D 62/00
Integrated devices comprising inorganic semiconductor devices	H10D 84/00 - H10D 89/00
Ion implantation into semiconductor materials of wafers, substrates or parts of devices	H10P 30/20
Diffusion of dopants within, into or out of semiconductor bodies or layers	H10P 32/10

H10W 20/00

Relationships with other classification places

Groups H10W 70/00, H10W 72/00 and H10W 20/00 each cover interconnections, depending on the location of the interconnections.

Group H10W 20/00 covers interconnections that are not in the package. These interconnections are in chips, wafers or substrates other than package substrates. The interconnections may be at least partially surrounded by the semiconductor material of the wafers or by the material of the substrates (in group H10W 20/20), or may be on the wafers or substrates (e.g. in front-end-of-line [FEOL] or back-end-of-line [BEOL] metallisation layers within a chip).

Group H10W 70/00 covers interconnections in packages that are within package substrates, interposers or redistribution layers [RDL].

Group H10W 72/00 covers interconnections in packages that are in parts of the package other than in package substrates, interposers or redistribution layers. For example, bond wires between a chip and a package substrate.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Package substrates; Interposers; Redistribution layers [RDL]	H10W 70/00
Interconnections or connectors in packages other than in package substrates, interposers or redistribution layers	H10W 72/00
Electrically-conductive connections, in general	H01R
Printed circuits	H05K 1/00
Interconnections, e.g. lead-frames, bond wires or solder balls	H10H 20/857
Interconnections of active-matrix LED displays	H10H 29/49
Interconnections of integrated devices, or assemblies of multiple devices, comprising at least one organic element specially adapted for rectifying, amplifying, oscillating or switching, covered by group H10K 10/00	H10K 19/80
Interconnections of devices controlled by radiation	H10K 39/38
Constructional details of interconnections, e.g. terminals	H10K 59/82

Interconnections in thermoelectric devices comprising a junction of dissimilar materials	H10N 10/82
Interconnections in piezoelectric or electrostrictive devices	H10N 30/87
Formation of conductive or resistive materials	H10P 14/40
Etching of wafers, substrates or parts of devices	H10P 50/00

H10W 20/20

Definition statement

This place covers:

Interconnections that provide a current path internal to wafers or substrates.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections in insulating or insulated package substrates, interposers or redistribution layers	H10W 70/62
Vias in insulating or insulated package substrates	H10W 70/63

H10W 20/40

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Redistribution layers outside of chips	H10W 70/60

Special Rules of classification

Contact plugs that directly contact the semiconductor body, and hence are electrodes, may be classified in this group.

H10W 20/42

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections within wafers or substrates, e.g. through-silicon vias	H10W 20/20
Vias in insulating or insulated package substrates	H10W 70/63

H10W 20/46

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Air gaps as isolation regions in semiconductor bodies between components of integrated devices	H10W 10/20

H10W 20/49

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

antifuse	a part of an interconnection that is capable of having its state changed from non-conductive to conductive
fuse	a part of an interconnection that is capable of having its state changed from conductive to non-conductive

H10W 40/00

References

Limiting references

This place does not cover:

Integrated devices comprising arrangements for thermal protection	H10D 89/60

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for protection of devices other than thermal protection	H10W 42/00
Arrangements for thermal protection or thermal control of stacked chips	H10W 90/288
Modifications common to different types of electric apparatus to facilitate cooling, ventilating or heating	H05K 7/20
Arrangements for cooling, heating, ventilating or compensating for temperature fluctuations for inorganic semiconductor devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation	H10F 77/60
Arrangements for heat extraction or cooling for inorganic light-emitting devices	H10H 20/858

Arrangements for heating or cooling of organic light-emitting devices	H10K 50/87

H10W 42/00

References

Limiting references

This place does not cover:

Arrangements for thermal protection	H10W 40/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Encapsulations	H10W 74/00
Containers	H10W 76/00
Arrangements for preventing damage to photovoltaic cells caused by corpuscular radiation	H10F 77/80

H10W 44/20

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Antennas, in general	H01Q
Waveguides, in general	H01P

H10W 46/00

Definition statement

This place covers:

Marks in or on the chips, wafers, substrates or packages of devices.

H10W 70/00

Relationships with other classification places

Groups H10W 70/00, H10W 72/00 and H10W 20/00 each cover interconnections, depending on the location of the interconnections.

Group H10W 20/00 covers interconnections that are not in the package. These interconnections are in chips, wafers or substrates other than package substrates. The interconnections may be at least partially surrounded by the semiconductor material of the wafers or by the material of the substrates (in group H10W 20/20), or may be on the wafers or substrates (e.g. in front-end-of-line [FEOL] or back-end-of-line [BEOL] metallisation layers within a chip).

Group H10W 70/00 covers interconnections in packages that are within package substrates, interposers or redistribution layers [RDL].

Group H10W 72/00 covers interconnections in packages that are in parts of the package other than in package substrates, interposers or redistribution layers. For example, bond wires between a chip and a package substrate.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections in chips, wafers or substrates	H10W 20/00
Interconnections in packages other than in package substrates, interposers or redistribution layers	H10W 72/00
Printed circuits	H05K 1/00
Apparatus or processes for manufacturing printed circuits	H05K 3/00

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

redistribution layer	interconnections in the package, such as metal traces or vias, that laterally reroute ("redistribute") the chip's input/output [I/O] layout into a different, desired I/O pad layout for external connections. Examples include: fan-in RDLs [FI-RDL], i.e. for redistributing I/O signals from a larger chip to a smaller package substrate or interposer; and fan-out RDLs [FO-RDLs], i.e. for redistributing I/O signals from a smaller chip to a larger package substrate or interposer.

Synonyms and Keywords

In patent documents the following abbreviations are often used:

RDL	Redistribution layer

H10W 70/60

References

Limiting references

This place does not cover:

Leadframes	H10W 70/40

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections external to wafers or substrates, e.g. back-end-of-line [BEOL] metallisations or vias connecting to gate electrodes	H10W 20/40
Insulating or insulated package substrates, interposers or redistribution layers between stacked chips	H10W 90/22
Printed circuits	H05K 1/00

H10W 70/62

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Conductive parts of interconnections external to wafers or substrates, e.g. back-end-of-line [BEOL] metallisations or vias connecting to gate electrodes	H10W 20/41
Interconnections in printed circuit board	H05K 1/00

H10W 70/63

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections within wafers or substrates, e.g. through-silicon vias	H10W 20/20

Vias external to wafers or substrates, e.g. back-end-of-line [BEOL] metallisations or vias connecting to gate electrodes	H10W 20/42

H10W 72/00

Definition statement

This place covers:

Interconnections or connectors in parts of packages other than in package substrates, interposers or redistribution layers. For example, between a chip and a package substrate, or in an encapsulation.

Relationships with other classification places

Groups H10W 70/00, H10W 72/00 and H10W 20/00 each cover interconnections, depending on the location of the interconnections.

Group H10W 20/00 covers interconnections that are not in the package. These interconnections are in chips, wafers or substrates other than package substrates. The interconnections may be at least partially surrounded by the semiconductor material of the wafers or by the material of the substrates (in group H10W 20/20), or may be on the wafers or substrates (e.g. in front-end-of-line [FEOL] or back-end-of-line [BEOL] metallisation layers within a chip).

Group H10W 70/00 covers interconnections in packages that are within package substrates, interposers or redistribution layers [RDL].

Group H10W 72/00 covers interconnections in packages that are in parts of the package other than in package substrates, interposers or redistribution layers. For example, bond wires between a chip and a package substrate.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections in chips, wafers or substrates	H10W 20/00
Interconnections in insulated package substrates, interposers or redistribution layers [RDL]	H10W 70/62
Electrically-conductive connections, in general	H01R

Special Rules of classification

If a connector is directly on an electrode or interconnection, without an intervening bond pad, so that the electrode or interconnection acts as a bond pad, the electrode or interconnection may be classified in groups for bond pads.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

connector	an element within a package for electrically or physically connecting chips or package parts to other chips, package parts or a circuit board (e.g. to a printed circuit board [PCB])

H10W 72/20

Definition statement

This place covers:

Bump connectors, dummy bumps or thermal bumps in packages. For example, a bump between a chip and a package substrate; or a bump on the surface of a package substrate opposite to a mounted chip.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of bump connectors	H10W 72/012
Connecting or disconnecting of bump connectors	H10W 72/072
Underfills	H10W 74/15
Positions of bump connectors relative to package parts	H10W 90/721

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

bump connector	a bump that provides electrical connection. Examples include solder balls or copper pillars. An electrically-conductive connector on the electrodes or bond pads of a chip or package part, for electrical connection between objects. Examples include solder balls or copper pillars.
dummy bump	a bump having similar properties to a bump connector (such as shape or material), for purposes other than electrical connection, such as mechanical connection
thermal bump	a bump having similar properties to a bump connector (such as shape or material), for purposes other than electrical connection, such as for thermal connection between objects

Synonyms and Keywords

In patent documents, the following words/expressions are often used as synonyms:

"solder bump", "bump" and "solder ball"

H10W 72/29

Definition statement

This place covers:

Pads or under-bump metallurgy [UBM] for bump connectors.

H10W 72/30

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of die-attach connectors	H10W 72/013
Connecting or disconnecting of die-attach connectors	H10W 72/073
Underfills	H10W 74/15
Positions of die-attach connectors relative to package parts	H10W 90/731

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

die-attach connector	a connector for bonding or mounting of a chip, primarily intended for mechanical connection. Examples include: (a) an insulating adhesive to connect the inactive surface of a chip to a package substrate; (b) a conductive solder or sintered layer to connect the inactive side of a chip to a leadframe.

H10W 72/50

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of bond wires	H10W 72/015
Connecting or disconnecting of bond wires	H10W 72/075
Positions of bond wires relative to package parts	H10W 90/751

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

bond wire	a conducting connector in the form of typically a flexible thread that is intended to be connected to an object by wirebonding methods, e.g. by thermocompression, ultrasonic or thermosonic methods

H10W 72/60

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of strap connectors	H10W 72/016
Connecting or disconnecting of strap connectors	H10W 72/076
Positions of strap connectors relative to package parts	H10W 90/761

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

strap connector	a conductive connector, often having a width that is of the scale of a chip's width, that is typically used for high-power applications

H10W 72/90

Definition statement

This place covers:

Bond pads in general, i.e. where the nature of a related connector is unspecified or generic to multiple types of connectors.

Relationships with other classification places

Bond pads specially adapted for a specific type of connector are classified in a group covering the connector type. For example, bond pads specially adapted for wire connectors are classified in group H10W 72/59 and bond pads specially adapted for strap connectors are classified in group H10W 72/60.

References

Application-oriented references

Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Bond pads specially adapted for bump connectors	H10W 72/29
Bond pads specially adapted for conductive adhesives	H10W 72/49
Bond pads specially adapted for bond wires	H10W 72/59
Bond pads specially adapted for strap connectors	H10W 72/60

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of bond pads	H10W 72/019
Direct bonding of bond pads	H10W 80/00
Positions of direct-bonded bond pads relative to package parts	H10W 90/791

H10W 74/00

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Die-attach connectors	H10W 72/30
Encapsulations or containers for stacked chips	H10W 90/291
Encapsulations or containers for integrated devices, or assemblies of multiple devices, having inorganic photovoltaic cells	H10F 19/80
Coatings for inorganic semiconductor devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation	H10F 77/30
Encapsulations or containers for inorganic semiconductor devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation	H10F 77/50
Coatings for inorganic light-emitting devices	H10H 20/84

Encapsulations for inorganic light-emitting devices	H10H 20/852
Encapsulations for integrated devices, or assemblies of multiple devices, comprising at least one inorganic light-emitting device	H10H 29/852
Passivation, containers or encapsulations for organic devices specially adapted for rectifying, amplifying, oscillating or switching	H10K 10/88
Passivation, containers or encapsulations for organic devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation	H10K 30/88
Passivation, containers or encapsulations for organic light-emitting devices	H10K 50/84

H10W 76/00

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Detachable holders for supporting packaged chips in operation	H10W 78/00
Encapsulations or containers for stacked chips	H10W 90/291
Casings, cabinets or drawers for electric apparatus	H05K 5/00
Encapsulations or containers for integrated devices, or assemblies of multiple devices, having photovoltaic cells	H10F 19/80
Containers or encapsulations of image sensors	H10F 39/804
Encapsulations or containers light-receiving devices	H10F 77/50

Packages for light-emitting devices	H10H 20/85
Containers for light-emitting devices	H10H 20/8506

H10W 76/42

Definition statement

This place covers:

Materials formed in containers before or after mounting chips in the container.

Special Rules of classification

In this group, the phase of the fillings is determined at the operating temperature of the device.

H10W 76/48

Definition statement

This place covers:

Gettering materials formed in containers or matrix materials having gettering materials as components therein, which are formed in containers.

Special Rules of classification

In this group, the phase of the fillings is determined at the operating temperature of the device.

H10W 78/00

Relationships with other classification places

Group H10W 78/00 covers the aspect of a holder being detachable, while other groups cover the holders.

For example, package substrates, containers or heat sinks that are detachable may be classified both in group H10W 78/00 and in the groups covering package substrates, containers or heat sinks.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Securing means for detachable heating or cooling arrangements, e.g. clamps	H10W 40/60
Package substrates; Interposers; Redistribution layers [RDL]	H10W 70/00
Printed circuits	H05K 1/00

H10W 80/00

Definition statement

This place covers:

Direct bonding of:

- chips, e.g. chip-to-chip;
- wafers having devices and interconnections therein or thereon, e.g. wafer-to-wafer;
- substrates having devices and interconnections therein or thereon; or
- combinations thereof, e.g. chip-to-wafer.

Relationships with other classification places

Bonding of wafers or substrates either (i) before the step of making of any interconnections or (ii) before the step of packaging of devices, whichever step comes first, is covered in H10P 10/00. Aspects of bonding involving chips, wafers or substrates, which already have interconnections therein/thereon, are covered in group H10W 80/00.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections external to wafers or substrates, e.g. back-end-of-line [BEOL] metallisations	H10W 20/40
Bond pads, in general	H10W 72/90
Positions of direct-bonded bond pads relative to package parts	H10W 90/791

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

direct bonding	bonding of two objects without the use of intervening bonding material (e.g. without solder or adhesive). Examples include: (a) direct pad-to-pad bonding; (b) direct insulator-to-insulator bonding; and (c) hybrid bonding, namely the combination of (a) and (b) above.

H10W 90/00

Definition statement

This place covers:

The relative positions of multiple chips within a single package, e.g. adjacent chips in a single encapsulation.

The relative positions of multiple chips within multiple packages, e.g. one encapsulated chip on another encapsulated chip in a "package-on-package" configuration.

Relationships with other classification places

1. Package parts per se are covered by other groups of this subclass, e.g. encapsulations are covered by H10W 74/00.

2. The types of devices in the assembly of devices are captured in groups of subclasses H10B, H10D, H10F, H10H, H10K or H10N; whereas the configuration of chips in the packages is covered in H10W 90/00 if they meet any of the following conditions:

(1) they are for devices covered by subclasses H10B or H10D; or

(2) they are generically applicable to devices covered by H10B, H10D, H10F, H10H, H10K or H10N.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Assemblies of multiple devices comprising at least one memory device covered by subclass H10B	H10B 80/00
Assemblies of multiple devices comprising at least one device covered by subclass H10D	H10D 80/00
Assemblies of multiple devices comprising at least one photovoltaic cell covered by group H10F 10/00	H10F 19/00
Assemblies of multiple devices comprising at least one element covered by group H10F 30/00, e.g. comprising a photodiode	H10F 39/00
Assemblies of multiple devices comprising at least one light-emitting device covered by group H10H 20/00	H10H 29/20
Assemblies of multiple devices comprising at least one organic radiation-sensitive element covered by group H10K 30/00	H10K 39/00
Assemblies of multiple devices comprising at least one organic light-emitting element covered by group H10K 50/00	H10K 59/00

Assemblies of multiple devices comprising at least one thermoelectric or thermomagnetic element covered by groups H10N 10/00 - H10N 15/00	H10N 19/00
Assemblies of multiple devices comprising at least one piezoelectric, electrostrictive or magnetostrictive element covered by groups H10N 30/00 - H10N 35/00	H10N 39/00
Assemblies of multiple devices comprising at least one galvanomagnetic or Hall-effect element covered by groups H10N 50/00 - H10N 52/00	H10N 59/00
Assemblies of multiple devices comprising at least one superconducting element covered by group H10N 60/00	H10N 69/00
Assemblies of multiple devices comprising at least one solid-state element covered by group H10N 70/00	H10N 79/00
Assemblies of multiple devices comprising at least one bulk negative-resistance effect element covered by group H10N 80/00	H10N 89/00

H10W 95/00

Special Rules of classification

The manufacture or treatment of elements covered by subclass of H10W where provision for the process exists in this subclass are covered by the groups that provide for it. For example, the manufacture or treatment of an encapsulation is covered by group H10W 74/01.

The manufacture or treatment of elements covered by this subclass that would be classified together with the part because no provision for the process exists in this subclass are covered by the group related to the part. For example, the manufacture or treatment of a bump connector should be classified in group H10W 72/20.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

packaging	manufacture or treatment of a package or its parts

3. REVISION CONCORDANCE LIST (RCL)

Type*	**From CPC Symbol (existing)**	**To CPC Symbol(s)**
D	H10W 70/093	< administrative transfer to H10W 70/099>
C	H10W 90/00	H10B 80/00, H10D 80/00, H10D 80/20, H10D 80/211, H10D 80/213, H10D 80/215, H10D 80/231, H10D 80/251, H10D 80/30, H10F 39/90, H10F 39/95, H10H 29/20, H10H 29/24, H10H 29/30, H10H 29/32, H10H 29/34, H10H 29/345, H10H 29/352, H10H 29/362, H10H 29/37, H10H 29/39, H10H 29/41, H10H 29/45, H10H 29/49, H10H 29/962, H10K 19/901, H10K 39/601, H10K 39/621, H10K 59/90, H10K 59/95, H10K 65/00, H10N 19/00, H10N 19/101, H10N 39/00, H10N 59/00, H10N 69/00, H10N 79/00, H10N 89/00, H10N 89/02, H10W 90/00, H10W 90/10, H10W 90/15, H10W 90/155, H10W 90/20, H10W 90/22, H10W 90/231, H10W 90/24, H10W 90/26, H10W 90/271, H10W 90/275, H10W 90/28, H10W 90/284, H10W 90/288, H10W 90/291, H10W 90/293, H10W 90/295, H10W 90/701, H10W 90/721, H10W 90/722, H10W 90/723, H10W 90/724, H10W 90/725, H10W 90/726, H10W 90/727, H10W 90/728, H10W 90/729, H10W 90/731, H10W 90/732, H10W 90/733, H10W 90/734, H10W 90/735, H10W 90/736, H10W 90/737, H10W 90/738, H10W 90/739, H10W 90/751, H10W 90/752, H10W 90/753, H10W 90/754, H10W 90/755, H10W 90/756, H10W 90/757, H10W 90/758, H10W 90/759, H10W 90/761, H10W 90/762, H10W 90/763, H10W 90/764, H10W 90/765, H10W 90/766, H10W 90/767, H10W 90/768, H10W 90/769, H10W 90/791, H10W 90/792, H10W 90/794, H10W 90/796, H10W 90/798, H10W 90/811

C	H10W 90/701	H10W90/701, H10W72/20, H10W72/221, H10W72/222, H10W72/223, H10W72/224, H10W72/225, H10W72/227, H10W72/228, H10W72/231, H10W72/232, H10W72/234, H10W72/235, H10W72/237, H10W72/241, H10W72/242, H10W72/244, H10W72/245, H10W72/247, H10W72/248, H10W72/251, H10W72/252, H10W72/2524, H10W72/2528, H10W72/253, H10W72/255, H10W72/257, H10W72/261, H10W72/263, H10W72/265, H10W72/267, H10W72/281, H10W72/283, H10W72/285, H10W72/287, H10W72/29, H10W72/30, H10W72/321, H10W72/322, H10W72/323, H10W72/324, H10W72/325, H10W72/327, H10W72/328, H10W72/331, H10W72/332, H10W72/334, H10W72/335, H10W72/337, H10W72/341, H10W72/342, H10W72/344, H10W72/345, H10W72/347, H10W72/348, H10W72/351, H10W72/352, H10W72/3524, H10W72/3528, H10W72/353, H10W72/354, H10W72/355, H10W72/357, H10W72/361, H10W72/365, H10W72/367, H10W72/381, H10W72/383, H10W72/385, H10W72/387, H10W72/40, H10W72/49, H10W72/50, H10W72/521, H10W72/522, H10W72/523, H10W72/524, H10W72/525, H10W72/527, H10W72/528, H10W72/531, H10W72/533, H10W72/534, H10W72/535, H10W72/536, H10W72/5363, H10W72/5366, H10W72/5368, H10W72/537, H10W72/541, H10W72/543, H10W72/5434, H10W72/5438, H10W72/5445, H10W72/5449, H10W72/5453, H10W72/547, H10W72/5473, H10W72/5475, H10W72/551, H10W72/552, H10W72/5522, H10W72/5524, H10W72/5525, H10W72/5527, H10W72/5528,

Type*	**From CPC Symbol (existing)**	**To CPC Symbol(s)**
		H10W72/553, H10W72/555, H10W72/557, H10W72/581, H10W72/583, H10W72/585, H10W72/59, H10W72/60, H10W72/621, H10W72/622, H10W72/623, H10W72/624, H10W72/625, H10W72/627, H10W72/631, H10W72/634, H10W72/635, H10W72/637, H10W72/641, H10W72/642, H10W72/643, H10W72/644, H10W72/645, H10W72/646, H10W72/647, H10W72/6478, H10W72/651, H10W72/652, H10W72/6524, H10W72/6528, H10W72/653, H10W72/655, H10W72/657, H10W72/681, H10W72/683, H10W72/685, H10W72/691, H10W72/701, H10W72/709, H10W72/90, H10W72/921, H10W72/922, H10W72/9223, H10W72/9226, H10W72/923, H10W72/9232, H10W72/924, H10W72/925, H10W72/926, H10W72/927, H10W72/931, H10W72/932, H10W72/934, H10W72/936, H10W72/941, H10W72/9413, H10W72/9415, H10W72/942, H10W72/944, H10W72/9445, H10W72/951, H10W72/952, H10W72/9524, H10W72/9528, H10W72/953, H10W72/957, H10W72/961, H10W72/963, H10W72/965, H10W72/967, H10W72/981, H10W72/983, H10W72/985, H10W72/987, H10W90/724, H10W90/725, H10W90/7295, H10W90/754, H10W90/755, H10W90/764, H10W90/765

* C = entries with modified file scope where reclassification of documents from the entries is involved; Q = new entries which are firstly populated with documents via administrative transfers from deleted (D) entries. Afterwards, the transferred documents into the Q entry will either stay or be moved to more appropriate entries, as determined by intellectual reclassification; D = deleted entries; F = frozen entries will be deleted once reclassification of documents from the entries is completed.

NOTES:

- Only C, D, F, and Q type entries are included in the table above.
- When multiple symbols are included in the “To” column, do not use ranges of symbols.

- For administrative transfer of documents, the following text should be used: "< administrative transfer to XX>", "<administrative transfer to XX and YY simultaneously>", or "<administrative transfer to XX, YY, ...and ZZ simultaneously>" when administrative transfer of the same documents is to more than one place.
- Administrative transfer to main trunk groups is assumed to be the source allocation type, unless otherwise indicated.
- Administrative transfer to 2000/Y series groups is assumed to be "additional information".
- If needed, instructions for allocation type should be indicated within the angle brackets using the abbreviations "ADD" or "INV": <administrative transfer to XX ADD>, <administrative transfer to XX INV>, or < administrative transfer to XX ADD, YY INV, ... and ZZ ADD simultaneously>.
- In certain situations, the "D" entries of 2000-series or Y-series groups may not require a destination ("To") symbol, however it is required to specify "<no transfer>" in the "To" column for such cases.
- RCL is not needed for finalisation projects.

4. CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)

CPC	**IPC**	**Action***
H10W 70/093		DELETE

*Action column:

- For an (N) or (Q) entry, provide an IPC symbol and complete the Action column with “NEW.”
- For an existing CPC main trunk entry or indexing entry where the existing IPC symbol needs to be changed, provide an updated IPC symbol and complete the Action column with “UPDATED.”
- For a (D) CPC entry or indexing entry complete the Action column with “DELETE.” IPC symbol does not need to be included in the IPC column.
- For an (N) 2000 series CPC entry which is positioned within the main trunk scheme (breakdown code) provide an IPC symbol and complete the action column with “NEW”.
- For an (N) 2000 series CPC entry positioned at the end of the CPC scheme (orthogonal code), with no IPC equivalent, complete the IPC column with “CPCONLY” and complete the action column with “NEW”.

NOTES:

- F symbols are <u>not</u> included in the CICL table above.
- T and M symbols are not included in the CICL table above unless a change to the existing IPC is desired.