EUROPEAN PATENT OFFICE
U.S. PATENT AND TRADEMARK OFFICE

CPC NOTICE OF CHANGES 1782

DATE: AUGUST 1, 2025

PROJECT MP12697

The following classification changes will be effected by this Notice of Changes:

Action	**Subclass**	**Group(s)**
SCHEME:		
Titles Changed:	H01L	25/03
DEFINITIONS:		
Definitions Modified:	H10B	SUBCLASS
	H10K	SUBCLASS
	H10N	SUBCLASS

No other subclasses/groups are impacted by this Notice of Changes.

This Notice of Changes includes the following *[Check the ones included]:*

1. CLASSIFICATION SCHEME CHANGES
   - ☒ A. New, Modified or Deleted Group(s)
   - ☐ B. New, Modified or Deleted Warning(s)
   - ☐ C. New, Modified or Deleted Note(s)
   - ☐ D. New, Modified or Deleted Guidance Heading(s)
2. DEFINITIONS
   - ☒ A. New or Modified Definitions (Full definition template)
   - ☐ B. Modified or Deleted Definitions (Definitions Quick Fix)
3. ☐ REVISION CONCORDANCE LIST (RCL)
4. ☐ CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)
5. ☐ CHANGES TO THE CROSS-REFERENCE LIST (CRL)

CPC NOTICE OF CHANGES 1782

DATE: AUGUST 1, 2025

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1. CLASSIFICATION SCHEME CHANGES

A. New, Modified or Deleted Group(s)

SUBCLASS H01L – SEMICONDUCTOR DEVICES NOT COVERED BY CLASS H10

Type*	Symbol	Indent Level Number of dots (e.g. 0, 1, 2)	Title "CPC only" text should normally be enclosed in {curly brackets}**	Transferred to#
M	H01L 25/03	1	all the devices being of a type provided for in a single subclass of subclasses H10B, H10D, H10F, H10H, H10K or H10N, e.g. assemblies of rectifier diodes	

*N = new entries where reclassification into entries is involved; C = entries with modified file scope where reclassification of documents from the entries is involved; Q = new entries which are firstly populated with documents via administrative transfers from deleted (D) entries. Afterwards, the transferred documents into the Q entry will either stay or be moved to more appropriate entries, as determined by intellectual reclassification; T= existing entries with enlarged file scope, which receive documents from C or D entries, e.g. when a limiting reference is removed from the entry title; M = entries with no change to the file scope (no reclassification); D = deleted entries; F = frozen entries will be deleted once reclassification of documents from the entries is completed; U = entries that are unchanged.

NOTES:

- **No {curly brackets} are used for titles in CPC only subclasses, e.g. C12Y, A23Y; 2000 series symbol titles of groups found at the end of schemes (orthogonal codes); or the Y section titles. The {curly brackets} are used for 2000 series symbol titles found interspersed throughout the main trunk schemes (breakdown codes).
- U groups: it is obligatory to display the required "anchor" symbol (U group), i.e. the entry immediately preceding a new group or an array of new groups to be created (in case new groups are not clearly subgroups of C-type groups).Always include the symbol, indent level and title of the U group in the table above.
- All entry types should be included in the scheme changes table above for better understanding of the overall scheme change picture. Symbol, indent level, and title are required for all types .
- "Transferred to" column must be completed for all C, D, F, and Q type entries. F groups will be deleted once reclassification is completed.
- When multiple symbols are included in the "Transferred to" column, avoid using ranges of symbols in order to be as precise as possible.
- For administrative transfer of documents, the following text should be used: "< administrative transfer to XX>", "<administrative transfer to XX and YY simultaneously>", or "<administrative transfer to XX, YY, ...and ZZ simultaneously>" when administrative transfer of the same documents is to more than one place.
- Administrative transfer to main trunk groups is assumed to be the source allocation type, unless otherwise indicated.
- Administrative transfer to 2000/Y series groups is assumed to be "additional information".
- If needed, instructions for allocation type should be indicated within the angle brackets using the abbreviations "ADD" or "INV": <administrative transfer to XX ADD> , <administrative transfer to XX INV>, or < administrative transfer to XX ADD, YY INV, ... and ZZ ADD simultaneously>.
- In certain situations, the "D" entries of 2000-series or Y-series groups may not require a destination ("Transferred to") symbol, however it is required to specify "<no transfer>" in the "Transferred to" column for such cases.
- For finalisation projects, the deleted "F" symbols should have <no transfer> in the "Transferred to" column.
- For more details about the types of scheme change, see CPC Guide.

2. A. DEFINITIONS (modified)

H10B

References

Glossary of terms

Replace: The Glossary of terms table with the revised table below.

In this place, the following terms or expressions are used with the meaning indicated:

chip	a piece of a wafer or a substrate that has been processed to contain devices therein or thereon. The expression "diced chip" refers to the result of dicing a wafer or a substrate into a plurality of chips, whereas "undiced chip" refers to a chip before dicing or with no dicing.
device	an electric circuit element (e.g. diode, transistor, LED, etc.); (depending on the context) can also refer to an integrated device (e.g. CMOS-IC, DRAM device, etc.). A device may be in the form of a bare or packaged chip.
dopant	the atoms or compounds added to a material during doping
doping	the intentional addition of a small quantity of atoms or compounds into a material to achieve a desired characteristic, e.g. to produce an n-type or p-type material
individual	refers to: an electric circuit element not being an integrated device; or a component of an integrated device. Examples of individual devices include: diodes, transistors, photovoltaic cells, Josephson-junction devices, light-emitting diodes [LED], organic LEDs or a single LED component within an integrated device.
integrated device	a device consisting of a plurality of semiconductor or other solid-state electric circuit elements formed in or on a common substrate
integrated circuit	an integrated device where all the electric circuit elements (e.g. diodes, transistors, LEDs, etc.) are

	formed in or on a common substrate, including interconnections between the elements
component	an electric circuit element (e.g. diode, transistor, LED, etc.) that is one of a plurality of elements formed in or on a common substrate, e.g. in an integrated device
wafer	it can be one of the following: (a) a slice of semiconductor or electric solid-state active material. For example: a slice of silicon; a slice of a semiconducting compound, e.g. gallium nitride [GaN]; a slice of lithium tantalate [$LiTaO_3$] for superconductor applications. (b) A multilayered laminate, having at least one layer of semiconductor or electric solid-state active material, the layer being meant to be processed into devices. For example: silicon-on-insulator [SOI]; silicon-on-glass [SOG]; silicon-on-sapphire [SOS]; a composite wafer comprising silicon carbide [SiC] on polycrystalline silicon [Si] support; a layer of semiconducting nanowires on glass. A wafer is typically processed by (e.g.) deposition, etching, doping or diffusion, and is then typically diced into chips.
body	the region of semiconductor (resp. solid-state) material(s) within which, or at the surface of which, the physical effects that are characteristic of the device occur, and any bordering semiconductor (resp. solid-state) material(s) that are contiguous with this region. Examples: in a field-effect transistor [FET], the physical effects occur in the channel region between the source and the drain. The semiconductor body includes the channel region, the source and drain regions, and any contiguous semiconductor material; in a light-emitting diode [LED], the physical effects occur at a junction of active semiconductor layers. The semiconductor body includes these active semiconductor layers and any contiguous semiconductor layers, such as buffer layers, possibly a growth substrate, etc., that are between the cathode and anode electrodes; in a thermoelectric device, the solid-state body includes all solid-state materials in the path of current between the electrodes.

electrode	a conductive region in or on the semiconductor body or solid-state body of a device (and other than the body itself) which exerts an electrical influence on the body, irrespective of whether or not an external electrical connection is made thereto. The term covers metallic regions which exert electrical influence on the body through an insulating region (e.g. in intentional non-parasitic capacitive coupling), or inductive coupling arrangements. In a capacitive coupling arrangement, the dielectric region is regarded as part of the electrode. The overall conductive wiring may comprise multiple portions. In such a case, only the wiring portions that exert an electrical influence on the body are considered portions of the electrode. Examples: conductive layer(s) in direct physical contact with the body; conductive region(s) exerting an inductive coupling onto the body; a multilayer structure which exerts influence on the body through an insulating region, e.g. in intentional non-parasitic capacitive coupling.
interconnection	a conductive arrangement for conducting electric current from an electrode of a circuit element to another part of the circuit. Examples include metal wirings.
container	a solid construction in which (one or more) devices are placed, or which is formed around the devices, for forming packaged devices. A container requires a partial or total enclosure and it may also comprise a filling.
encapsulation	an enclosure consisting of (one or more) layers, e.g. comprising organic polymers, which at least partially enclose the (one or more) devices, thereby protecting them. An encapsulation is often used to hermetically seal devices.
field-effect	refers to semiconductor technology wherein a voltage applied to a gate electrode creates an electric field that allows for control of current near the interface of the gate and the body, e.g. to create an inversion channel between the source and drain of a MOSFET
package	the collection of all elements, which are external to the chip, that protect the chip or connect it to another object. Package therefore covers

	encapsulations, containers, package substrates, interposers, heatsinks or the like. Package does not include objects at a higher system level, like circuit boards and beyond, e.g. a housing in which the circuit board is enclosed.
unipolar	refers to semiconductor technology that primarily involves one type only of charge carrier, i.e. it involves either holes or electrons but not both
bipolar	refers to semiconductor technology that involves multi-carrier-type operation, i.e. which simultaneously uses both electrons and holes as charge carriers
MIS	metal-insulator-semiconductor
MOS	metal-oxide-semiconductor
FET	field-effect transistor
MISFET	metal-insulator-semiconductor field-effect transistor
TFT	thin-film transistor
programming	setting a desired state of a memory cell
writing, erasing	changing the state of a memory cell, in a memory cell wherein programming can occur as many times as desired
core, core region	the portion of a memory cell having storage components, select components, or data lines such as bit lines and word lines. The core also includes devices for local accessing (e.g. reading, writing or erasing) of the storage elements, for example, select transistors of NAND strings or read/write ports of SRAM.
peripheral region, periphery	the portion of a memory device outside the core region having devices or parts for global accessing (e.g. reading, writing, erasing) of the devices of the core region. It includes, e.g. word line drivers, multiplexers or sense amplifiers.
boundary region between the core region and peripheral circuit region	the portion of a memory device that contains neither core devices (e.g. storage components or select components) nor peripheral devices (e.g. word line drivers or multiplexers), typically comprising structural parts such as bit line fan-outs between the core region and the peripheral region, or dummy elements or staircase structures for 3D NAND

H10K

References

Glossary of terms

Replace: The Glossary of terms table with the revised table below.

In this place, the following terms or expressions are used with the meaning indicated:

chip	a piece of a wafer or a substrate that has been processed to contain devices therein or thereon. The expression "diced chip" refers to the result of dicing a wafer or a substrate into a plurality of chips, whereas "undiced chip" refers to a chip before dicing or with no dicing.
device	an electric circuit element (e.g. diode, transistor, LED, etc.); (depending on the context) can also refer to an integrated device (e.g. CMOS-IC, DRAM device, etc.). A device may be in the form of a bare or packaged chip.
dopant	the atoms or compounds added to a material during doping
doping	the intentional addition of a small quantity of atoms or compounds into a material to achieve a desired characteristic, e.g. to produce an n-type or p-type material
individual	refers to: an electric circuit element not being an integrated device; or a component of an integrated device. Examples of individual devices include: diodes, transistors, photovoltaic cells, Josephson-junction devices, light-emitting diodes [LED], organic LEDs or a single LED component within an integrated device.
integrated device	a device consisting of a plurality of semiconductor or other solid-state electric circuit elements formed in or on a common substrate
integrated circuit	an integrated device where all the electric circuit elements (e.g. diodes, transistors, LEDs, etc.) are

	formed in or on a common substrate, including interconnections between the elements
component	an electric circuit element (e.g. diode, transistor, LED, etc.) that is one of a plurality of elements formed in or on a common substrate, e.g. in an integrated device
wafer	it can be one of the following: (a) a slice of semiconductor or electric solid-state active material. For example: a slice of silicon; a slice of a semiconducting compound, e.g. gallium nitride [GaN]; a slice of lithium tantalate [$LiTaO_3$] for superconductor applications. (b) A multilayered laminate, having at least one layer of semiconductor or electric solid-state active material, the layer being meant to be processed into devices. For example: silicon-on-insulator [SOI]; silicon-on-glass [SOG]; silicon-on-sapphire [SOS]; a composite wafer comprising silicon carbide [SiC] on polycrystalline silicon [Si] support; a layer of semiconducting nanowires on glass. A wafer is typically processed by (e.g.) deposition, etching, doping or diffusion, and is then typically diced into chips.
body	the region of semiconductor (resp. solid-state) material(s) within which, or at the surface of which, the physical effects that are characteristic of the device occur, and any bordering semiconductor (resp. solid-state) material(s) that are contiguous with this region. Examples: in a field-effect transistor [FET], the physical effects occur in the channel region between the source and the drain. The semiconductor body includes the channel region, the source and drain regions, and any contiguous semiconductor material; in a light-emitting diode [LED], the physical effects occur at a junction of active semiconductor layers. The semiconductor body includes these active semiconductor layers and any contiguous semiconductor layers, such as buffer layers, possibly a growth substrate, etc., that are between the cathode and anode electrodes; in a thermoelectric device, the solid-state body includes all solid-state materials in the path of current between the electrodes.

electrode	a conductive region in or on the semiconductor body or solid-state body of a device (and other than the body itself) which exerts an electrical influence on the body, irrespective of whether or not an external electrical connection is made thereto. The term covers metallic regions which exert electrical influence on the body through an insulating region (e.g. in intentional non-parasitic capacitive coupling), or inductive coupling arrangements. In a capacitive coupling arrangement, the dielectric region is regarded as part of the electrode. The overall conductive wiring may comprise multiple portions. In such a case, only the wiring portions that exert an electrical influence on the body are considered portions of the electrode. Examples: conductive layer(s) in direct physical contact with the body; conductive region(s) exerting an inductive coupling onto the body; a multilayer structure which exerts influence on the body through an insulating region, e.g. in intentional non-parasitic capacitive coupling.
interconnection	a conductive arrangement for conducting electric current from an electrode of a circuit element to another part of the circuit. Examples include metal wirings.
container	a solid construction in which (one or more) devices are placed, or which is formed around the devices, for forming packaged devices. A container requires a partial or total enclosure and it may also comprise a filling.
encapsulation	an enclosure consisting of (one or more) layers, e.g. comprising organic polymers, which at least partially enclose the (one or more) devices, thereby protecting them. An encapsulation is often used to hermetically seal devices.
field-effect	refers to semiconductor technology wherein a voltage applied to a gate electrode creates an electric field that allows for control of current near the interface of the gate and the body, e.g. to create an inversion channel between the source and drain of a MOSFET
package	the collection of all elements, which are external to the chip, that protect the chip or connect it to another object. Package therefore covers

	encapsulations, containers, package substrates, interposers, heatsinks or the like. Package does not include objects at a higher system level, like circuit boards and beyond, e.g. a housing in which the circuit board is enclosed.
unipolar	refers to semiconductor technology that primarily involves one type only of charge carrier, i.e. it involves either holes or electrons but not both
bipolar	refers to semiconductor technology that involves multi-carrier-type operation, i.e. which simultaneously uses both electrons and holes as charge carriers
MIS	metal-insulator-semiconductor
MOS	metal-oxide-semiconductor
FET	field-effect transistor
MISFET	metal-insulator-semiconductor field-effect transistor
TFT	thin-film transistor
active material	the material within which the physical effects that are characteristic of the device occur
auxiliary electrode	one part of a multi-layered electrode, often being metallic and intended to increase the conductivity of transparent oxide electrodes
coordination compound	a material having a chemical structure in which a central atom is chemically bonded to surrounding nonmetal atoms or groups of atoms. The central atom may be a metal atom or may be a metalloid (e.g. B, Si, Ge, As, Sb, Te or Po).
electroluminescent layer, emissive layer	the layer within which electrons and holes combine, resulting in light emission
organic device	a device that comprises one or more organic materials as the active material, e.g. using only organic active materials or e.g. using a combination of an organic material and another material
radiation-sensitive	refers to a device or a component that is sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation
tandem OLED	an OLED that comprises multiple electroluminescent units between one set of electrodes and a charge generation layer between the electroluminescent units

tandem PV cell	a photovoltaic cell that comprises multiple stacked photovoltaic units, e.g. p-n junctions, between one set of electrodes. Often each unit is made from a semiconductor of different bandgap energy, so each is sensitive to a different part of the electromagnetic spectrum.
terminal	the electrode or interconnection within a device, which serves as a connecting point between electrodes or interconnections within the device and interconnections that may be in the device's package or may be external to the device. An example is a bond pad on the cathode of an OLED, which may connect between the cathode electrode and a bonding wire in the OLED's package.
tiled display	a display that comprises a juxtaposition of smaller interconnected panels in order to achieve a large-area display

H10N

References

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