

H03M

CODING; DECODING; CODE CONVERSION IN GENERAL (using fluidic means [F15C 4/00](#); optical analogue/digital converters [G02F 7/00](#); coding, decoding or code conversion, specially adapted for particular applications, see the relevant subclasses, e.g. [G01D](#), [G01R](#), [G06F](#), [G06T](#), [G09G](#), [G10L](#), [G11B](#), [G11C](#), [H04B](#), [H04L](#), [H04M](#), [H04N](#); ciphering or deciphering for cryptography or other purposes involving the need for secrecy [G09C](#))

Definition statement

This place covers:

The scope of the subclass [H03M](#) is so broad that a detailed description of the subject matter appropriate for this place is correctly possible only at the main-group level, e.g. [H03M 7/00](#).

Provisions that are valid at a general level (e.g. of a kind appropriate to more than one of the main groups) are provided in the sections that follow.

The user is otherwise referred to the IPC definitions for the individual main groups of [H03M](#) which follow hereinafter. The following list is intended to assist the user.

Coding and decoding

In general	H03M 1/00
To or from differential modulation	H03M 3/00
In connection with keyboards	H03M 11/00

Conversion

Of the form of individual digits	H03M 5/00
Of the sequence of digits	H03M 7/00
Parallel/series or vice versa	H03M 9/00

Others

Error detection or error correction	H03M 13/00
Subject matter not provided for in other groups of this subclass	H03M 99/00

Relationships with other classification places

See the application places listed below the subclass title.

References

Limiting references

This place does not cover:

Using fluidic means	F15C 4/00
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Coding, decoding or code conversion, specially adapted for particular applications, see the relevant subclasses	G01D , G01R , G06F , G06T , G09G , G10L , G11B , G11C , H04B , H04L , H04M , H04N
Optical analogue/digital converters	G02F 7/00
Ciphering or deciphering for cryptography or other purposes involving the need for secrecy	G09C

H03M 1/00

Analogue/digital conversion; Digital/analogue conversion (conversion of analogue values to or from differential modulation [H03M 3/00](#))

Definition statement

This place covers:

- A/D or D/A converters as such.
- A/D or D/A conversion systems, e.g. systems comprising one or more A/D or D/A converters working together or systems comprising A/D or D/A converters in combination with other components such as gain stages, filters or which contribute to the overall A/D or D/A conversion.
- Position or velocity encoders insofar as their coding aspects are relevant.

Relationships with other classification places

The structural association with components such as transducers, sensors, gain stages or filters can be classified either in [H03M 1/00](#) or in the subclass covering the component (or in both the subclasses), depending on which aspect is more relevant.

In particular A/D or D/A converters represented as "black boxes" in a specific application (e.g. a measuring or telecommunication system) are in general not classified in [H03M](#).

Relations between [H03M 1/00](#) and [H03M 3/00](#)

A/D and D/A converters using differential modulation are classified in [H03M 3/00](#). According to the reference out following main group symbol [H03M 1/00](#), for all A/D and D/A converters using differential modulation, e.g. delta modulation, DPCM and nowadays in particular delta-sigma modulation, main group [H03M 3/00](#) has precedence over [H03M 1/00](#). Note however, that inventions actually relating to "normal" converters which are used as components within such differential modulators are classified in [H03M 1/00](#) again (because they can be more widely applied than only in the "differential" context). An example of the latter is dynamic element matching in D/A converters used in feedback paths of multi-bit delta-sigma A/D converters or in feedforward paths of multi-bit delta-sigma D/A converters, which is classified in group branch [H03M 1/066](#).

Position or velocity encoders

In principle the classification in [H03M 1/00](#) is directed to the coding aspects, whereas that in [G01D](#) or [G01P](#) is directed to the transducer aspects, but in practice they also appear to have subgroups directed to coding aspects.

Electro-optical A/D or D/A converters

In many cases inventors state to have invented an optical A/D or D/A converter though in fact only the sampling or signal conditioning is optical but the conversion itself is electronic. In principle both these cases and true electro-optical converters are classified in [H03M](#) while true optical converters are classified in [G02F 7/00](#), but in practice many electro-optical converters appear to have been classified in [G02F 7/00](#) as well.

References

Limiting references

This place does not cover:

A/D or D/A conversion using differential modulation	H03M 3/00
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Informative references

Attention is drawn to the following places, which may be of interest for search:

Digital delta-sigma modulators per se	H03M 7/3002
A/D or D/A converters using fluidic means (e.g. pneumatic, hydraulic)	F15C 4/00
Position encoders	G01D 5/00
Speed encoders	G01P 3/00
Measuring electric variables using an A/D converter	G01R 19/25
Testing combined analogue and digital circuits in general	G01R 31/3167
Electro-optical A/D or D/A converters	G02F 7/00
Time-to-digital converters	G04F 10/005
Current or voltage sources	G05F 3/00
Digital pulse width modulators per se, i.e. resulting in a discrete PWM signal	G06F 1/025 , H03M 5/08
Interfacing or handshaking between A/D or D/A converters on the one hand and computers on the other hand	G06F 3/05
Comparators : for comparing digital (multi-bit) signals for comparing logic signals for comparing analogue signals	G06F 7/02 , H03K 3/00 , H03K 5/24
A/D or D/A converters performing calculations (i.e. on two or more input signals)	G06J 1/00
Transmission of measurement or control data	G08C
Display devices, e.g. LCD displays, using D/A converters	G09G 3/00
Recording or reproducing data using A/D or D/A converters	G11B 20/10
S/H circuits in general	G11C 27/02
Multi-position switches	H01H 19/56
Operational amplifiers	H03F
Sample rate conversion	H03H 17/0416 , H03H 17/0621
Analogue pulse width modulators per se	H03K 7/08
Multiplexers per se	H03K 17/00
Transmission systems using pulse modulation	H04B 14/02
Multiplex transmission systems	H04J
Pulse-shaping in general	H04L 25/03
DC level restoring in general in television receivers	H04L 25/06 , H04N 5/18
Imagers using A/D converters	H04N 25/00
Integrated device structure	H10D 84/00 - H10D 89/00

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Pattern shifting code	Serial multiple bit code in which the first n--1 bits of each combination are identical to the last n-- 1 bits of the preceding combination. E.g. 000 001 010 101 011 111 110 100
Quantisation value generator	Component generating an analogue value corresponding to an elementary digital value, i.e. to a single bit or digit
Reconfigurable	The converter can be set to operate in different ways by setting switches to a particular position

Synonyms and Keywords

In patent documents the following abbreviations are often used:

English:

ADC	A/D converter
CODEC	coder and decoder
DAC	D/A converter
DEM	dynamic element matching
DWA	data weighted averaging
PWM	pulse width modulation
S/H circuit	sample/hold circuit
SAR	successive approximation register
SA-ADC	successive approximation type A/D converter

French:

CAD, CAN	A/D converter
CDA, CNA	D/A converter

German:

ADU, ADW	A/D converter
DAU, DAW	D/A converter

In patent documents the following expressions are often used as synonyms:

English:

Chain code	pattern shifting code
Encoder, digitiser, quantiser, binariser, voltage-to-digital converter	A/D converter
Flash converter	simultaneous A/D converter
Pipeline converter	synchronous multiple stage SA-ADC each stage of which operates on a different sample
Half -flash convertersemi-flash converter	multiple bits per stage type SA-ADC converting the input value either in two steps in a single flash converter or sequentially in two series-connected flash converters
Two -pass convertertwo-step converter	multiple bits per stage recirculation type SA-ADC converting the input value in two steps in a single flash converter
Dual rank converter extended-flash converter serial-parallel convertertwo-stage converter	multiple bits per stage type SA-ADC converting the input value sequentially in two series-connected flash converters
Algorithmic converter	recirculation type SA-ADC
Tracking converter	servo-type converter

French:

Convertisseur A/N, codeur, numériseur, quantificateur	A/D converter
Convertisseur N/A	D/A converter
Convertisseur instantané	parallel A/D converter

German:

A/D-Wandler, A/D-Übersetzer	A/D converter
D/A-Wandler, D/A-Übersetzer	D/A converter

H03M 1/002

{Provisions or arrangements for saving power, e.g. by allowing a sleep mode, using lower supply voltage for downstream stages, using multiple clock domains or by selectively turning on stages when needed}

Definition statement

This place covers:

This group deals with the provision of special means for saving power, e.g. for allowing a sleep mode.

Special rules of classification

Thus the group should not be used for overall designs using less power than prior ones.

H03M 1/02

Reversible analogue/digital converters

Definition statement

This place covers:

This group covers converters which are truly reconfigurable between A/D and D/A conversion as well as CODEC's having separate A/D and D/A converters with at least partially common control.

H03M 1/04

using stochastic techniques

Definition statement

This place covers:

converters in which the conversion process as such has a stochastic nature or which convert the analogue or digital signal to a (possibly intermediate) signal in which the information content is represented by stochastic parameters.

It does not cover the use of dither or the random selection among identical elements for averaging out errors.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Signal in which the information content is represented by stochastic parameters used for calculations	G06F 7/70
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H03M 1/0639

{using dither, e.g. using triangular or sawtooth waveforms (for increasing resolution [H03M 1/201](#))}

References

Limiting references

This place does not cover:

using dither for increasing resolution	H03M 1/201
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H03M 1/12

Analogue/digital converters ({[H03M 1/001](#) – } [H03M 1/10](#) take precedence)

Special rules of classification

[H03M 1/001](#) - [H03M 1/10](#) take precedence

H03M 1/1235

{Non-linear conversion not otherwise provided for in subgroups of [H03M 1/12](#)}

References**References out of a residual place**

Examples of places in relation to which this place is residual:

This group is residual to A/D converters having an intentionally non-linear transfer characteristic and not falling within the scope of anyone of groups	H03M 1/367 , H03M 1/464 , H03M 1/58 , H03M 1/62 .
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H03M 1/124

{Sampling or signal conditioning arrangements specially adapted for A/D converters}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

S/H circuits	G11C 27/02
Sample rate conversion	H03H 17/0416 , H03H 17/0621

H03M 1/245

{Constructional details of parts relevant to the encoding mechanism, e.g. pattern carriers, pattern sensors}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

Details of housings, casings or the like	G01 , H01 , H05
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H03M 1/301

{Constructional details of parts relevant to the encoding mechanism, e.g. pattern carriers, pattern sensors}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

Details of housings, casings or the like	G01 , H01 , H05
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H03M 1/36

simultaneously only, i.e. parallel type

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Asynchronous serial converters	H03M 1/42
Thermometer to binary encoders	H03M 7/165

Special rules of classification

It is noted that some patent documents deal with converters stated by the inventor to be "parallel converters using n comparators for n bits" or similar but in which in fact the reference values of the second and further comparators are modified according to the outputs of one or more preceding comparators. Thus, in reality these converters are not parallel but asynchronous serial converters falling within the scope of [H03M 1/42](#).

H03M 1/42

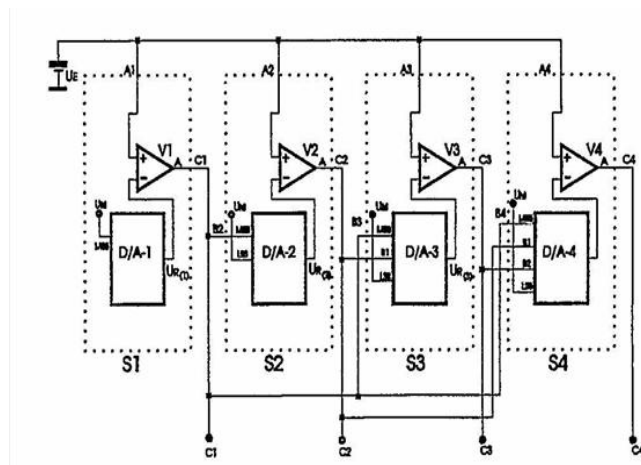
Sequential comparisons in series-connected stages with no change in value of analogue signal

Definition statement

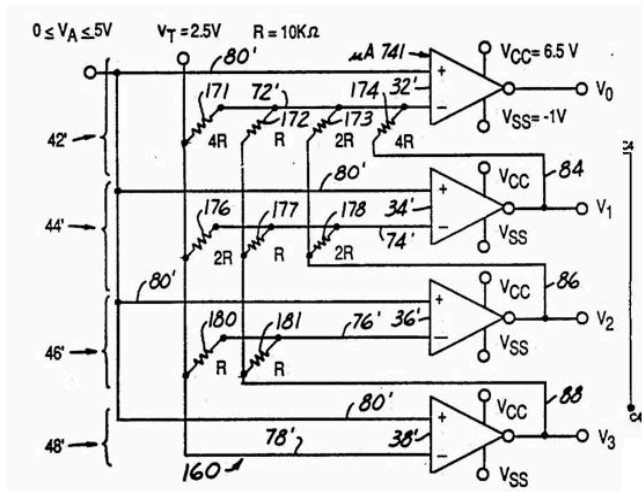
This place covers:

Multiple stage A/D converters in which the input signal is broadcasted to all stages while the reference value applied to each stage but the first one is modified by the output of one or more preceding stages.

Examples:



Definition statement



H03M 1/44

Sequential comparisons in series-connected stages with change in value of analogue signal

Definition statement

This place covers:

Multiple stage A/D converters in which the input signal is broadcasted to all stages while the reference value applied to each stage but the first one is modified by the output of one or more preceding stages.

H03M 1/48

Servo-type converters

Definition statement

This place covers:

A/D converters in which the output signal continuously tracks the input signal by means of reconversion of the output signal to an analogue feedback signal which is compared to the input signal.

The error signal usually adjusts the digital generator in one or the other direction, in dependence upon the sign of the error, in order to reach the correct position along the shortest route. However, occasionally the digital generator can be adjusted in one direction only; then it has to move circularly through nearly a full cycle in order to obtain a change in the other direction.

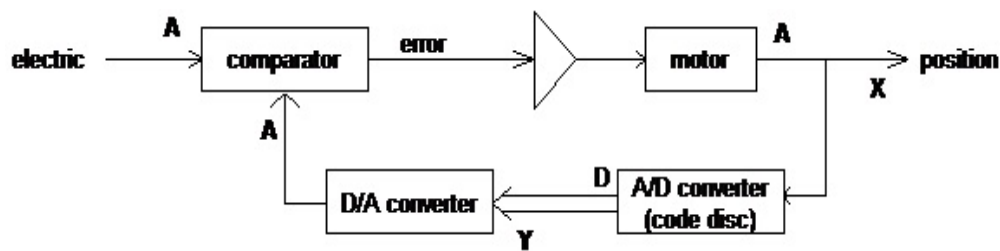
Relationships with other classification places

It is difficult sometimes to distinguish the latter systems from the range sweeping type ([H03M 1/56](#)) in which, however, the digital generator returns to a datum position between successive conversions.

The "successive approximation" type converters ([H03M 1/46](#)) are sometimes called "feedback converters" as well but are also reset between conversions.

Also, it is sometimes difficult to distinguish servo-type converters from A/D converters using differential modulation ([H03M 3/00](#)) which, however, deliver an output signal having a reduced number of bits at an oversampling rate, thus needing a decimation filter for converting it to a final result at full resolution and Nyquist rate. General analogue servo-systems using only digital feedback, for example as shown in the following block diagram, do, strictly spoken, not fall within the definition of an A/D conversion system.

However, they are very similar to an A/D conversion system using a D/A converter in a feedback arrangement (output Y instead of X) and therefore these systems are classified in [H03M 1/48](#) unless the converters are merely shown as black boxes.



H03M 1/50

with intermediate conversion to time interval ([H03M 1/64](#) takes precedence)

References

Limiting references

This place does not cover:

Analogue/digital converters with intermediate conversion to phase of sinusoidal or similar periodical signals	H03M 1/64
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Informative references

Attention is drawn to the following places, which may be of interest for search:

Time-to-digital converters	G04F 10/005
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H03M 1/66

Digital/analogue converters ({[H03M 1/001](#) – } [H03M 1/10](#) take precedence)

Special rules of classification

[H03M 1/001](#) - [H03M 1/10](#) take precedence

H03M 1/668

{Servo-type converters}

Definition statement

This place covers:

D/A converters in which the output signal continuously tracks the input signal by means of reconversion of the output signal to an digital feedback signal which is compared to the input signal.

The error signal usually adjusts the analogue generator in one or the other direction, in dependence upon the sign of the error, in order to reach the correct position along the shortest route. However, occasionally the analogue generator can be adjusted in one direction only; then it has to move circularly through nearly a full cycle in order to obtain a change in the other direction. It is difficult sometimes to distinguish the latter systems from the range sweeping type ([H03M 1/82](#)) in which, however, the analogue generator returns to a datum position between successive conversions.

H03M 1/78

using ladder network

Definition statement

This place covers:

Networks comprising impedances in series as well as parallel branches.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Networks having impedances in series branches only	H03M 1/76
Networks having impedances in parallel branches only	H03M 1/80

H03M 3/00

Conversion of analogue values to or from differential modulation

Definition statement

This place covers:

- Analogue differential modulators, e.g. delta modulators, differential pulse code modulators, delta-sigma modulators;
- A/D and D/A converters or conversion systems using differential modulation.

Relationships with other classification places

The structural association with components such as transducers, sensors, gain stages or filters can be classified either in [H03M 3/00](#) or in the subclass covering the component (or in both the subclasses), depending on which aspect is more relevant.

In particular differential modulators represented as "black boxes" in a specific application (e.g. a measuring or telecommunication system) are in general not classified in [H03M](#).

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Digital delta-sigma modulators	H03M 7/3004
Recording or reproducing data using A/D or D/A converters	G11B 20/10
Transmission systems using differential modulation	H04B 14/06

Synonyms and Keywords

In patent documents the following abbreviations are often used:

ADM	Adaptive Delta Modulator
ADPCM	Adaptive Differential Pulse Code Modulator
ADSM	Adaptive Delta-Sigma Modulator
DM	Delta Modulator

DPCM	Differential Pulse Code Modulator
DPWM	Differential Pulse Width Modulator
DSM	Delta-Sigma Modulator
MASH	Multiple Stage Noise Shaping Delta-Sigma Modulator
SDM	Sigma-Delta Modulator

In patent documents the following expressions are often used as synonyms:

Bitstream converter	A/D converter using single bit delta-sigma modulation
Noise-shaper	delta-sigma modulator
Sigma-delta modulator	delta-sigma modulator

H03M 3/04

Differential modulation with several bits {, e.g. differential pulse code modulation [DPCM] ([H03M 3/30](#) takes precedence)}

References

Limiting references

This place does not cover:

Delta-sigma modulation	H03M 3/30
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Informative references

Attention is drawn to the following places, which may be of interest for search:

Voice coding	G10L 19/00
Image coding	H04N 19/00

H03M 3/354

{at one point, i.e. by adjusting a single reference value, e.g. bias or gain error}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Gain setting for range control	H03M 3/478
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H03M 3/382

{at one point of the transfer characteristic, i.e. by adjusting a single reference value, e.g. bias or gain error}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

Gain setting for range control	H03M 3/478
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H03M 3/494

{Sampling or signal conditioning arrangements specially adapted for delta-sigma type analogue/digital conversion systems}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

Sample/hold circuits	G11C 27/02
Sample rate conversion	H03H 17/0416 , H03H 17/0621

H03M 3/508

{Details relating to the interpolation process}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

Interpolation filters in general	H03H 17/0416 , H03H 17/0621
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H03M 5/00

Conversion of the form of the representation of individual digits

Definition statement

This place covers:

Conversion of codes where one aspect is the representation of the code as a signal, e.g. a code embodied by pulses or other shapes (e.g. sinusoidal). Examples are modulation codes (like Manchester coding).

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

A/D or D/A conversion	H03M 1/00
Differential modulation	H03M 3/00 , H03M 7/3002

Special rules of classification

In groups [H03M 5/02](#) - [H03M 5/22](#), in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

Classification of additional information:

- The invention as such as well as additional information shall be classified.
- The use of the Indexing Codes for classification is compulsory and shall be used in addition to the appropriate CPC Symbol.
- For the search in main group [H03M 5/00](#) it is noted that additional information has been classified in this group from 01--04--2004 onwards.

H03M 7/00

Conversion of a code where information is represented by a given sequence or number of digits to a code where the same {, similar or subset of} information is represented by a different sequence or number of digits

Definition statement

This place covers:

A sequence of numerical or textual symbols representing a code and transformations/conversions thereof into a different sequence of numbers or textual symbols. It comprises in particular code conversions resulting in shorter codes (data compression and decompression).

The sequence of textual symbols could be part of a structured text document, for example an XML document.

Also covered are devices which provide for such code conversion, e.g. hardware implemented code converters and code converters based on logic circuit and programmable converters.

Furthermore, data reduction methods in order to get a short representation of a signal or of digital data in general are also covered. An example would be methods for reducing the number of necessary samples in data acquisition.

Relationships with other classification places

Relations between [H03M 7/46](#) and [H03M 5/145](#):

- [H03M 7/46](#) deals with data compression by replacing a sequence of same digits/characters with the value of the digit/character and a specification of its number (run-length code/compression).
- [H03M 5/145](#) deals with run-length-limited codes, i.e. modulation schemes which contain a maximum number of same digits.

Relations between [H03M 7/30](#) and [H04N 19/00](#):

Use of data compression bandwidth reduction for in video coding ([H04N 19/00](#)) when the data compression is merely represented as a "black box" are not in the scope of [H03M 7/30](#). However, if a certain data compression scheme for video bandwidth reduction is detailed and goes beyond conventional compression algorithms, this new aspect can be classified in [H03M 7/30](#). An example is

Relationships with other classification places

the use of arithmetic coding in video coding (e.g. CABAC) where specific aspects should be classified under [H03M 7/30](#).

In general, data compression schemes merely represented as "black boxes" in a certain application field should not be classified under [H03M 7/00](#).

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Use of compressive sensing	G01L 1/00 , G01L 5/00
Processing of structured documents, e.g. xml, also for the purpose of size reduction	G06F 40/12
Audio coding	G10L 19/00
Source coding for video and arithmetic data compression for video coding	H04N 19/00

Special rules of classification

- In groups [H03M 7/02](#) - [H03M 7/50](#), in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

Classification of additional information:

- The invention as such as well as additional information shall be classified.
- The use of the Indexing Codes for classification is compulsory and shall be used in addition to the appropriate ECLA code.
- For the search in main group [H03M 7/00](#) it is noted that in general additional information has been classified in this group from 01--04--2004 onwards. However, in group branch [H03M 7/3002](#) it has been classified for all documents.

Further information:

[H03M 7/26](#)

This subgroup deals solely with data compression and is not to be used for run-length-limited modulation techniques.

[H03M 7/30](#)

This group branch in general deals with all types of data compression unless the data compression is specified merely as a "black box". It also deals with precoding before the actual compression stage in order to get better compression results (e.g. Burrows-Wheeler transform).

[H03M 7/3002](#)

This group branch deals with digital differential modulation, e.g. delta modulation [DM], differential pulse code modulation [DPCM], delta-sigma modulation.

Synonyms and Keywords

In patent documents the following abbreviations are often used:

ADM	Adaptive Delta Modulator
ADPCM	Adaptive Differential Pulse Code Modulator
ADSM	Adaptive Delta-Sigma Modulator
CABAC	Context-Adaptive Binary Arithmetic Coding

CAVLC	Context-Adaptive Variable Length Coding
DM	Delta Modulator
DPCM	Differential Pulse Code Modulator
DPWM	Differential Pulse Width Modulator
DSM	Delta-Sigma Modulator
LZ	Lempel-Ziv
MASH	Multiple Stage Noise Shaping Delta-Sigma Modulator
SDM	Sigma-Delta Modulator
VLC	Variable-Length Coding

In patent documents the following expressions are often used as synonyms:

Error quantiser	error feedback type delta-sigma modulator
Noise-shaper	delta-sigma modulator
Sigma-delta modulator	delta-sigma modulator

H03M 7/20

Conversion to or from n-out-of-m codes

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Number-of-one counters	G06F 7/607
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H03M 7/26

Conversion to or from stochastic codes

Definition statement

This place covers:

This subgroup deals solely with data compression and is not to be used for run-length-limited modulation techniques.

H03M 7/30

Compression (speech analysis-synthesis for redundancy reduction [G10L 19/00](#); for image communication [H04N](#)); Expansion; Suppression of unnecessary data, e.g. redundancy reduction

Definition statement

This place covers:

all types of data compression unless the data compression is specified merely as a "black box". It also deals with precoding before the actual compression stage in order to get better compression results, e.g. Burrows-Wheeler transform.

References

Limiting references

This place does not cover:

Speech analysis-synthesis for redundancy reduction	G10L 19/00
Speech analysis-synthesis for image communication	H04N

Informative references

Attention is drawn to the following places, which may be of interest for search:

Data acquisition	G06F 17/40
Image data processing	G06T 9/00
Redundancy reduction in data recording	G11B 20/14
Transmission	H04B 1/66

H03M 7/3044

{Conversion to or from differential modulation with several bits only, i.e. the difference between successive samples being coded by more than one bit, e.g. differential pulse code modulation [DPCM] ([H03M 7/3004](#) takes precedence; voice coding [G10L 19/00](#); image coding [H04N 19/00](#))}

References

Limiting references

This place does not cover:

Digital delta-sigma modulation	H03M 7/3004
Speech analysis-synthesis for redundancy reduction	G10L 19/00
Speech analysis-synthesis for image communication	H04N 19/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Image data processing	G06T 9/00
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H03M 9/00

Parallel/series conversion or vice versa (digital stores in which the information is moved stepwise per se [G11C 19/00](#))

Definition statement

This place covers:

Parallel/series conversion or vice-versa, in general;

Timing and synchronisation aspects thereof.

References

Limiting references

This place does not cover:

Parallel/series conversion or vice-versa of bits, or groups of bits, which are specifically adapted for transmission in telecommunication or data communication apparatus	H04J 3/047
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Informative references

Attention is drawn to the following places, which may be of interest for search:

Generation or distribution of clock signals, per se	G06F 1/04
Regularising the speed of data flow, e.g. using first in first out registers for implementing a data queue, per se	G06F 5/06
Frequency multipliers or dividers, per se	G06F 7/68
Digital stores in which the information is moved stepwise, per se	G11C 19/00
Synchronisation of pulse signals to a clock signal, per se	H03K 5/135
Multiplexer switches, per se	H03K 17/002 , H03K 17/62 , H03K 17/693 , H03K 17/76
Frequency dividers using counters, per se	H03K 21/00 - H03K 29/00
Phase locked loops or delay locked loops, per se	H03L 7/00
Synchronisation of a data receiver with a transmitter, per se	H04L 7/00
Line transmission arrangements where a single bit stream is divided between several channels and reassembled at the receiver, per se	H04L 25/14

H03M 11/00

Coding in connection with keyboards or like devices, i.e. coding of the position of operated keys (keyboard switch arrangements, structural association of coders and keyboards [H01H 13/70](#), [H03K 17/94](#))

References

Limiting references

This place does not cover:

Mapping, i.e. converting a generated code set to a different one	G06F 3/023
Virtual, i.e. software generated keyboards	G06F 3/023
Constructional details of keys or keyboards	H01H 13/70
Electrical details of keyboard switches	H03K 17/94

Synonyms and Keywords

In patent documents the following expressions are often used as synonyms:

Ghost key	Phantom key
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H03M 13/00

Coding, decoding or code conversion, for error detection or error correction; Coding theory basic assumptions; Coding bounds; Error probability evaluation methods; Channel models; Simulation or testing of codes (error detection or error correction for analogue/digital, digital/analogue or code conversion [H03M 1/00](#) – [H03M 11/00](#); specially adapted for digital computers [G06F 11/08](#); for information storage based on relative movement between record carrier and transducer [G11B](#), e.g. [G11B 20/18](#); for static stores [G11C](#))

Definition statement

This place covers:

Encoding, decoding, coding or decoding schemes for the correction or detection of errors, i.e. error control coding (ECC) or forward error correction (FEC)

- Codes for the correction or detection of errors, e.g. block codes, convolutional codes or concatenated codes
- Construction or design (including modification of existing codes by e.g. puncturing or extension) of codes for the correction or detection of errors
- Algorithms, methods or devices for encoding or decoding of codes for the correction or detection of codes
- Unequal error protection codes or schemes, i.e. codes or coding schemes that provide several levels of error protection

Coded modulation for error detection or correction.

Combination of error correction coding and techniques for the efficient use of the spectrum, e.g. modulation codes with error correction properties

Synchronisation by means of error correction codes

Relationships with other classification places

[H03M 13/00](#) has relationships with a plurality of different other technical areas, wherein the relationships are characterised in that the other technical areas relate to applications and frameworks to which the [H03M 13/00](#) specific techniques are applied.

Techniques for error control coding and forward error correction, which are characterised by their intrinsic nature, which is independent of its field of use, are to be classified in [H03M 13/00](#). This makes [H03M 13/00](#) a function-oriented place.

The application of techniques for error control coding or forward error correction in the sense that a function is plugged into an application without modification of the intrinsic properties of the function itself is only to be classified in the respective application place (e.g. the use of a CRC check to determine whether data read from a memory is error free, the use of Reed-Solomon codes on a recording medium, the use of LDPC coded modulation in a transmitter arrangement).

If the application requires an adaptation of the techniques for error control coding or forward error correction to a particular application place, which involves a modification of the intrinsic properties of the function as well, then the classification in the function-oriented place and the application place is obligatory (e.g. the use of a CRC in a memory wherein the CRC calculation is parallelized in order to increase the read speed; this modification involves an intrinsic property of the CRC calculation; e.g. the design of an LDPC code having particular distance properties for a LDPC coded modulation scheme in a transmitter arrangement).

The application places that have relationships with [H03M 13/00](#) are as follows:

Relationships with other classification places

- The mere application of error control coding or forward error correction to memories and computers: [G06F 11/00](#), in particular [G06F 11/08](#);
- The mere application of error control coding or forward error correction to recording: [G11B 20/00](#), in particular [G11B 20/18](#);
- The mere application of error control coding or forward error correction to static stores: [G11C 29/00](#);
- The mere application of error control coding or forward error correction to arrangements at the transmitting and receiving sides of transmission systems: [H04L 1/00](#)
- The mere application of error control coding or forward error correction to packet switched networks (e.g. packet loss): [H04L 12/00](#)
- The mere application of error control coding or forward error correction to base band systems for channel estimation, detection (e.g. sequence estimation, MAP detection) and equalisation: [H04L 25/00](#)
- The mere application of error control coding or forward error correction to modulated carries systems: [H04L 27/00](#)
- The mere application of error control coding or forward error correction to signalling and control (for e.g. protocol aspects such as error control mechanisms in multimedia streaming protocols): [H04L 65/00](#), for e.g. protocol aspects (e.g. error control mechanisms in multimedia streaming protocols)
- The mere application of error control coding or forward error correction to television systems: [H04N 7/0357](#) and [H04N 19/89](#)
- [H03M 13/00](#) is the application place for functions from [G06F 7/00](#), e.g. finite field processing ([G06F 7/00](#)) for encoding or decoding of Reed-Solomon codes.

References

Limiting references

This place does not cover:

Error detection or error correction for analogue/digital, digital analogue or code conversion	H03M 1/00 - H03M 11/00
Information storage based on relative movement between record carrier and transducer	G03B
Specially Adapted for digital computers	G06F 11/08
Static stores	G11C
Error detection or Error correction in transmission systems	H04L 1/004
Television Systems	H04N 7/0357

Informative references

Attention is drawn to the following places, which may be of interest for search:

Implementation aspects regarding operations, e.g. finite field processing	G06F 7/00
Application places in which specially adapted ECC/FEC techniques may be found	G06F 11/00 , G11B 20/00 , G11C 29/00 , H04L 1/00 , H04L 12/00 , H04L 25/00 , H04L 27/00 , H04N 7/00
Cryptographic mechanisms or cryptographic; arrangements for secret or secure communications; Network security protocols	H04L 9/00
Network architectures or network communication protocols for network security	H04L 63/00

Network arrangements, protocols or services for supporting real-time applications in data packet communication	H04L 65/00
Network arrangements or protocols for supporting network services or applications	H04L 67/00

Special rules of classification

The invention as such as well as additional information shall be classified

[H03M 13/61](#) - [H03M 13/65](#) are used to introduce a so-called 2nd dimension to the classification and are, thus, always to be used in combination with one of the subgroups of the range [H03M 13/00](#)-[H03M 13/45](#) or the corresponding Indexing Codes

Component or constituent codes within a particular scheme are to be classified by means of the appropriate Indexing Codes; for instance, a product code built from a Reed-Muller code and a BCH code should be classified using [H03M 13/2909](#) (product code) and [H03M 13/136](#) and [H03M 13/152](#) to indicate its component codes

For the search in main group [H03M 13/00](#) it is noted that additional information has been classified in this group from 01-04-2004 onwards.

Further information:

It follows a brief explanation of those CPC subgroups, where it might not be clear from the wording alone what technical features are meant to fall within their scope:

[H03M 13/6362](#)

- covers punctured codes in general and particular details regarding a strategy/scheme for rate matching by puncturing that extends beyond the mere use of punctured codes
- [H03M 13/6368](#), [H03M 13/6393](#) should be used when a particular type of puncturing is used, viz. rate compatible or complementary puncturing

[H03M 13/033](#)

- this subgroup covers methods for the construction of codes, wherein the generic term construction covers the design of generator and parity-check matrices, the design of generator polynomials, the design of mapping schemes, the design of puncturing schemes etc.
- if the design includes a computer search or a random component with subsequent optimisation, then the subgroup [H03M 13/033](#) shall be allocated

[H03M 13/091](#)

- this subgroup covers the calculation of CRCs (either during encoding or decoding) when the calculation is performed in a parallel or partly parallel manner, e.g. by 8 or 32 bit parallel processing
- in contrast to partly parallel or parallel processing, there is serial processing in which a CRC is calculated 1 bit by 1 bit as it is done with a conventional linear feed-back shift register

[H03M 13/093](#)

- in some applications a CRC is calculated over an information word of n bits
- during transmission over a plurality of hops, the information word may be updated, e.g. some bits in the header are changed, which requires a recalculation of the CRC
- methods that do not fully recalculate the CRC but update the CRC only in respect to the changes of the information word (by exploitation of the linearity of the CRC code) are to be classified here

[H03M 13/1114](#)

- known in the literature as "Memory-Aware Decoder Architectures" and "Merged-Schedule Message-Passing (MSMP) algorithm"

- see XP011104612 page 980, Section [C](#) for a detailed description
- the memory efficiency is mainly due to eliminating the storage required to save every bit-to-check messages or check-to-bit messages as in the standard message passing decoding algorithm

[H03M 13/1131](#)

- scheduling is the order in which the messages of the graph should be propagated
- the "classical" scheduling is the so-called flooding schedule, where all nodes of one class, e.g. all messages send from bit nodes to check nodes, are updated before the nodes of the other class, e.g. all messages send from variable nodes to check nodes, are updated; this can be done one node at a time (serially) or in parallel.
- full parallel flooding schedule processing should be classified under [H03M 13/1134](#) (Remark: any full parallel schedule is implicitly a flooding schedule) and partly parallel flooding schedule processing under [H03M 13/1137](#)
- note that serial flooding schedules are not explicitly classified
- the "shuffled" scheduling mixes check node and variable node processing, e.g. check node processing of some check nodes is started before all variable nodes have been updated; this again can be performed serially, i.e. one node after the other, or partly-parallel, i.e. several nodes in parallel.
- serial "shuffled" scheduling should solely be classified under [H03M 13/114](#).
- partly-parallel "shuffled" scheduling should be classified under [H03M 13/1137](#) and [H03M 13/114](#).

[H03M 13/155](#)

- only for shortened or extended codes that fit into [H03M 13/151](#); these codes include in particular Reed-Solomon and BCH codes
- code shortening or extension for codes other than that, i.e. for codes that are not associated with error location and error correction polynomials, are to be classified under [H03M 13/618](#); these codes include, for instance, Hamming codes or LDPC codes

[H03M 13/1555](#)

- decoder implementations that comprise a set of data processing elements connected in series, so that the output of one element is the input of the next one and so that the elements of a pipeline are often executed in parallel or in time-sliced fashion
- for instance, Reed-Solomon decoders are often implemented using a pipeline with 3 stages for syndrome calculation, calculation of the error locator polynomial and Chien search; cf. e.g. US2003140303

[H03M 13/1565](#)

- a cyclic block code with minimum hamming distance d can correct up to $(d-1)/2$ errors
- however, as long as the code is not perfect, i.e. does not meet the Hamming bound, there exist error patterns with weight greater than $(d-1)/2$ that can be corrected
- algorithms that provide decoding beyond $(d-1)/2$ errors are to be classified using [H03M 13/1565](#)

[H03M 13/157](#)

- evaluation of polynomial equations, e.g. syndrome evaluation using a blockwise parallelized Horner scheme

[H03M 13/1575](#)

- direct decoding denotes decoding methods/decoders that do not require the calculation and evaluation of the error locator polynomial by means of complex algorithms like Berlekamp-Massey decoding or Chien search
- direct decoding is limited to small error weights or codes with small minimum Hamming distance
- by means of direct decoding the error locator polynomial or its roots or even the error values can be directly determined from the syndromes

[H03M 13/158](#)

Methods and arrangements for finite field processing when applied in an encoder or decoder for error correcting codes, e.g. a finite field multiplier.

If the finite field processing is not disclosed in the context of error control coding, then this class is not to be given.

Methods and arrangements for finite field arithmetic are always to be circulated to [G06F 7/72](#).

[H03M 13/25](#)

Coded modulation.

The subgroups [H03M 13/251](#) - [H03M 13/258](#) provide details as to the type of code that is used.

The type of code can be further refined by using the appropriate Indexing Code or ECLA subgroup; e.g. coded modulation with a Reed-Muller code would be classified using [H03M 13/251](#) (coded modulation with block coding) and [H03M 13/136](#) (Reed-Muller codes).

[H03M 13/27](#)

For a complete classification of a document concerning interleaving, it may be required to allocate more than one subgroup of [H03M 13/27](#) to the document.

[H03M 13/2703](#) - [H03M 13/2757](#) relate to different types of interleavers, whereas [H03M 13/2771](#) - [H03M 13/2796](#) relate to characteristics other than the type of interleaving.

Hence, a document relating to interleaving should usually have a designation of the type of interleaving ([H03M 13/2703](#) - [H03M 13/2757](#)) and optionally one or more classes relating to the other characteristics ([H03M 13/2771](#) - [H03M 13/2796](#)).

[H03M 13/2771](#) indicates that the document deals with interleavers/interleaving for turbo codes (so-called turbo code internal interleavers).

[H03M 13/2728](#)

This subgroup covers the principle underlying a helical type interleaver for 1-bit dummy codes

[H03M 13/276](#)

This subgroup covers the actual calculation of interleaving addresses.

Note that the principle underlying a particular interleaving type may be described without actually providing details about how the address or index calculation is performed or implemented.

If a document does not only relate to a particular type of interleaver but provides in addition details about the calculation of interleaver addresses or indices, then this class should be given in addition.

[H03M 13/2764](#)

Circuits/hardware implementations for the calculation of interleaver addresses or indices.

See also the comments w.r.t. [H03M 13/276](#).

[H03M 13/2912](#)

Product codes in which the sub-block comprising the checks-on-checks or parity-on-parity is not present (as it is either not generated or removed).

[H03M 13/2927](#)

Turbo decoding of concatenated block codes is to be classified in [H03M 13/2963](#).

If the decoding strategy involves iterative decoding different from turbo decoding, e.g. sub-sequent decoding of rows and columns of a product code, then this feature (iterative decoding) is to be classified using [H03M 13/2948](#).

[H03M 13/2939](#)

Coding schemes including any concatenation of two or more convolutional codes, wherein decoding is not based on the turbo principle, e.g. serial concatenation of convolutional codes without turbo decoding.

[H03M 13/2948](#)

If the decoding strategy involves iterative decoding different from turbo decoding, e.g. decoding without exchange of extrinsic soft-decision information between decoders, then this feature (iterative decoding) is to be classified using [H03M 13/2948](#).

[H03M 13/2957](#)

Note that [H03M 13/2957](#) is also to be allocated when a component code is replaced by a non-coded constraint, e.g. turbo equalisation (cf. also the Glossary of terms and the comments on [H03M 13/63](#)).

[H03M 13/333](#)

Feedback from the channel decoder to a synchronisation unit is used to establish synchronisation with respect to a frame or block of bits.

[H03M 13/336](#)

Phase recovery in combination with channel decoding, wherein feedback from the channel decoder to phase estimation is used to achieve or improve the recovery/estimation of the symbol phase.

[H03M 13/3707](#)

Decoding methods or techniques providing more than one decoding algorithm for one code and selection of the appropriate decoding method or technique

Adaptive decoding in which decoding is adapted to some extrinsic or intrinsic parameter, e.g. setting of internal thresholds.

[H03M 13/3715](#)

The extrinsic or intrinsic parameter is the number of estimated errors or information about the state of the channel (e.g. SNR).

[H03M 13/3723](#)

Initialisation is meant to denote the configuration of the decoder (e.g. setting of internal variables) prior to decoding.

Initialisation of MAP decoders for turbo decoding using the result of the previous iteration; initialisation of variable nodes for LDPC code decoding; initialisation of state probabilities for a tail-biting MAP decoder.

[H03M 13/3776](#)

Note that re-encoding is often performed to estimate error rates but is not integral to decoding as such.

[H03M 13/3994](#)

For trellis decoding, some bits may be known (e.g. during decoding of concatenated codes, padding bits) to the decoder, which exploits this information as a priori information.

The trellis decoder is forced to take the a priori known decision, for instance, by adding to the ACS circuit a decision-overriding logic or by saturating state or branch metrics.

This technique is sometimes referred to by state pinning or decision forcing or trellis pruning.

[H03M 13/451](#)

For decoding, the optimum code word (in terms of a metric) is searched in a set of possible code words

The set of possible code words is often denoted by candidate code words

[H03M 13/456](#)

This subgroup includes maximum likelihood or MAP decoding, wherein a list of all code words of the code or its dual code is processed.

[H03M 13/458](#)

SISO decoding of block codes with updating of hard decisions of most reliable symbols using extrinsic information from least reliable symbols.

[H03M 13/613](#)

Use of properties of the code to be encoded or decoded that relate to its dual code.

This includes, for instance, decoding using the trellis of the dual code instead of that of the code itself.

[H03M 13/63](#) and its subgroups:

These subgroups are intended to cover the combination of error control coding and other techniques.

These subgroups are in particular important when the so-called turbo principle is applied to e.g. demodulation (turbo demodulation) or equalisation (turbo equalisation); then, [H03M 13/2957](#) is to be used to indicate the use of the turbo principle and [H03M 13/6325](#) and [H03M 13/6331](#), respectively, are used to indicate the non-coded constraint.

[H03M 13/65](#) and its subgroups:

- These subgroups are in general independent of the error control code/scheme and relate to implementation aspects and the intended application (in terms of standardized communication systems)
- [H03M 13/6569](#) is used for documents that are specific to implementations on processors or in software (e.g. software defined radio)
- [H03M 13/6575](#) covers implementations using circuits without memory, e.g. boolean circuits; these type of circuits are often applied to encoding and decoding when the operations can be expressed by means of boolean algebra

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Product	mathematical operation
Turbo	the term turbo denotes the principle that soft-decision information is exchanged in an iterative manner between two decoders or between one decoder and another unit like e.g. a demodulator or equaliser; turbo is also used to denote a code (turbo code) that can be turbo decoded, e.g. a parallel concatenated convolutional code or a serial concatenated convolutional code

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

ACS	Add-Compare-Select
APP	A Posteriori Probability
BCM	Block Coded modulation
BP	Belief Propagation
CC	Convolutional Code
DED	Double Error Detecting
ECC	Error Control Codes/Coding
EDC	Error Detection/Detecting Code
EG	Euclidian Geometry
EXIT	EXtrinsic Information Transfer
FEC	Forward Error Correction
GF	Galois Field
GMD	Generalised Minimum Distance
LDPC	Low-Density Parity-Check
MAP	Maximum A Posteriori
LLR	Log-Likelihood Ratio
MDS	Maximum Distance Separable
ML	Maximum Likelihood
MLD	Maximum Likelihood Decoding
PCCC	Parallel Concatenated Convolutional Code
QC	Quasi-Cyclic
OSD	Ordered Statistics Decoding
RM	Reed-Muller
RS	Reed-Solomon
RSC	Recursive Systematic Convolutional code
SCCC	Serial Concatenated Code
SEC	Single Error Correcting
SISO	Soft-In Soft-Out
SOVA	Soft-Output Viterbi Algorithm
SPA	Sum-Product Algorithm
TB	Tail-Biting
TCM	Trellis-Coded Modulation
UEP	Unequal Error Protection
VA	Viterbi Algorithm

In patent documents, the following words/expressions are often used as synonyms:

- "CRC", "FCS" and "BCS"
- "message passing", "sum-product algorithm", "belief propagation"

- "APP", "MAP", and "BCJR"
- "Max-LOG-MAP", "maxlogMAP", "maxAPP"
- "LDPC codes" and "Gallager codes"

H03M 13/09

Error detection only, e.g. using cyclic redundancy check [CRC] codes or single parity bit

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Error detection or correction by redundancy in data representation	G06F 11/08
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H03M 13/158

{Finite field arithmetic processing}

Definition statement

This place covers:

Methods and arrangements for finite field processing when applied in an encoder or decoder for error correcting codes, e.g. a finite field multiplier.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Methods or arrangements for finite field arithmetic	G06F 7/72
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Special rules of classification

If the finite field processing is not disclosed in the context of error control coding, then this group is not to be given.

H03M 13/2975

{Judging correct decoding, e.g. iteration stopping criteria}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Stopping criteria for iterative decoding	H04L 1/0051
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H03M 13/3905

{Maximum a posteriori probability [MAP] decoding or approximations thereof based on trellis or lattice decoding, e.g. forward-backward algorithm, log-MAP decoding, max-log-MAP decoding}

References**Informative references**

Attention is drawn to the following places, which may be of interest for search:

MAP decoding for transmission of digital information	H04L 1/0055
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H03M 99/00

Subject matter not provided for in other groups of this subclass

References**Limiting references**

This place does not cover:

Analogue/digital conversion; Digital/analogue conversion	H03M 1/00
Conversion of analogue values to or from differential modulation	H03M 3/00
Conversion of the form of the representation of individual digits	H03M 5/00
Conversion of a code where information is represented by a given sequence or number of digits to a code where the same information is represented by a different sequence or number of digits	H03M 7/00
Parallel/series conversion or vice versa	H03M 9/00
Coding in connection with keyboards or like devices, i.e. coding of the position of operated keys	H03M 11/00
Coding, decoding or code conversion, for error detection or error correction; Coding theory basic assumptions; Coding bounds; Error probability evaluation methods; Channel models; Simulation or testing of codes	H03M 13/00