CPC  COOPERATIVE PATENT CLASSIFICATION

H  ELECTRICITY
(NOTE omitted)

H03  BASIC ELECTRONIC CIRCUITRY

H03M  CODING; DECODING; CODE CONVERSION IN GENERAL (using fluidic means F15C 4/00; optical analogue/digital converters G02F 7/00; coding, decoding or code conversion, specially adapted for particular applications, see the relevant subclasses, e.g. G01D, G01R, G06F, G06T, G09G, G10L, G11B, G11C, H04B, H04L, H04M, H04N; ciphering or deciphering for cryptography or other purposes involving the need for secrecy G09C)

WARNINGS

1. The following IPC groups are not in the CPC scheme. The subject matter for these IPC groups is classified in the following CPC groups:
   H03M 7/32 covered by H03M 7/3002, H03M 7/3004, H03M 7/3006, H03M 7/3008, H03M 7/3011, H03M 7/3013, H03M 7/3015, H03M 7/3017, H03M 7/302, H03M 7/3024, H03M 7/3028, H03M 7/3031, H03M 7/3033, H03M 7/3035, H03M 7/3037, H03M 7/304, H03M 7/3042, H03M 7/3048
   H03M 7/34 covered by H03M 7/3051
   H03M 7/36 covered by H03M 7/3022, H03M 7/3026, H03M 7/3044
   H03M 7/38 covered by H03M 7/3046
   H03M 7/44 covered by H03M 7/3049

2. In this subclass non-limiting references (in the sense of paragraph 39 of the Guide to the IPC) may still be displayed in the scheme.

1/00 Analogue/digital conversion; Digital/anogue conversion (conversion of analogue values to or from differential modulation H03M 3/00)
1/001 . (Analogue/digital/anogue conversion)
1/002 . [Provisions or arrangements for saving power, e.g. by allowing a sleep mode, using lower supply voltage for downstream stages, using multiple clock domains or by selectively turning on stages when needed]
1/004 . [Reconfigurable analogue/digital or digital/anogue converters (H03M 1/02 takes precedence)]
1/005 . . (among different converters types]
1/007 . . (among different resolutions]
1/008 . . (among different conversion characteristics, e.g. between mu-255 and a-laws]
1/02 . Reversible analogue/digital converters
1/06 . Continuously compensating for, or preventing, undesired influence of physical parameters (periodically, e.g. by using stored correction values, H03M 1/10)
1/0602 . . (of deviations from the desired transfer characteristic [H03M 1/0617 takes precedence])
1/0604 . . . (at one point, i.e. by adjusting a single reference value, e.g. bias or gain error (gain setting for range control H03M 1/18))
1/0607 . . . . (Offset or drift compensation (removal of offset already present on the analogue input signal H03M 1/1295))
1/0609 . . . [at two points of the transfer characteristic, i.e. by adjusting two reference values, e.g. offset and gain error]
1/0612 . . . [over the full range of the converter, e.g. for correcting differential non-linearity]
1/0614 . . . [of harmonic distortion (H03M 1/0617 takes precedence)]
1/0617 . . . [characterised by the use of methods or means not specific to a particular type of detrimental influence]
1/0619 . . . [by dividing out the errors, i.e. using a ratiometric arrangement]
1/0621 . . . . [with auxiliary conversion of a value corresponding to the physical parameter(s) to be compensated for]
1/0624 . . . . [by synchronisation]
1/0626 . . . . [by filtering]
1/0629 . . . . [Anti-aliasing]
1/0631 . . . . [Smoothing]
1/0634 . . . . [by averaging out the errors, e.g. using sliding scale]
1/0636 . . . . . [in the amplitude domain]
1/0639 . . . . . [using dither, e.g. using triangular or sawtooth waveforms (for increasing resolution H03M 1/201)]
1/0641 . . . . . . [the dither being a random signal]
1/0643 . . . . . . [in the spatial domain]
of noise { (H03M 1/0617 takes precedence) }
1/10872 . . . . (by disabling changes in the output during the transitions, e.g. by holding or latching)

1/10881 . . . . (by forcing a gradual change from one output level to the next, e.g. soft-start)

1/1089 . . . . [of temperature variations]

1/10 Calibration or testing

1/1004 . . . . (without interrupting normal operation, e.g. by providing an additional component for temporarily replacing components to be tested or calibrated (H03M 1/1009, H03M 1/1071 take precedence))

1/1009 . . . . [Calibration]

1/1014 . . . . [at one point of the transfer characteristic, i.e. by adjusting a single reference value, e.g. bias or gain error (gain setting for range control H03M 1/18)]

1/1019 . . . . [by storing a corrected or correction value in a digital look-up table]

1/1023 . . . . [Offset correction (H03M 1/1019 takes precedence; removal of offset already present on the analogue input signal H03M 1/1295)]

1/1028 . . . . [at two points of the transfer characteristic, i.e. by adjusting two reference values, e.g. offset and gain error (gain setting for range control H03M 1/18)]

1/1033 . . . . [over the full range of the converter, e.g. for correcting differential non-linearity]

1/1038 . . . . [by storing corrected or correction values in one or more digital look-up tables (H03M 1/1057 takes precedence)]

1/1042 . . . . [the look-up table containing corrected values for replacing the original digital values (H03M 1/1052 takes precedence)]

1/1047 . . . . [using an auxiliary digital/analogue converter for adding the correction values to the analogue signal (H03M 1/1052 takes precedence)]

1/1052 . . . . [using two or more look-up tables each corresponding to a different type of error, e.g. for offset, gain error and non-linearity error respectively]

1/1057 . . . . [by trimming, i.e. by individually adjusting at least part of the quantisation value generators or stages to their nominal values]

1/1061 . . . . [using digitally programmable trimming circuits]

1/1066 . . . . [Mechanical or optical alignment]

1/1071 . . . . [Measuring or testing]

1/1076 . . . . [Detection or location of converter hardware failure, e.g. power supply failure, open or short circuit]

1/108 . . . . [Converters having special provisions for facilitating access for testing purposes]

1/1085 . . . . [using domain transforms, e.g. Fast Fourier Transform]

1/109 . . . . [for dc performance, i.e. static testing (H03M 1/1085 takes precedence)]

1/1095 . . . . [for ac performance, i.e. dynamic testing (H03M 1/1085 takes precedence)]

1/12 . . . . [Analogue/digital converters ((H03M 1/001 – ) H03M 1/10 take precedence)]

1/1205 . . . . [Multiplexed conversion systems]

1/121 . . . . [Interleaved, i.e. using multiple converters or converter parts for one channel]
 delivering more than one bit the same or a different conversion means and
specially adapted for A/D converters }

Sampling or signal conditioning arrangements
for in subgroups of H03M 1/12
(H03M 1/141
with scale factor modification, i.e. by
takes precedence )

H03M 1/143
in a single stage, i.e. recirculation type
( H03M 1/141
in a single stage, i.e. recirculation type
the steps being performed sequentially
the steps being performed sequentially in
series-connected stages (H03M 1/161 takes precedence))

{ Details of sampling arrangements or methods }

Asynchronous, i.e. free-running operation
within each conversion cycle

{ Constructional details of parts relevant
to the encoding mechanism, e.g. pattern
carriers, pattern sensors }

Automatic control for modifying the range of
signals the converter can handle, e.g. gain ranging

{ in feedback mode, i.e. by determining the
range to be selected from one or more previous
digital output values }

{ the feedback signal controlling the
reference levels of the analogue/digital
converter }

{ the feedback signal controlling the gain
of an amplifier or attenuator preceding the
analogue/digital converter }

Detailed of the range being
based on more than one digital output
value, e.g. on a running average, a power
estimation or the rate of change

{ in feedforward mode, i.e. by determining the
range to be selected directly from the input
signal }

{ using an auxiliary analogue/digital
converter }

{ Multi-path, i.e. having a separate analogue/
digital converter for each possible range }

Increasing resolution using an n bit system to
obtain n + m bits

{ by dithering }

{ by interpolation }

{ using an analogue interpolation circuit }

{ in which one or more virtual intermediate
reference signals are generated between
adjacent original reference signals, e.g.
by connecting pre-amplifier outputs to
multiple comparators }

{ using resistor strings for redistribution
of the original reference signals or
signals derived therefrom }

{ using a logic interpolation circuit }

{ using a digital interpolation circuit }

{ by prediction }

{ pattern-reading type }

{ using relatively movable reader and disc or
strip }

{ Constructional details of parts relevant
to the encoding mechanism, e.g. pattern
carriers, pattern sensors }

with weighted coding, i.e. the weight given
to a digit depends on the position of the digit
within the block or code word, e.g. there is
a given radix and the weights are powers of
this radix

{ with non-weighted coding }

{ of the pattern-shifting type, e.g. pseudo-
random chain code }
Analogue value compared with reference values takes precedence

for direct conversion to a residue number

having slightly different pitches, e.g. of the Vernier or nonius type

analogue value compared with reference values

by current sources rather than by voltage

in which the information is represented using current sources, e.g. of the binary weighted type

the stages being of the folding type

using switched capacitors

the stages being of the folding type

using current sources as quantisation value

using tapped delay lines

for position encoding, e.g. using resolvers or synchros

for position encoding, e.g. using resolvers or synchros

for waveshaping

using current mode circuits, i.e. circuits in which the information is represented by current values rather than by voltage values

using current mode circuits, i.e. circuits in which the information is represented by current values rather than by voltage values

Servo-type converters

by interpolation, by curve-fitting, by smoothing

Digital/analogue converters (H03M 1/001 –

Improving the reconstruction of the analogue output signal beyond the resolution of the digital input signal, e.g. by interpolation, by curve-fitting, by smoothing

Multiplexed conversion systems

Non-linear conversion not otherwise provided for in subgroups of H03M 1/66

with intermediate conversion to phase of sinusoidal or similar periodical signals

using switched capacitors

Non-linear conversion

for intermediate conversion to frequency of pulses

for intermediate conversion to phase of sinusoidal or similar periodical signals

Servo-type converters

multiplexing conversion systems

with intermediate conversion to phase of sinusoidal or similar periodical signals

Servo-type converters

using switched capacitors

using current mode circuits, i.e. circuits in which the information is represented by current values rather than by voltage values

using current mode circuits, i.e. circuits in which the information is represented by current values rather than by voltage values

Servo-type converters

using switched capacitors

Servo-type converters

using current sources as quantisation value generators

Automatic control for modifying converter range

having slightly different pitches, e.g. of the Vernier or nonius type

having slightly different pitches, e.g. of the Vernier or nonius type

using switched capacitors

using switched capacitors

using switched capacitors

using switched capacitors

using switched capacitors

using switched capacitors

using switched capacitors
differential modulation
Conversion of analogue values to or from
3/00

3/02
3/022
3/024
3/04
3/042
3/30

Delta modulation, i.e. one-bit differential
modulation (H03M 3/30 takes precedence)
[with adaptable step size, e.g. adaptive delta
modulation [ADM]]
[using syllabic companding, e.g. continuously
variable slope delta modulation [CVSD]]
Differential modulation with several bits (e.g. differential
code format [ADC], (H03M 3/30 takes precedence)]
[with adaptable step size, e.g. adaptive
differential pulse code modulation [ADPCM]]
[Delta-sigma modulation]

NOTE

[In group branch H03M 3/30, in the absence of
an indication to the contrary, classification is
made in the first appropriate place.]

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[with special provisions or arrangements for
power saving, e.g. by allowing a sleep mode,
using lower supply voltage for downstream
stages, using multiple clock domains, by
selectively turning on stages when needed]
[Continuously compensating for, or preventing,
undesired influence of physical parameters
(periodically, e.g. by using stored correction
values, H03M 3/278)]
[characterised by means or methods for
compensating or preventing more than one type
of error at a time, e.g. by synchronisation or
using a ratiometric arrangement]
[by averaging out the errors]
[using dither]
[the dither being in the time domain]

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[the dither being at least partially
dependent on the input signal]
[the dither being a random signal]
[in particular a pseudo-random
signal]
(by permutation in the time domain, e.g.
dynamic element matching (in multiple bit
sub-converters H03M 1/066)]
(by chopping)
(by double sampling, e.g. correlated
double sampling)
(by filtering other than the noise-shaping
inherent to delta-sigma modulators, e.g. anti-
alising)
(by suppressing active signals at
predetermined times, e.g. muting, using non-
overlapping clock phases)
(by using return-to-zero signals)
(by using redundancy)
[at deviations from the desired transfer
characteristic]
[at one point, i.e. by adjusting a single
reference value, e.g. bias or gain error]
[Offset or drift compensation (removal
of offset already present on the analogue
input signal H03M 3/494)]
[of non-linear distortion, e.g. instability
(avoiding instability by structural design
H03M 3/44)]
[by temporarily adapting the operation upon
detection of instability conditions]
[in feedback mode, e.g. by reducing the
order of the modulator]
(by resetting one or more loop filter
stages)
[in feed-forward mode, e.g. using look-
ahead circuits]
[of noise other than the quantisation noise
already being shaped inherently by delta-sigma
modulators]
[Compensation or reduction of delay or
phase error]
[Jitter reduction]
[Relaxation of settling time constraints,
e.g. slew rate enhancement]
[Prevention or reduction of switching
transients, e.g. glitches]
[Testing]
[Calibration]
[at one point of the transfer characteristic, i.e.
by adjusting a single reference value, e.g. bias
or gain error]
[Offset correction (removal of offset
already present on the analogue input signal
H03M 3/494)]
[over the full range of the converter, e.g. for
correcting differential non-linearity]
[by storing corrected or correction values in
one or more digital look-up tables]
[Structural details of delta-sigma modulators, e.g.
incremental delta-sigma modulators (of digital
delta-sigma modulators H03M 7/3004)]
3/392 . . . . . [Arrangements for selecting among plural operation modes, e.g. for multi-standard operation]
3/394 . . . . . [among different orders of the loop filter]
3/396 . . . . . [among different frequency bands]
3/398 . . . . . [among different converter types]
3/40 . . . . . [Arrangements for handling converter signals, e.g. complex modulators]
3/402 . . . . . [Arrangements specific to bandpass modulators]
3/404 . . . . . [characterised by the type of bandpass filters used]
3/406 . . . . . [by the use of a pair of integrators forming a closed loop]
3/408 . . . . . [by the use of an LC circuit]
3/41 . . . . . [combined with modulation or demodulation from the carrier]
3/412 . . . . . [characterised by the number of quantisers and their type and resolution]
3/414 . . . . . [having multiple quantisers arranged in cascadable loops, each of the second and further loops processing the quantisation error of the loop preceding it, e.g. multiple stage noise shaping [MASH] type]
3/416 . . . . . [all these quantisers being multiple bit quantisers]
3/418 . . . . . [all these quantisers being single bit quantisers]
3/42 . . . . . [having multiple quantisers arranged in parallel loops]
3/422 . . . . . [having one quantiser only]
3/424 . . . . . [the quantiser being a multiple bit one]
3/426 . . . . . [the quantiser being a successive approximation type analogue/digital converter]
3/428 . . . . . [with lower resolution, e.g. single bit, feedback]
3/43 . . . . . [the quantiser being a single bit one]
3/432 . . . . . [the quantiser being a pulse width modulation type analogue/digital converter, i.e. differential pulse width modulation]
3/434 . . . . . [with multi-level feedback]
3/436 . . . . . [characterised by the order of the loop filter, e.g. error feedback type]

**NOTE**
In this group branch the order of the loop filters is considered to be the number of integrators for a baseband modulator and the number of resonators for a bandpass modulator respectively.

3/438 . . . . . [the modulator having a higher order loop filter in the feedforward path]
3/44 . . . . . [with provisions for rendering the modulator inherently stable]

**NOTE**
In this subgroup, classification is made both here and in H03M 3/478 if both subgroups are relevant.

3/442 . . . . . [by restricting the swing within the loop, e.g. gain scaling]
3/444 . . . . . [using non-linear elements, e.g. limiters]
3/446 . . . . . [by a particular choice of poles or zeroes in the z-plane, e.g. by positioning zeroes outside the unit circle, i.e. causing the modulator to operate in a chaotic regime]
3/448 . . . . . [by removing part of the zeroes, e.g. using local feedback loops]
3/45 . . . . . [with distributed feedback inputs, i.e. with forward paths from the modulator input to more than one filter stage]
3/452 . . . . . [with weighted feedback summation, i.e. with feedforward paths from more than one filter stage to the quantiser input]
3/454 . . . . . [with distributed feedback, i.e. with feedback paths from the quantiser output to more than one filter stage]
3/456 . . . . . [the modulator having a first order loop filter in the feedback path]
3/458 . . . . . [Analogue/digital converters using delta-sigma modulation as an intermediate step]
3/46 . . . . . [using a combination of at least one delta-sigma modulator in series with at least one analogue/digital converter of a different type]
3/462 . . . . . [Details relating to the decimation process (decimation filters in general H03H 17/0416, H03H 17/0621)]
3/464 . . . . . [Details of the digital/analogue conversion in the feedback path]
3/466 . . . . . [Multiplexed conversion systems]
3/468 . . . . . [Interleaved, i.e. using multiple converters or converter parts for one channel, e.g. using Hadamard codes, pi-delta-sigma converters]
3/47 . . . . . [using time-division multiplexing]
3/472 . . . . . [Shared, i.e. using a single converter for multiple channels]
3/474 . . . . . [using time-division multiplexing]
3/476 . . . . . [Non-linear conversion systems]
3/478 . . . . . [Means for controlling the correspondence between the range of the input signal and the range of signals the converter can handle; Means for out-of-range indication]

**NOTE**
In this subgroup, classification is made both here and in H03M 3/44 if both subgroups are relevant.

3/48 . . . . . [characterised by the type of range control, e.g. limiting]
3/482 . . . . . [by adapting the quantisation step size]
3/484 . . . . . [by adapting the gain of the feedback signal, e.g. by adapting the reference values of the digital/analogue converter in the feedback path]
3/486 . . . . . [by adapting the input gain]
3/488 . . . . . [using automatic control]
3/49 . . . . . [in feedback mode, i.e. by determining the range to be selected from one or more previous digital output values]
3/492 . . . . . [in feed forward mode, i.e. by determining the range to be selected directly from the input signal]
In groups H03M 5/02 – H03M 5/22, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

3. In this main group, in the absence of an indication to the contrary, additional information has been classified systematically for documents published from 01-04-2004 onwards.}

1. In groups H03M 7/001 - H03M 7/50, the last place priority rule is applied, i.e. at each hierarchical level, in the absence of an indication to the contrary, classification is made in the last appropriate place.

2. In groups H03M 7/02 – H03M 7/50, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

3. In this main group, in the absence of an indication to the contrary, additional information has been classified systematically for documents published from 01-04-2004 onwards.}

Conversion of the form of the representation of individual digits

1. In groups H03M 5/02 - H03M 5/22, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

2. In this main group, additional information has been classified systematically for documents published from 01-04-2004 onwards.]

Conversion of a code where information is represented by a given sequence or number of digits to a code where the same information is represented by a different sequence or number of digits

1. In groups H03M 7/001 - H03M 7/50, the last place priority rule is applied, i.e. at each hierarchical level, in the absence of an indication to the
7/3017 . . . . . {Arrangements specific to bandpass modulators}
7/302 . . . . . (characterised by the number of quantisers and their type and resolution)
7/3022 . . . . . {having multiple quantisers arranged in cascaded loops, each of the second and further loops processing the quantisation error of the loop preceding it, i.e. multiple stage noise shaping [MASH] type}
7/3024 . . . . . {having one quantiser only}
7/3026 . . . . . {the quantiser being a multiple bit one}
7/3028 . . . . . {the quantiser being a single bit one}
7/3031 . . . . . {characterised by the order of the loop filter, e.g. having a first order loop filter in the feedforward path}

**NOTE**

In this group the order of the loop filters is considered to be the number of integrators for a baseband modulator and the number of resonators for a bandpass modulator respectively.

7/3033 . . . . . {the modulator having a higher order loop filter in the feedforward path, e.g. with distributed feedforward inputs}
7/3035 . . . . . {with provisions for rendering the modulator inherently stable, e.g. by restricting the swing within the loop, by removing part of the zeroes using local feedback loops, by positioning zeroes outside the unit circle causing the modulator to operate in a chaotic regime}
7/3037 . . . . . {with weighted feedforward summation, i.e. with feedforward paths from more than one filter stage to the quantiser input}
7/304 . . . . . {with distributed feedback, i.e. with feedback paths from the quantiser output to more than one filter stage}
7/3042 . . . . . {the modulator being of the error feedback type, i.e. having loop filter stages in the feedback path only}
7/3044 . . . {Conversion to or from differential modulation with several bits only, i.e. the difference between successive samples being coded by more than one bit, e.g. differential pulse code modulation [DPCM] (H03M 7/3004 takes precedence; voice coding G10L 19/00; image coding H04N 19/00)}
7/3046 . . . . . {adaptive, e.g. adaptive differential pulse code modulation [ADPCM]}
7/3048 . . . {Conversion to or from one-bit differential modulation only, e.g. delta modulation [DM] (H03M 7/3004 takes precedence)}
7/3051 . . . . . {adaptive, e.g. adaptive delta modulation [ADM]}
7/3053 . . . {Block-compounding PCM systems}
7/3055 . . . {Conversion to or from Modulo-PCM}
7/3057 . . . {Distributed Source coding, e.g. Wyner-Ziv, Slepian Wolf}
7/3059 . . . {Digital compression and data reduction techniques where the original information is represented by a subset or similar information, e.g. lossy compression}
7/3062 . . . {Compressive sampling or sensing}
7/3064 . . . {Segmenting}
7/3066 . . . {by means of a mask or a bit-map}
7/3068 . . . {Precoding preceding compression, e.g. Burrows-Wheeler transformation}
7/3071 . . . . . {Prediction}
7/3073 . . . . . {Time}
7/3075 . . . . . {Space}
7/3077 . . . . . {Sorting}
7/3079 . . . . . {Context modeling}
7/3082 . . . {Vector coding (for television signals, see H04N 19/94)}
7/3084 . . . {using adaptive string matching, e.g. the Lempel-Ziv method}
7/3086 . . . (employing a sliding window, e.g. LZ77)
7/3088 . . . {employing the use of a dictionary, e.g. LZ78}
7/3091 . . . {Data deduplication}
7/3093 . . . {using fixed length segments}
7/3095 . . . {using variable length segments}
7/3097 . . . {Grammar codes}
7/40 . . . Conversion to or from variable length codes, e.g. Shannon-Fano code, Huffman code, Morse code
7/4006 . . . {Conversion to or from arithmetic code}
7/4012 . . . {Binary arithmetic codes}
7/4018 . . . {Context adaptive binary arithmetic codes [CABAC]}
7/4025 . . . {constant length to or from Morse code conversion}
7/4031 . . . {Fixed length to variable length coding}
7/4037 . . . {Prefix coding}
7/4043 . . . . . {Adaptive prefix coding}
7/4045 . . . . . {Tree adaptation}
7/4056 . . . . . {Coding table selection}
7/4062 . . . . . {Coding table adaptation}
7/4068 . . . . . {Parameterized codes}
7/4075 . . . . . . {Golomb codes}
7/4081 . . . {Static prefix coding}
7/4087 . . . . . {Encoding of a tuple of symbols}
7/4093 . . . {Variable length to variable length coding}
7/42 . . . using table look-up for the coding or decoding process, e.g. using read-only memory (H03M 7/4006 takes precedence)
7/425 . . . {for the decoding process only}
7/46 . . . Conversion to or from run-length codes, i.e. by representing the number of consecutive digits, or groups of digits, of the same kind by a code word and a digit indicative of that kind
7/48 . . . alternation with other codes during the code conversion process, e.g. run-length coding being performed only as long as sufficiently long runs of digits of the same kind are present
7/50 . . . Conversion to or from non-linear codes, e.g. companding
7/55 . . . {Compression Theory, e.g. compression of random number, repeated compression}
7/60 . . . {General implementation details not specific to a particular type of compression}
7/6005 . . . {Decoder aspects}
11/00 Coding in connection with keyboards or like devices, i.e. coding of the position of operated keys (keyboard switch arrangements, structural association of coders and keyboards \textit{H01H 13/70, H03K 17/94})

**NOTE**

{In this main group additional information has been classified systematically for documents published from 01-01-2013 onwards.}

11/000 . . . . [Encoders aspects]
11/002 . . . . Details
11/004 . . . . Coding of multifunction keys
11/006 . . . . by operating the multifunction key itself in different ways
11/008 . . . . by operating selected combinations of multifunction keys
11/10 . . . . by methods based on duration or pressure detection of keystrokes
11/12 . . . . by operating a key a selected number of consecutive times whereafter a separate enter key is used which marks the end of the series
11/14 . . . . by using additional keys, e.g. shift keys, which determine the function performed by the multifunction key
11/16 . . . . wherein the shift keys are operated after the operation of the multifunction keys
11/18 . . . . wherein the shift keys are operated before the operation of the multifunction keys
11/20 . . . . Dynamic coding, i.e. by key scanning (\textit{H03M 11/26 takes precedence})
11/22 . . . . Static coding (\textit{H03M 11/26 takes precedence})

11/24 . . . . using analogue means, e.g. by coding the states of multiple switches into a single multi-level analogue signal or by indicating the type of a device using the voltage level at a specific tap of a resistive divider)
11/26 . . . . using opto-electronic means

13/00 Coding, decoding or code conversion, for error detection or error correction; Coding theory basic assumptions; Coding bounds; Error probability evaluation methods; Channel models; Simulation or testing of codes (error detection or error correction for analogue/digital, digital/analogue or code conversion \textit{H03M 1/00 – H03M 11/00} specially adapted for digital computers \textit{G06F 11/08}, for information storage based on relative movement between record carrier and transducer \textit{G11B}, e.g. \textit{G11B 20/18}, for static stores \textit{G11C})

13/01 . . . . Coding theory basic assumptions; Coding bounds; Error probability evaluation methods; Channel models; Simulation or testing of codes
13/015 . . . . (Simulation or testing of codes, e.g. bit error rate \textit{[BER]} measurements)
13/03 . . . . Error detection or forward error correction by redundancy in data representation, i.e. code words containing more digits than the source words
13/033 . . . . (Theoretical methods to calculate these checking codes)
13/036 . . . . (Heuristic code construction methods, i.e. code construction or code search based on using trial-and-error)
13/05 . . . . using block codes, i.e. a predetermined number of check bits joined to a predetermined number of information bits ((\textit{H03M 13/29}06 takes precedence))
13/07 . . . . Arithmetic codes
13/09 . . . . Error detection only, e.g. using cyclic redundancy check [CRC] codes or single parity bit
13/091 . . . . [Parallel or block-wise CRC computation]
13/093 . . . . [CRC update after modification of the information word]
13/095 . . . . [Error detection codes other than CRC and single parity bit codes]
13/096 . . . . [Checksums]
13/098 . . . . [using single parity bit]
13/11 . . . . using multiple parity bits
13/1102 . . . . [Codes on graphs and decoding on graphs, e.g. low-density parity check [LDPC] codes]
13/1105 . . . . (Decoding)
13/1108 . . . . [Hard decision decoding, e.g. bit flipping, modified or weighted bit flipping]
13/1111 . . . . [Soft-decision decoding, e.g. by means of message passing or belief propagation algorithms]
13/1114 . . . . [Merged schedule message passing algorithm with storage of sums of check-to-bits node messages or sums of bit-to-check node messages, e.g. in order to increase the memory efficiency]
13/117 . . . . . [using approximations for check node processing, e.g. an outgoing message is depending on the signs and the minimum over the magnitudes of all incoming messages according to the min-sum rule]
13/112 . . . . . . [with correction functions for the min-sum rule, e.g. using an offset or a scaling factor]
13/1122 . . . . . . [storing only the first and second minimum values per check node]
13/1125 . . . . . . [using different domains for check node and bit node processing, wherein the different domains include probabilities, likelihood ratios, likelihood differences, log-likelihood ratios or log-likelihood difference pairs]
13/1128 . . . . . . [Judging correct decoding and iterative stopping criteria other than syndrome check and upper limit for decoding iterations]
13/1131 . . . . . . [Scheduling of bit node or check node processing]
13/1134 . . . . . . [Full parallel processing, i.e. all bit nodes or check nodes are processed in parallel]
13/1137 . . . . . . [Partly parallel processing, i.e. sub-blocks or sub-groups of nodes being processed in parallel]
13/114 . . . . . . [Shuffled, staggered, layered or turbo decoding schedules]
13/1142 . . . . . [using trapping sets]
13/1145 . . . . . . [Pipelined decoding at code word level, e.g. multiple code words being decoded simultaneously]
13/1148 . . . . . . [Structural properties of the code parity-check or generator matrix]
13/1151 . . . . . . [Algebraically constructed LDPC codes, e.g. LDPC codes derived from Euclidean geometries [EG-LDPC codes] (H03M 13/116, H03M 13/1174 take precedence)]
13/1154 . . . . . . [Low-density parity-check convolutional codes [LDPC-CC]]
13/1157 . . . . . . [Low-density generator matrices [LDGM]]
13/116 . . . . . . [Quasi-cyclic LDPC (QC-LDPC) codes, i.e. the parity-check matrix being composed of permutation or circulant sub-matrices]
13/1162 . . . . . . [Array based LDPC codes, e.g. array codes]
13/1165 . . . . . . [QC-LDPC codes as defined for the digital video broadcasting [DVB] specifications, e.g. DVB-Satellite [DVB-S2]]
13/1168 . . . . . . [wherein the sub-matrices have column and row weights greater than one, e.g. multi-diagonal sub-matrices]
13/1171 . . . . . . [Parity-check or generator matrices with non-binary elements, e.g. for non-binary LDPC codes]
13/1174 . . . . . . [Parity-check or generator matrices built from sub-matrices representing known block codes such as, e.g. Hamming codes, e.g. generalized LDPC codes]
13/1177 . . . . . . [Regular LDPC codes with parity-check matrices wherein all rows and columns have the same row weight and column weight, respectively]
13/118 . . . . . . [Parity check matrix structured for simplifying encoding, e.g. by having a triangular or an approximate triangular structure (H03M 13/1165 takes precedence)]
13/1182 . . . . . . [wherein the structure of the parity-check matrix is obtained by reordering of a random parity-check matrix]
13/1185 . . . . . . [wherein the parity-check matrix comprises a part with a double-diagonal]
13/1188 . . . . . . [wherein in the part with the double-diagonal at least one column has an odd column weight equal or greater than three]
13/1191 . . . . . . [Codes on graphs other than LDPC codes]
13/1194 . . . . . . [Repeat-accumulate [RA] codes]
13/1197 . . . . . . [Irregular repeat-accumulate [IRA] codes]
13/13 . . . . . . . . Linear codes
13/132 . . . . . . [Algebraic geometric codes, e.g. Goppa codes]
13/134 . . . . . . [Non-binary linear block codes not provided for otherwise]
13/136 . . . . . . [Reed-Muller [RM] codes]
13/138 . . . . . . [Codes linear in a ring, e.g. Z4-linear codes or Nordstrom-Robinson codes]
13/15 . . . . . . . . Cyclic codes, i.e. cyclic shifts of codewords produce other codewords, e.g. codes defined by a generator polynomial, Bose-Chaudhuri-Hocquenghem [BCH] codes (H03M 13/17 takes precedence)]
13/1505 . . . . . [Golay Codes]
13/151 . . . . . . [using error location or error correction polynomials]
13/1515 . . . . . [Reed-Solomon codes]
13/152 . . . . . . [Bose-Chaudhuri-Hocquenghem [BCH] codes]
13/1525 . . . . . [Determination and particular use of error location polynomials]
13/153 . . . . . . [using the Berlekamp-Massey algorithm]
13/1535 . . . . . [using the Euclid algorithm]
13/154 . . . . . . [Error and erasure correction, e.g. by using the error and erasure locator or Forney polynomial]
13/1545 . . . . . [Determination of error locations, e.g. Chien search or other methods or arrangements for the determination of the roots of the error locator polynomial]
13/155 . . . . . . [Shortening or extension of codes]
13/1555 . . . . . [Pipelined decoder implementations]
using interleaving techniques

13/2703 . . . (the interleaver involving at least two directions)
13/2707 . . . [Simple row-column interleaver, i.e. pure block interleaving]
13/271 . . . [Row-column interleaver with permutations, e.g. block interleaving with inter-row, inter-column, intra-row or intra-column permutations]
13/2714 . . . [Turbo interleaver for 3rd generation partnership project [3GPP] universal mobile telecommunications systems [UMTS], e.g. as defined in technical specification TS 25.212]
13/2717 . . . (the interleaver involves 3 or more directions)
13/2721 . . . (the interleaver involves a diagonal direction, e.g. by using an interleaving matrix with read-out in a diagonal direction)
NOTE
This group covers also aspects when a component code is replaced by a non-coded constraint, e.g. like in joint turbo decoding and detection

13/2966 . . . . {Particular turbo code structure}

NOTE
this group covers hybrid parallel and serial concatenated turbo code structures and other unusual code structures that do not fit into
H03M 13/2963 - H03M 13/2972

13/2963 . . . . {Turbo-block codes, i.e. turbo codes based on block codes, e.g. turbo decoding of product codes}
13/2966 . . . . {Turbo codes concatenated with another code, e.g. an outer block code}
13/2969 . . . . {Non-binary turbo codes}
13/2972 . . . . {Serial concatenation using convolutional component codes}
13/2975 . . . . {Judging correct decoding, e.g. iteration stopping criteria}
13/2978 . . . . {Particular arrangement of the component decoders}
13/2981 . . . . {using as many component decoders as component codes}
13/2984 . . . . {using less component decoders than component codes, e.g. multiplexed decoders and scheduling thereof}

13/2972 . . . . {using at least three error correction codes
(H03M 13/2957 takes precedence)}
13/2945 . . . . {using a block and a convolutional code
(H03M 13/2957 takes precedence)}
13/2942 . . . . {wherein a block of parity bits is computed
only from combined information bits or only from parity bits, e.g. a second block of parity bits is computed from a first block of parity bits obtained by systematic encoding of a block of information bits, or a block of parity bits is obtained by an XOR combination of sub-blocks of information bits}
13/2948 . . . . {iterative decoding
(H03M 13/2957 takes precedence)}
13/2951 . . . . {using iteration stopping criteria}
13/2954 . . . . {using Picket codes or other codes providing error burst detection capabilities, e.g. burst indicator codes and long distance codes [LDC]}
13/3905 . . . {Maximum a posteriori probability [MAP] decoding or approximations thereof based on trellis or lattice decoding, e.g. forward-backward algorithm, log-MAP decoding, max-log-MAP decoding}

**WARNING**

Group H03M 13/3905 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3905 should be considered in order to perform a complete search.

13/3911 . . . . {Correction factor, e.g. approximations of the exp(1+x) function}

**WARNING**

Group H03M 13/3911 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3911 should be considered in order to perform a complete search.

13/3916 . . . . {for block codes using a trellis or lattice}

**WARNING**

Group H03M 13/3916 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3916 should be considered in order to perform a complete search.

13/3922 . . . . {Add-Compare-Select [ACS] operation in forward or backward recursions}

**WARNING**

Group H03M 13/3922 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3922 should be considered in order to perform a complete search.

13/3927 . . . . {Log-Likelihood Ratio [LLR] computation by combination of forward and backward metrics into LLRs}

**WARNING**

Group H03M 13/3927 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3927 should be considered in order to perform a complete search.

13/3933 . . . . {Decoding in probability domain}

**WARNING**

Group H03M 13/3933 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3933 should be considered in order to perform a complete search.

13/3938 . . . . {Tail-biting [H03M 13/2996 takes precedence]}

**WARNING**

Group H03M 13/3938 is incomplete pending reclassification of documents from group H03M 13/42.

Groups H03M 13/42 and H03M 13/3938 should be considered in order to perform a complete search.

13/3944 . . . . {for block codes, especially trellis or lattice decoding thereof}

13/395 . . . . {using a collapsed trellis, e.g. M-step algorithm, radix-n architectures with n>2}

13/3955 . . . . {using a trellis with a reduced state space complexity, e.g. M-algorithm or T-algorithm}

13/3961 . . . . {Arrangements of methods for branch or transition metric calculation}

13/3966 . . . . {based on architectures providing a highly parallelized implementation, e.g. based on systolic arrays}

13/3972 . . . . {using sliding window techniques or parallel windows}

13/3977 . . . . {using sequential decoding, e.g. the Fano or stack algorithms}

13/3983 . . . . {for non-binary convolutional codes}

13/3988 . . . . {for rate k/n convolutional codes, with k>1, obtained by convolutional encoders with k inputs and n outputs}

13/3994 . . . . {using state pinning or decision forcing, i.e. the decoded sequence is forced through a particular trellis state or a particular set of trellis states or a particular decoded symbol}

13/41 . . . . {using the Viterbi algorithm or Viterbi processors}

13/4107 . . . . {implementing add, compare, select [ACS] operations}

13/4115 . . . . {list output Viterbi decoding}

13/4123 . . . . {implementing the return to a predetermined state}

13/413 . . . . {tail-biting Viterbi decoding}

13/4138 . . . . {soft-output Viterbi algorithm based decoding, i.e. Viterbi decoding with weighted decisions}

13/4146 . . . . {soft-output Viterbi decoding according to Battail and Hagenauer in which the soft-output is determined using path metric differences along the maximum-likelihood path, i.e. "SOVA" decoding}

13/4153 . . . . {two-step SOVA decoding, i.e. the soft-output is determined by a second traceback operation after the determination of the hard decision like in the Berrou decoder}
H03M

13/4161 . . . . . . [implementing path management]
13/4169 . . . . . . (using traceback (H03M 13/4192 takes precedence)
13/4176 . . . . . . {using a plurality of RAMs, e.g. for carrying out a plurality of traceback implementations simultaneously)
13/4184 . . . . . . (using register-exchange (H03M 13/4192 takes precedence)
13/4192 . . . . . . (using combined traceback and register-exchange
13/42 . . . . . . (Frozen) [MAP decoding or approximations thereof based on trellis or lattice decoding, e.g. forward-backward algorithm, log-MAP decoding, max-log-MAP decoding)

WARNING

Group H03M 13/42 is no longer used for the classification of documents as of MAY 1, 2019.

The content of this group is being reclassified into groups H03M 13/3905, H03M 13/3911, H03M 13/3916, H03M 13/3922, H03M 13/3927, H03M 13/3933 and H03M 13/3938

All groups listed in this Warning should be considered in order to perform a complete search.

13/43 . . . Majority logic or threshold decoding
13/45 . . . Soft decoding, i.e. using symbol reliability information (H03M 13/41 takes precedence)
13/451 . . . . . . [using a set of candidate code words, e.g. ordered statistics decoding [OSD]
13/453 . . . . . . { wherein the candidate code words are obtained by an algebraic decoder, e.g. Chase decoding
13/455 . . . . . . { using a set of erasure patterns or successive erasure decoding, e.g. generalized minimum distance [GMD] decoding
13/456 . . . . . . { wherein all the code words of the code or its dual code are tested, e.g. brute force decoding
13/458 . . . . . . [by updating bit probabilities or hard decisions in an iterative fashion for convergence to a final decoding result]
13/47 . . . Error detection, forward error correction or error protection, not provided for in groups H03M 13/01 - H03M 13/37
13/49 . . . Unidirectional error detection or correction
13/51 . . . Constant weight codes; n-out-of-m codes; Berger codes
13/53 . . . Codes using Fibonacci numbers series
13/61 . . . . . . { Aspects and characteristics of methods and arrangements for error correction or error detection, not provided for otherwise}
13/611 . . . . . . { Specific encoding aspects, e.g. encoding by means of decoding}
13/612 . . . . . . { Aspects specific to channel or signal-to-noise ratio estimation (H03M 13/63 takes precedence)
13/613 . . . . . . { Use of the dual code
13/615 . . . . . . { Use of computational or mathematical techniques

13/616 . . . . . . { Matrix operations, especially for generator matrices or check matrices, e.g. column or row permutations
13/617 . . . . . . { Polynomial operations, e.g. operations related to generator polynomials or parity-check polynomials
13/618 . . . . . . { Shortening and extension of codes
13/63 . . . . . . { Joint error correction and other techniques (H03M 13/31 and H03M 13/33 take precedence)
13/6306 . . . . . . { Error control coding in combination with Automatic Repeat reQuest [ARQ] and diversity transmission, e.g. coding schemes for the multiple transmission of the same information or the transmission of incremental redundancy (H03M 13/3761, H03M 13/3769 and H03M 13/635 take precedence)
13/6312 . . . . . . { Error control coding in combination with data compression
13/6318 . . . . . . { using variable length codes
13/6325 . . . . . . { Error control coding in combination with demodulation
13/6331 . . . . . . { Error control coding in combination with equalisation
13/6337 . . . . . . { Error control coding in combination with channel estimation
13/6343 . . . . . . { Error control coding in combination with techniques for partial response channels, e.g. recording
13/635 . . . . . . { Error control coding in combination with rate matching
13/6356 . . . . . . { by repetition or insertion of dummy data, i.e. rate reduction
13/6362 . . . . . . { by puncturing
13/6368 . . . . . . { using rate compatible puncturing or complementary puncturing
13/6375 . . . . . . { Rate compatible punctured convolutional [RCPC] codes
13/6381 . . . . . . { Rate compatible punctured turbo [RCPT] codes
13/6387 . . . . . . { Complementary punctured convolutional [CPC] codes
13/6393 . . . . . . { Rate compatible low-density parity check [LDPC] codes
13/665 . . . . . . { Purpose and implementation aspects
13/6502 . . . . . . { Reduction of hardware complexity or efficient processing
13/6505 . . . . . . { Memory efficient implementations
13/6508 . . . . . . { Flexibility, adaptability, parametrability and configurability of the implementation
13/6511 . . . . . . { Support of multiple decoding rules, e.g. combined MAP and Viterbi decoding
13/6513 . . . . . . { Support of multiple code types, e.g. unified decoder for LDPC and turbo codes
13/6516 . . . . . . { Support of multiple code parameters, e.g. generalized Reed-Solomon decoder for a variety of generator polynomials or Galois fields
13/6519 . . . . . . { Support of multiple transmission or communication standards
13/6522 . . . . . . { Intended application, e.g. transmission or communication standard
13/6525 . . . . . . { 3GPP LTE including E-UTRA
13/6527 . . . . . . { [IEEE 802.11 [WLAN]

CPC - 2020.08  14
13/653 . . . {3GPP HSDPA, e.g. HS-SCCH or DS-DSCH related}
13/6533 . . . {ITU 992.X [ADSL]}
13/6536 . . . {GSM GPRS}
13/6538 . . . {ATSC VBS systems}
13/6541 . . . {DVB-H and DVB-M}
13/6544 . . . {IEEE 802.16 (WiMAX and broadband wireless access)}
13/6547 . . . {TCP, UDP, IP and associated protocols, e.g. RTP}
13/655 . . . {UWB OFDM}
13/6552 . . . {DVB-T2}
13/6555 . . . {DVB-C2}
13/6558 . . . {3GPP2}
13/6561 . . {Parallelized implementations}
13/6563 . . {Implementations using multi-port memories}
13/6566 . . {Implementations concerning memory access contentions}
13/6569 . . {Implementation on processors, e.g. DSPs, or software implementations}
13/6572 . . {Implementations using a tree structure, e.g. implementations in which the complexity is reduced by a tree structure from O(n) to O(log(n))}
13/6575 . . {Implementations based on combinatorial logic, e.g. Boolean circuits}
13/6577 . . {Representation or format of variables, register sizes or word-lengths and quantization}
13/658 . . . {Scaling by multiplication or division}
13/6583 . . . {Normalization other than scaling, e.g. by subtraction}
13/6586 . . . . {Modulo/modular normalization, e.g. 2’s complement modulo implementations}
13/6588 . . . . {Compression or short representation of variables}
13/6591 . . . {Truncation, saturation and clamping}
13/6594 . . . {Non-linear quantization}
13/6597 . . . {Implementations using analogue techniques for coding or decoding, e.g. analogue Viterbi decoder}

99/00 Subject matter not provided for in other groups of this subclass