G11C  STATIC STORES  (information storage based on relative movement between record carrier and transducer G11B; semiconductor devices for storage H01L, e.g. H01L 27/108 - H01L 27/11597; pulse technique in general H03K, e.g. electronic switches H03K 17/00)

NOTES
1. This subclass covers devices or arrangements for storage of digital or analogue information in which no relative movement takes place between an information storage element and a transducer; which incorporate a selecting-device for writing-in or reading-out the information into or from the store
2. This subclass does not cover elements not adapted for storage and not provided with such means as referred to in Note (3) below, which elements are classified in the appropriate subclass, e.g. of H01, H03K.
3. In this subclass, the following terms are used with the meaning indicated:
   • “storage element” is an element which can hold at least one item of information and is provided with means for writing-in or reading-out this information;
   • “memory” is a device, including storage elements, which can hold information to be extracted when desired.

WARNINGS
1. The following IPC groups are not in the CPC scheme. The subject matter for these IPC groups is classified in the following CPC groups:
   - G11C 8/02 covered by G11C 8/00, H03K 17/00
   - G11C 11/4193 covered by G11C 11/00
   - G11C 11/4195 covered by G11C 11/00
   - G11C 11/4197 covered by G11C 11/00
2. In this subclass non-limiting references (in the sense of paragraph 39 of the Guide to the IPC) may still be displayed in the scheme.

5/00 Details of stores covered by G11C 11/00
5/005 . {Circuit means for protection against loss of information of semiconductor storage devices (manufacturing semi-conductor by using bombardement with radiation H01L 21/26; error detection, monitoring G06F 11/00) }
5/02 . Disposition of storage elements, e.g. in the form of a matrix array
5/025 . . {Geometric lay-out considerations of storage- and peripheral-blocks in a semiconductor storage device (geometrical lay-out of the components in integrated circuits, H01L 27/0207) }
5/04 . . {Supports for storage elements ; e.g. memory modules ; Mounting or fixing of storage elements on such supports }
5/05 . . . Supporting of cores in matrix
5/06 . Arrangements for interconnecting storage elements electrically, e.g. by wiring
5/063 . . {Voltage and signal distribution in integrated semi-conductor memory access lines, e.g. word-line, bit-line, cross-over resistance, propagation delay }
5/066 . . {Means for reducing external access-lines for a semiconductor memory clip, e.g. by multiplexing at least address and data signals }
5/08 . . for interconnecting magnetic elements, e.g. toroidal cores
5/10 . . for interconnecting capacitors
5/12 . . Apparatus or processes for interconnecting storage elements, e.g. for threading magnetic cores
5/14 . . Power supply arrangements (in general G05F, H02J, H02M), e.g. Power down/chip (de)selection, layout of wiring/power grids, multiple supply levels
5/141 . . {Battery and back-up supplies (back-up supplies per se H02J 9/061) }
5/142 . . {Contactless power supplies, e.g. RF, induction, IR (in general H02J 5/00) }
5/143 . . {Detection of memory cassette insertion/removal; Continuity checks of supply and ground lines (in general G01R 31/50); Detection of supply variations/interruptions/levels (G11C 5/148 takes precedence); Switching between alternative supplies (back-up supplies per se H02J 9/061, G11C 5/141 takes precedence) }
5/144 . . {Detection of predetermined disconnection or reduction of power supply, e.g. power down or power standby }
5/145 . . {Applications of charge pumps (charge pumps per se H02M 3/07); Boosted voltage circuits (for logic circuits or inverting circuits H03K 19/00); Clamp circuits therefor (G11C 5/141 takes precedence) }
7/00 Arrangements for writing information into, or reading information out from, a digital store (G11C 5/00 takes precedence; auxiliary circuits for stores using semiconductor devices G11C 11/4063, G11C 11/413)

7/005 . [with combined beam-and individual cell access]
7/006 . [with means for avoiding parasitic signals]
7/007 . [with means for avoiding disturbances due to temperature effects]
7/008 . Sense amplifiers; Associated circuits, (e.g. timing or triggering circuits) (amplifiers per se H03F, H03K)
7/009 . [Differential amplifiers of non-latching type, e.g. comparators, long-tailed pairs]
7/010 . [Differential amplifiers of latching type]
7/011 . [Single-ended amplifiers]
7/012 . Control thereof
7/013 . Input/output [I/O] data interface arrangements, e.g. I/O data control circuits, I/O data buffers
7/014 . [Interface circuits for daisy chain or ring bus memory arrangements]
7/015 . [Data managing, e.g. manipulating data before writing or reading out, data bus switches or control circuits therefor]
7/016 . [Data masking during input/output]
7/017 . [Data reordering during input/output, e.g. crossbars, layers of multiplexers, shifting or rotating]
7/018 . [Read-write modes for single port memories, i.e. having either a random port or a serial port]
7/019 . [Serial bit line access mode, e.g. using bit line address shift registers, bit line address counters, bit line burst counters]
7/020 . [Page serial bit line access mode, i.e. using an enabled row address stroke pulse with its associated word line address and a sequence of enabled column address stroke pulses each with its associated bit line address]
7/021 . [Extended data output [EDO] mode, i.e. keeping output buffer enabled during an extended period of time]
7/022 . [Static column decode serial bit line access mode, i.e. using an enabled row address stroke pulse with its associated word line address and a sequence of enabled bit line addresses]
7/023 . [using serially addressed read-write data registers (G11C 7/1036 takes precedence)]
7/024 . [using data registers of which only one stage is addressed for sequentially outputting data from a predetermined number of stages, e.g. nibble read-write mode]
7/025 . [using data shift registers]

7/1039 . [using pipelining techniques, i.e. using latches between functional memory parts, e.g. row/column decoders, I/O buffers, sense amplifiers]
7/1040 . [using interleaving techniques, i.e. read-write of one part of the memory while preparing another part]
7/1041 . [Read-write mode select circuits]
7/1042 . [Data bus control circuits, e.g. precharging, presetting, equalising]
7/1043 . [Data output circuits, e.g. read-out amplifiers, data output buffers, data output registers, data output level conversion circuits]
7/1044 . [Optical output buffers]
7/1045 . [Data output buffers, e.g. comprising level conversion circuits, circuits for adapting load]
7/1046 . [Data output latches]
7/1047 . [Control signal output circuits, e.g. status or busy flags, feedback command signals]
7/1048 . [Output synchronization]
7/1049 . [I/O lines read out arrangements (global or local sense amplifiers for bit lines G11C 7/006)]
7/1050 . [for memories with random access ports synchronised on clock signal pulse trains, e.g. synchronous memories, self timed memories]
7/1051 . [for multiport memories each having random access ports and serial ports, e.g. video RAM]
7/1052 . [Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level conversion circuits]
7/1053 . [Optical input buffers]
7/1054 . [Data input buffers, e.g. comprising level conversion circuits, circuits for adapting load]
7/1055 . [Data input latches]
7/1056 . [Control signal input circuits]
7/1057 . [Input synchronization]
7/1058 . [Write circuits, e.g. I/O line write drivers]
7/1059 . [Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, equalising circuits, for bit lines]
7/1060 . [Dummy cell management; Sense reference voltage generators]
7/1062 . [Bit line organisation; Bit line lay-out]
7/1063 . [Memory initialisation circuits, e.g. when powering up or down, memory clear, latent image memory]
7/1064 . [Read-write [R-W] timing or clocking circuits; Read-write [R-W] control signal generators or management]
7/1065 . [Clock generating, synchronizing or distributing circuits within memory device]
7/1066 . [Clock input buffers]
7/1067 . [Timing of memory operations based on dummy memory elements or replica circuits]
7/1068 . [Memory cell safety or protection circuits, e.g. arrangements for preventing inadvertent reading or writing; Status cells; Test cells]

8/00 Arrangements for selecting an address in a digital store (for stores using transistors G11C 11/407, G11C 11/413; {switching or gating circuits for general use H03K 17/001})
G11C

11/00 Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor (G11C 14/00 - G11C 21/00 take precedence)

11/005 [comprising combined but independently operative RAM-ROM, RAM-PROM, RAM-EPROM cells]

NOTE

Group G11C 11/56 takes precedence over groups G11C 11/02 - G11C 11/54

11/02 using magnetic elements (using multibit magnetic storage elements G11C 11/5607; counters with magnetic elements H03K 23/76; pulse generators, static switches, logic circuits with such elements H03K 3/45, H03K 17/80, H03K 19/16; measurement of magnetic variables G01R 33/00))

11/04 using storage elements having cylindrical form, e.g. rod, wire (G11C 11/06085) G11C 11/12, G11C 11/14 take precedence)

11/06 using single-aperture storage elements, e.g. ring core; using multi-aperture plates in which each individual aperture forms a storage element

11/06007 using a single aperture or single magnetic closed circuit

NOTE

Provisionally contains the following details: control write-, read-, address circuitry (pulse generators in general H03K 5/00, H03K 17/00); arrangements for temperature compensation; checking of the correct functioning and repair arrangements (checking methods in general G06F 11/00, G06F 11/28; testing magnetic elements per se G01R 33/00); magnetic properties, choice of materials or the like (materials per se H01F 1/00)

11/06014 using one such element per bit

11/06021 with destructive read-out

11/06028 [Matrixes]

11/06035 ("bit"-organised, e.g. 2 1/2D, 3D or a similar organisation, i.e. bit core selection for writing or reading, by at least two coincident partial currents)

11/06042 ("word"-organised, e.g. 2D organisation or linear selection, i.e. full current selection through all the bit-cores of a word during reading)

11/0605 with non-destructive read-out

11/06057 [Matrixes]

11/06064 ("bit"-organised (2 1/2D, 3D or similar organisation))

11/06071 ("word"-organised (2D organisation or linear selection))

11/06078 using two or more such elements pro bit

11/06085 [Multi-aperture structures or multi-magnetic closed circuits, each aperture storing a "bit", realised by rods, plates, grids, waffle-irons, i.e. magnetic loop for storage, one element per bit, and for non-destructive read-out (contains no documents, see G11C 11/06007, G11C 11/06014, G11C 11/06021, G11C 11/06028)]

11/063 bit organised, such as 2 1/2D, 3D organisation, i.e. for selection of an element by means of at least two coincident partial currents both for reading and for writing (contains no documents; see G11C 11/06035)

11/065 word organised, such as 2D organisation, or linear selection, i.e. for selection of all the elements of a word by means of a single full current for reading (contains no documents; see G11C 11/06042)

11/067 using elements with single aperture or magnetic loop for storage, one element per bit, and for non-destructive read-out (contains no documents, see G11C 11/06005, G11C 11/06071)

11/08 using multi-aperture storage elements, e.g. using transfluxors; using plates incorporating several individual multi-aperture storage elements (G11C 11/10 takes precedence; using multi-aperture plates in which each individual aperture forms a storage element G11C 11/006)

11/10 using multi-axial storage elements

11/12 using tensors; using twistors, i.e. elements in which one axis of magnetisation is twisted

11/14 using thin-film elements

11/15 using multi-magnetic layers (G11C 11/155 takes precedence)

11/155 with cylindrical configuration
using elements in which the storage effect is based on magnetic spin effect \((\text{sensors using magnetoresistive multilayer structures G01R 33/093; thin layer magnetic read heads for magnetic discs G11B 5/31; non-reciprocal magnetic elements in waveguides H01P; composition of ferromagnetic material H01F 1/00; gyrators H03H 7/002})\)

[details concerning the memory cell structure, e.g. the layers of the ferromagnetic memory cell]

[Auxiliary circuits]

[Address circuits or decoders]

[Bit-line or column circuits]

[Word-line or row circuits]

[Cell access]

[Reading or sensing circuits or methods]

[Writing or programming circuits or methods]

[Verifying circuits or methods]

[Timing circuits or methods]

[Protection circuits or methods]

[Power supply circuits]

using Hall-effect devices

using non-linear reactive devices in resonant circuits

using parametrons \(\text{, i.e. ferroresonant triggers; with overcritica feedback magnetic amplifiers or similar (pulse generators using parametrons and ferroresonant devices H03K 19/162, H03K 19/164; counters using such elements H03K 23/001)}\)

using ferroelectric elements \(\text{, using multibit ferroelectric storage elements G11C 11/565}; \text{pulse generators using ferroelectric elements H03K 3/45; counters using such elements H03K 23/76)}\)

[using ferroelectric capacitors]

[using MOS with ferroelectric gate insulating film]

[Auxiliary circuits]

[Address circuits or decoders]

[Bit-line or column circuits]

[Word-line or row circuits]

[Cell access]

[Reading or sensing circuits or methods]

[Writing or programming circuits or methods]

[Verifying circuits or methods]

[Timing circuits or methods]

[Protection circuits or methods]

[Power supply circuits]

using electrostatic storage on a common layer, e.g. Forrester-Haef tubes \(\{\text{William tubes (G11C 11/22 takes precedence; construction of Williams tubes H01J 31/00)}\}\)

using capacitors \(\text{G11C 11/22 takes precedence; using a combination of semiconductor devices and capacitors G11C 11/34, e.g. G11C 11/40)}\)

using discharge tubes \(\{\text{counters using such elements H03K 25/00}\}\)

[using counting tubes G11C 11/265; pulse generators, electronic switches, logic circuits using such elements H03K 3/37, H03K 17/52, H03K 19/04}\)

using vacuum tubes \(\{\text{counting tubes G11C 11/265; pulse generators, electronic switches, logic circuits using such elements H03K 3/37, H03K 17/52, H03K 19/04}\}\)

using semiconductor devices \(\{\text{processes or apparatus for the manufacture or treatment of semiconductor or solid state devices H01L 21/00; integrated circuit devices H01L 27/00; generating electric pulses, e.g. bistable devices using semiconductor devices H03K 3/00}\}\)

with charge storage in a depletion layer, e.g. charge coupled devices \(\{\text{in shift registers G11C 19/282}\}\)

using diodes, e.g. as threshold elements \(\{\text{i.e. diodes assuming a stable ON-stage when driven above their threshold (S- or N- characteristic)}\}\)

using tunnel diodes

using thyristors \(\{\text{or the avalanche or negative resistance type, e.g. PNPN, SCR, SCS, UJT}\}\)

using transistors

forming cells needing refreshing or charge regeneration, i.e. dynamic cells

with charge regeneration individual to each memory cell, i.e. internal refresh

with charge regeneration common to a multiplicity of memory cells, i.e. external refresh

with one charge-transfer gate, e.g. MOS transistor, per cell

[using a plurality of serially connected access transistors, each having a storage capacitor]

\textbf{WARNING}

Not complete, see also \text{G11C 11/404}

with three charge-transfer gates, e.g. MOS transistors, per cell

Management or control of the refreshing or charge-regeneration cycles

[Arbitration, priority and concurrent access to memory cells for read/write or refresh operations]

[Refresh operations in memory devices with an internal cache or data buffer]

[External triggering or timing of internal or partially internal refresh operations, e.g. auto-refresh or CAS-before-RAS triggered refresh]

[Internal triggering or timing of refresh, e.g. hidden refresh, self refresh, pseudo-SRAMs]

[Refresh operations over multiple banks or interleaving]

[Partial refresh of memory arrays]

[Temperature related aspects of refresh operations]
11/4063 . . . . . . . Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing or timing
11/4067 . . . . . . . for memory cells of the bipolar type
11/407 . . . . . . . for memory cells of the field-effect type
11/4072 . . . . . . . Circuits for initialisation, powering up or down, clearing memory or presetting
11/4074 . . . . . . . Power supply or voltage generation circuits, e.g. bias voltage generators, substrate voltage generators, back-up power, power control circuits
11/4076 . . . . . . . Timing circuits (for regeneration management G11C 11/406)
11/4078 . . . . . . . Safety or protection circuits, e.g. for preventing inadvertent or unauthorised reading or writing; Status cells; Test cells (protection of memory contents during checking or testing G11C 29/52)
11/408 . . . . . . . Address circuits
11/4082 . . . . . . . [Address Buffers; level conversion circuits]
11/4085 . . . . . . . [Word line control circuits, e.g. word line drivers, - boosters, - pull-up, - pull-down, - precharge]
11/4087 . . . . . . . [Address decoders, e.g. bit- or word line decoders; Multiple line decoders]
11/409 . . . . . . . Read-write (R-W) circuits
11/4091 . . . . . . . Sense or sense/refresh amplifiers, or associated sense circuitry, e.g. for coupled bit-line precharging, equalising or isolating
11/4093 . . . . . . . Input/output (I/O) data interface arrangements, e.g. data buffers
11/4094 . . . . . . . Bit-line management or control circuits
11/4096 . . . . . . . Input/output (I/O) data management or control circuits, e.g. reading or writing circuits, I/O drivers or bit-line switches
11/4097 . . . . . . . Bit-line organisation, e.g. bit-line layout, folded bit lines
11/4099 . . . . . . . Dummy cell treatment; Reference voltage generators
11/41 . . . . . . . forming [static] cells with positive feedback, i.e. cells not needing refreshing or charge regeneration; e.g. bistable multivibrator or Schmitt trigger
11/411 . . . . . . . using bipolar transistors only
11/4113 . . . . . . . [with at least one cell access to base or collector of at least one of said transistors, e.g. via access diodes, access transistors]
11/4116 . . . . . . . [with at least one cell access via separately connected emitters of said transistors or via multiple emitters, e.g. T2L, ECL]
11/412 . . . . . . . using field-effect transistors only ([latent image memory G11C 7/20; multi-port cells G11C 8/16])
11/4125 . . . . . . . [Cells incorporating circuit means for protection against loss of information (in general G11C 5/005)]

11/413 . . . . . . . Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing, power reduction (in general G11C 5/00 - G11C 8/00)
11/414 . . . . . . . for memory cells of the bipolar type
11/415 . . . . . . . Address circuits
11/416 . . . . . . . Read-write (R-W) circuits
11/417 . . . . . . . for memory cells of the field-effect type
11/418 . . . . . . . Address circuits
11/419 . . . . . . . Read-write (R-W) circuits
11/42 . . . . . . . using opto-electronic devices, i.e. light-emitting and photoelectric devices electrically or optically - [feedback -] coupled
11/44 . . . . . . . using superconductive elements, e.g. cryotron
11/46 . . . . . . . using thermoelectric elements
11/48 . . . . . . . using displaceable coupling elements, e.g. ferromagnetic cores, to produce change between different states of mutual or self-inductance

13/00 Digital stores characterised by the use of storage elements not covered by groups G11C 11/00, G11C 23/00 - G11C 25/00
13/0002 . . . . . . . [using resistive RAM [RRAM] elements]
13/0004 . . . . . . . [comprising amorphous/crystalline phase transition cells]
13/0007 . . . . . . . [comprising metal oxide memory material, e.g. perovskites]
13/0009 . . . . . . . [RRAM elements whose operation depends upon chemical change]
G11C

13/0011 . . . [comprising conductive bridging RAM [CBRAM] or programming metallization cells [PMCs]]
13/0014 . . . [comprising cells based on organic memory material]
13/0016 . . . [comprising polymers]
13/0019 . . . [comprising bio-molecules]
13/0021 . . . [Auxiliary circuits]
13/0023 . . . [Address circuits or decoders]
13/0026 . . . [Bit-line or column circuits]
13/0028 . . . [Word-line or row circuits]
13/003 . . . [Cell access]
13/0033 . . . [Disturbance prevention or evaluation; Refreshing of disturbed memory data]
13/0035 . . . [Evaluating degradation, retention or wearout, e.g. by counting writing cycles]
13/0038 . . . [Power supply circuits]
13/004 . . . [Reading or sensing circuits or methods]
2013/0042 . . . [Read using differential sensing, e.g. bit line [BL] and bit line bar [BLB]]
2013/0045 . . . [Read using current through the cell]
2013/0047 . . . [Read destroying or disturbing the data]
2013/005 . . . [Read using potential difference applied between cell electrodes]
2013/0052 . . . [Read process characterized by the shape, e.g. form, length, amplitude of the read pulse]
2013/0054 . . . [Read is performed on a reference element, e.g. cell, and the reference sensed value is used to compare the sensed value of the selected cell]
2013/0057 . . . [Read done in two steps, e.g. wherein the cell is read twice and one of the two read values serving as a reference value]
13/0059 . . . [Security or protection circuits or methods]
13/0061 . . . [Timing circuits or methods]
13/0064 . . . [Verifying circuits or methods]
2013/0066 . . . [Verify correct writing whilst writing is in progress, e.g. by detecting onset or cessation of current flow in cell and using the detector output to terminate writing]
13/0069 . . . [Writing or programming circuits or methods]
2013/0071 . . . [Write using write potential applied to access device gate]
2013/0073 . . . [Write using bi-directional cell biasing]
2013/0076 . . . [Write operation performed depending on read result]
2013/0078 . . . [Write using current through the cell]
2013/008 . . . [Write by generating heat in the surroundings of the memory material, e.g. thermowrite]
2013/0083 . . . [Write to perform initialising, forming process, electro forming or conditioning]
2013/0085 . . . [Write a page or sector of information simultaneously, e.g. a complete row or word line]
2013/0088 . . . [Write with the simultaneous writing of a plurality of cells]
2013/009 . . . [Write using potential difference applied between cell electrodes]
2013/0092 . . . [Write characterized by the shape, e.g. form, length, amplitude of the write pulse]
2013/0095 . . . [Write using strain induced by, e.g. piezoelectric, thermal effects]
13/0097 . . . [Erasing, e.g. resetting, circuits or methods]
13/002 . . . [using elements whose operation depends upon chemical change ([G11C 13/009 takes precedence]); using electrochemical charge G11C 11/00]
13/025 . . . [using fullerene, e.g. C60, or nanotubes, e.g. carbon or silicon nanotubes]
13/04 . . . [using optical elements [using other beam accessed elements, e.g. electron, ion beam ([using electrostatic memory tubes G11C 11/23; recording of television signals H04N 5/76])]
13/041 . . . [using photochromic storage elements (G11C 13/042 takes precedence)]
13/042 . . . [using information stored in the form of an interference pattern (G11C 13/042 takes precedence)]
13/043 . . . [using magnetic (hologram, lippman; holography G02H, G02B 5/32)]
13/044 . . . [using electro-optical elements]
13/045 . . . [using photochromic storage elements]
13/046 . . . [using other storage elements storing information in the form of an interference pattern]
13/047 . . . [using electro-optical elements (G11C 13/042 takes precedence)]
13/048 . . . [using other optical storage elements]
13/06 . . . [using magneto-optical elements ([G11C 13/042 takes precedence]) magneto-optics in general G02F]

14/00 Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down
{[bistable elements storing the actual state when the supply voltage fails H03K 3/023, H03K 3/037, H03K 3/2865, H03K 3/356008]}
14/0009 . . . [in which the volatile element is a DRAM cell]
14/0018 . . . [whereby the nonvolatile element is an EEPROM element, e.g. a floating gate or metal-nitride-oxide-silicon [MNOS] transistor]
14/0027 . . . [and the nonvolatile element is a ferroelectric element]
14/0036 . . . [and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell]
14/0045 . . . [and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material]
14/0054 . . . [in which the volatile element is a SRAM cell]
14/0063 . . . [and the nonvolatile element is an EEPROM element, e.g. a floating gate or MNOS transistor]
14/0072 . . . [and the nonvolatile element is a ferroelectric element]
14/0081 . . . [and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell]
14/009 . . . [and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material]
Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores (in which information is addressed to a specific location G11C 11/00; selection information using addressing means, e.g. hashing, tree addressing, chaining G06F 11/22; information retrieval systems using a computer G06F 16/00))

Erasable programmable read-only memories (G11C 14/00 takes precedence)

Electrically programmable (programmable multibit digital storage elements G11C 11/5621)

Using variable threshold transistors, e.g. FAMOS

Comprising cells containing floating gate transistors (G11C 16/0483, G11C 16/0491 take precedence)

Comprising cells containing a single floating gate transistor and no select transistor, e.g. UV EPROM

Comprising cells containing a merged floating gate and select transistor

Comprising cells containing a single floating gate transistor and one or more separate select transistors

Comprising cells containing multiple floating gate devices, e.g. separate read-and-write FAMOS transistors with connected floating gates

Floating gate memory cells with both P and N channel memory transistors, usually sharing a common floating gate

Comprising plural independent floating gates which store independent data (for storage of more than two stable states at a single floating gate G11C 11/5621)

Comprising cells with charge storage in an insulating layer, e.g. metal-nitride-oxide-silicon [MNOS], silicon-oxide-nitride-oxide-silicon [SONOS] (G11C 16/0483, G11C 16/0491 take precedence)

Comprising plural independent storage sites which store independent data (for storage of more than two stable states at a single storage site G11C 11/5621)

Comprising cells having several storage transistors connected in series

Virtual ground arrays

Auxiliary circuits, e.g. for writing into memory (in general G11C 7/00)

Address circuits; Decoders; Word-line control circuits

Programming or data input circuits

[External programming circuits, e.g. EPROM programmers; In-circuit programming or reprogramming; EPROM emulators]

Circuits or methods for updating contents of nonvolatile memory, especially with "security" features to ensure reliable replacement, i.e. preventing that old data is lost before new data is reliably written

Programming all cells in an array, sector or block to the same state prior to flash erasing

Programming voltage switching circuits

Circuits for erasing electrically, e.g. erase voltage switching circuits

For erasing blocks, e.g. arrays, words, groups

Circuits for erasing optically

Initialising; Data preset; Chip identification

Safety or protection circuits preventing unauthorised or accidental access to memory cells

Preventing erasure, programming or reading when power supply voltages are outside the required ranges

Bit-line control circuits

Sensing or reading circuits; Data output circuits

Using differential sensing or reference cells, e.g. dummy cells

Power supply circuits

Timing circuits

Determination of programming status, e.g. threshold voltage, overprogramming or underprogramming, retention

Convergence or correction of memory cell threshold voltages; Repair or recovery of overerased or overprogrammed cells

Circuits or methods to recover overerased nonvolatile memory cells detected during erase verification, usually by means of a "soft" programming step

Circuits or methods to recover overprogrammed nonvolatile memory cells detected during program verification, usually by means of a "soft" erasing step

Disturbance prevention or evaluation; Refreshing of disturbed memory data

Circuits or methods to evaluate read or write disturbance in nonvolatile memory, without steps to mitigate the problem

Circuits or methods to prevent or reduce disturbance of the state of a memory cell when neighbouring cells are read or written

Circuits or methods to detect disturbed nonvolatile memory cells, e.g. which still read as programmed but with threshold less than the program verify threshold or read as erased but with threshold greater than the erase verify threshold, and to reverse the disturbance via a refreshing programming or erasing step

Circuits or methods to verify correct programming or erasure

Circuits or methods to verify correct erasure or for detecting overerased cells

Circuits or methods to verify correct erasure of nonvolatile memory cells
Read-only memories programmable only once; 
Semi-permanent stores, e.g. manually-replaceable information cards (e.g. multibit read-only memories (G11C 11/562); erasable programmable read-only memories G11C 16/00; coding, decoding or code conversion, in general H03M; combination of ROM and RAM G11C 11/005; G11C 14/00; for electrical control of combustion engines P02D 41/240));

17/005 . . . with a storage element common to a large number of data, e.g. perforated card (G11C 17/02, G11C 17/04 take precedence)

17/02 . . using magnetic or inductive elements (G11C 17/14 takes precedence)

17/04 . . using capacitive elements (G11C 17/06, G11C 17/14 take precedence)

17/06 . . using diode elements (G11C 17/14 takes precedence)

17/08 . . using semiconductor devices, e.g. bipolar elements (G11C 17/06, G11C 17/14 take precedence)

17/10 . . . in which contents are determined during manufacturing by a predetermined arrangement of coupling elements, e.g. mask-programmable ROM

17/12 . . . using field-effect devices

17/13 . . . [comprising cells having several storage transistors connected in series]

17/16 . . using electrically-fusable links

17/165 . . . Memory cells which are electrically programmed to cause a change in resistance, e.g. to permit multiple resistance steps to be programmed rather than conduct to or from non-conduct change of fuses and antifuses (digital stores using resistance random access memory elements G11C 13/0002)

17/18 . . Auxiliary circuits, e.g. for writing into memory (in general G11C 7/00)

19/00 Digital stores in which the information is moved stepwise, e.g. shift register (counting chains H03K 23/00) (stack stores, push-down stores (linear pulse counters H03K 23/54, pulse distributors H03K 5/15, methods and arrangements for shifting data G06F 5/01))

19/005 . . with ferro-electric elements (condensers)

19/02 . . using magnetic elements (G11C 19/14 takes precedence)

19/04 . . using cores with one aperture or magnetic loop

19/06 . . using structures with a number of apertures or magnetic loops, e.g. transfluxors [laddic]

19/08 . . using thin films in plane structure ((thin magnetic films and apparatus or processes specially adapted for manufacturing or assembling the same H01F 10/00, H01F 41/14))

19/080 . . . [using magnetic domain propagation]

19/0816 . . . [using a rotating or alternating coplanar magnetic field]

19/0825 . . . [using a variable perpendicular magnetic field]

19/0833 . . . [using magnetic domain interaction]

19/0841 . . . [using electric current]

19/085 . . . [generating magnetic fields therefor, e.g. uniform magnetic field for magnetic domain stabilisation (coil construction H01F 5/00; electromagnets H01F 7/00)]

19/0858 . . . [generating, replicating or annihilating magnetic domains (also comprising different types of magnetic domains, e.g. “Hard Bubbles”) (G11C 19/0866 takes precedence)]

19/0866 . . . [detecting magnetic domains (measuring or detecting magnetic fields in general G01R 33/02)]
Digital stores in which the information circulates (continuously) (stepwise G11C 19/00)

21/005 . . . (using electrical delay line (construction of such lines H03H 7/30, H03H 11/26))
21/02 . . . (using electromechanical delay lines, e.g. using a mercury tank (construction of such lines H03H 9/00))
21/023 . . . (using piezo-electric transducers, e.g. mercury tank)
Test algorithms, e.g. memory scan [MScan] algorithms; Test patterns, e.g. checkerboard patterns

Built-in arrangements for testing, e.g. built-in self testing [BIST] [or interconnection details]

[comprising voltage or current generators]

[comprising I/O circuitry]

[comprising clock generation or timing circuitry]

[Word line control]

[Bit line control]

[Location of test circuitry on chip or wafer]

[Error catch memory]

Implementation of control logic, e.g. test mode decoders

Address generation devices; Devices for accessing memories, e.g. details of addressing circuits

[Address decoder]

[Manipulation of word size]

[Address conversion or mapping, i.e. logical to physical address]

using counters or linear-feedback shift registers [LFSR]

Accessing serial memories

Accessing extra cells, e.g. dummy cells or redundant cells

Accessing multiple arrays (G11C 29/24 takes precedence)

[Concurrent test]

Dependent multiple arrays, e.g. multi-bit arrays

Accessing single arrays

Serial access; Scan testing

[Scan chain]

Accessing multiple bits simultaneously

Data generation devices, e.g. data inverters

[Pattern generator]

Response verification devices

using compression techniques

[Comparison of products, i.e. test results of chips or with golden chip]

using error correcting codes [ECC] or parity check

Indication or identification of errors, e.g. for repair

{for self repair}

[Internal storage of test result, quality data, chip identification, repair information]

Test trigger logic

Arrangements in static stores specially adapted for testing by means external to the store, e.g. using direct memory access [DMA] or using auxiliary access paths (external testing equipment G11C 29/56)

Marginal testing, e.g. race, voltage or current testing

{of threshold voltage}

{of impedance}

{of timing}

{of retention}

Protection of memory contents; Detection of errors in memory contents

Arrangements for designing test circuits, e.g. design for test [DFT] tools

External testing equipment for static stores, e.g. automatic test equipment [ATE]; Interfaces therefor

[Pattern generation]

[Error analysis, representation of errors]

[Timing aspects, clock generation, synchronisation]

[Apparatus features]

[Interface to device under test]

[Display of error information]

[Error catch memory]

Masking faults in memories by using spares or by reconfiguring

(by replacing auxiliary circuits, e.g. spare voltage generators, decoders or sense amplifiers, to be used instead of defective ones)

(with optimized replacement algorithms)

(using duplex memories, i.e. using dual copies)

[using address translation or modifications]

(using duplex memories, i.e. using dual copies)

[using optimized replacement algorithms]

(using auxiliary circuits, e.g. spare voltage generators, decoders or sense amplifiers, to be used instead of defective ones)

using compression techniques

(with improved access time or stability)

(with substitution of defective spares)

(with roll call arrangements for redundant substitutions)

(with reduced power consumption)

(with improved access time or stability)

(by introducing a delay in a signal path)

(by splitting the decoders in stages)

(by choosing redundant lines at an output stage)

(by adjacent switching)

[in serial access memories, e.g. shift registers, CCDs, bubble memories]
Subject matter not provided for in other groups of this subclass

Indexing scheme relating to arrangements for writing information into, or reading information out from, a digital store

- Isolation gates, i.e. gates coupling bit lines to the sense amplifier
- Transfer gates, i.e. gates coupling the sense amplifier output to data lines, I/O lines or global bit lines
- Register arrays
- Sense amplifier related aspects
- Sense amplifier enabled by a address transition detection related control signal
- Current sense amplifiers
- Sense amplifier drivers
- Frequency reading type sense amplifier
- Integrator type sense amplifier
- Aspects relating to interfaces of memory device to external buses
- Analog or multilevel bus
- Compression or decompression of data before storage
- Embedded memory devices, e.g. memories with a processing device on the same die or ASIC memory designs
- Aspects related to pads, pins or terminals
- Serial-parallel conversion of data or prefetch
- Wide data ports
- Equalization of bit lines
- Solid state audio (deprecated, only for historical reasons, G06F 3/16, G11B)
- Control and timing of internal memory operations
- Concurrent read and write (for multi-port memory G11C 7/1075)
- Late write
- Standby or low power modes
- Copy
- Memory devices with an internal cache buffer
- Calibration
- Write conditionally, e.g. only if new data and old data differ
- Latency related aspects
- Timing of a read operation (sense amplifier timing G11C 7/08, G11C 7/08)
- Timing of a write operation (sense amplifier timing G11C 7/08, G11C 7/08)

Indexing scheme relating to digital stores characterized by the use of particular electric or magnetic storage elements; Storage elements therefor

- Indexing scheme relating to cells needing refreshing or charge regeneration, i.e. dynamic cells
- Memory devices with multiple cells per bit, e.g. twin-cells
- Memory devices with silicon-on-insulator cells
- Refreshing of dynamic cells
- Calibration or ate or cycle tuning
- Parity or ECC in refresh operations
- Interleaved refresh operations
- Low level details of refresh operations
- Pseudo-SRAMs
- Refresh in standby or low power modes
- Voltage or leakage in refresh operations
- Indexing scheme relating to G11C 11/56 and sub-groups for features not covered by these groups
- Multilevel memory cell aspects
- Multilevel memory cell with more than one control gate
- Multilevel memory cell with more than one floating gate
- Multilevel memory cell with additional gates, not being floating or control gates
- Multilevel memory cell comprising negative resistance, quantum tunneling or resonance tunneling elements
- Multilevel magnetic memory cell using non-magnetic non-conducting interlayer, e.g. MTJ
- Multilevel magnetic memory cell using non-magnetic conducting interlayer, e.g. GMR, SV, PSV
- Multilevel ROM cell programmed by source, drain or gate contacting
- Multilevel memory programming aspects
- Multilevel programming verification
- Multilevel programming of more than one cell
- Multilevel programming and reading
- Multilevel programming and programming verification
- Multilevel memory reading aspects
- Multilevel memory reading of more than one cell
- Multilevel reading using successive approximation
- Mixed concurrent serial multilevel reading
- Reference cells
- Miscellaneous aspects
- Multilevel memory having cells with different number of storage levels
- Multilevel memory with buffers, latches, registers at input or output
- Multilevel memory comprising cache storage devices
- Multilevel memory comprising counting devices
- Multilevel memory with current-mirror arrangements
- Multilevel memory with flag bits, e.g. for showing that a "first page" of a word line is programmed but not a "second page"
- Multilevel memory with bit inversion arrangement
- Multilevel memory programming, reading or erasing operations wherein the order or sequence of the operations is relevant
Indexing scheme relating to G11C 13/00 for features not covered by this group

- Resistive cells; Technology aspects
- Metal ion trapping, i.e. using memory material including cavities, pores or spaces in form of tunnels or channels wherein metal ions can be trapped but do not react and form an electrodeposit creating filaments or dendrites
- Non-metal ion trapping, i.e. using memory material trapping non-metal ions given by the electrode or another layer during a write operation, e.g. trapping, doping
- Dissociation, i.e. using memory material including molecules which, during a write operation, are dissociated in ions which migrate further in the memory material
- Use of different molecule structures as storage states, e.g. part of molecule being rotated
- Current-voltage curve
- Memory cell being a nanotube, e.g. suspended nanotube
- Memory cell being a nanowire transistor
- Memory cell being a nanowire having RADIAL composition
- Memory cell comprising at least a nanowire and only two terminals
- Resistive cell, memory material aspects
- Material having complex metal oxide, e.g. perovskite structure
- Material having simple binary metal oxide structure
- Material including silicon
- Material includes an oxide or a nitride
- Material including carbon, e.g. graphite, grapheme
- Resistive cell structure aspects
- Structure including a barrier layer preventing or limiting migration, diffusion of ions or charges or formation of electrolytes near an electrode
- Structure characterized by the electrode material, shape, etc.
- Structure wherein the resistive material being in a transistor, e.g. gate
- Structure including a tunneling barrier layer, the memory effect implying the modification of tunnel barrier conductivity
- Structure including two electrodes, a memory active layer and at least two other layers which can be a passive or source or reservoir layer or a less doped memory active layer
- Structure including two electrodes, a memory active layer and a so called passive or source or reservoir layer which is NOT an electrode, wherein the passive or source or reservoir layer is a source of ions which migrate afterwards in the memory active layer to be only trapped there, to form conductive filaments there or to react with the material of the memory active layer in redox way
- Resistive array aspects

Indexing scheme relating to G11C 16/00 and subgroups, for features not directly covered by these groups

- Structural aspects of erasable programmable read-only memories
- Nonvolatile memory cell provided with a separate control gate for erasing the cells, i.e. erase gate, independent of the normal read control gate
- Floating gate cells in which the floating gate consists of multiple isolated silicon islands, e.g. nanocrystals
- Nonvolatile memory wherein data storage is accomplished by storing relatively few electrons in the storage layer, i.e. single electron memory
- Floating gate memory cells with a single polysilicon layer
- Reading and writing aspects of erasable programmable read-only memories
- Circuits or methods to write a page or sector of information simultaneously into a nonvolatile memory, typically a complete row or word line in flash memory
- Flash programming of all the cells in an array, sector or block simultaneously
- Flash erasure of all the cells in an array, sector or block simultaneously
- Suspension of programming or erasing cells in an array in order to read other cells in it
- Nonvolatile memory in which reading can be carried out from one memory bank or array whilst a word or sector in another bank or array is being erased or programmed simultaneously
Nonvolatile memory in which programming can be carried out in one memory bank or array whilst a word or sector in another bank or array is being erased simultaneously.

Floating gate memory which is adapted to be one-time programmable (OTP), e.g. containing multiple OTP blocks permitting limited update ability.

Floating gate memory programmed by reverse programming, e.g. programmed with negative gate voltage and erased with positive gate voltage or programmed with high source or drain voltage and erased with high gate voltage.

Reduction of number of input/output pins by using a serial interface to transmit or receive addresses or data, i.e. serial access memory.

Indexing scheme relating to checking stores for correct operation, subsequent repair or testing stores during standby or offline operation.

Indexing scheme relating to G11C 29/70, for implementation aspects of redundancy repair.

Location of redundancy information.

Redundancy information stored in a part of the memory core to be repaired.

Redundancy information loaded from the outside into the memory.

Time at which the repair is done.

After packaging.

Before packaging.

Storage technology used for the repair.

E-fuses, e.g. electric fuses or antifuses, floating gate transistors.

Laser fuses.