H01L

SEMICONDUCTOR DEVICES NOT COVERED BY CLASS H10 (use of semiconductor devices for measuring G01; resistors in general H01C; magnets, inductors or transformers H01F; capacitors in general H01G; electrolytic devices H01G 9/00; batteries or accumulators H01M; waveguides, resonators or lines of the waveguide type H01P; line connectors or current collectors H01R; stimulated-emission devices H01S; electromechanical resonators H03H; loudspeakers, microphones, gramophone pick-ups or like acoustic electromechanical transducers H04R; electric light sources in general H05B; printed circuits, hybrid circuits, casings or constructional details of electrical apparatus, manufacture of assemblages of electrical components H05K; use of semiconductor devices in circuits having a particular application, see the subclass for the application)

Definition statement

This place covers:

in general

- discrete and integrated semiconductor devices and
- other electric solid state devices (as far as not provided for in another subclass) and
- details thereof.

This includes the following kind of devices:

- integrated circuit devices, e.g. CMOS integrated devices, DRAM, EPROM or CCD;
- semiconductor devices (e.g. field-effect, bipolar) adapted for rectifying, amplifying, oscillating or switching, e.g. diodes, transistors or thyristors;
- semiconductor devices sensitive to radiation, e.g. photo diodes, photo transistors or solar cells;
- incoherent light emitting diodes, e.g. LED;
- solid state devices using organic materials as the active part or using a combination of organic materials with other materials as the active part, e.g. organic LED or polymer LED;
- electric solid state devices using thermoelectric, superconductive, piezoelectric, electrostrictive, magnetostrictive, galvano-magnetic or bulk negative resistance effects, e.g. thermo couples, Peltier elements, Josephson elements, piezo elements;
- photo-resistors, magnetic field dependent resistors or field effect resistors;
- capacitors having potential barriers or resistors having potential barriers;
- thin-film or thick-film circuits;
- processes and apparatus adapted for the manufacture or treatment of such devices, except where such processes relate to single step processes for which provision exists elsewhere.

Relationships with other classification places

Microstructural devices or systems are classified in subclass B81B, and the processes and apparatus specially adapted for the manufacture or treatment thereof are classified in subclass B81C. So, by way of example, microelectro-mechanical devices (MEMS), containing microelectronic and mechanical components, are classified in group B81B 7/02, and their manufacture, treatment or assembling in the relevant groups of B81C. Microstructural devices or systems working purely electrically or electronically, or related processes or apparatus for the manufacture or treatment thereof are, however, not covered by B81B or B81C and are classified in section H, for example in the groups of the current subclass H01L.

Microstructural devices or systems being of other than purely electrical or electronically type, and apparatus or processes for the manufacture or treatment thereof, which are normally classified in

the subclasses B81B and B81C, may be also classified in those groups of H01L providing for their structural or functional features, whenever such features are of interest per se.

Nanostructures, which are normally classified in subclass B82B, may be also classified in those groups of H01L providing for their structural or functional features, whenever such features are of interest per se.

References

Limiting references

This place does not cover:

Use of semiconductor devices for measuring	G01
Non-adjustable resistors from semiconductor material	H01C 7/00
Magnets, inductors, transformers	H01F
Capacitors in general	H01G
Electrolytic devices	H01G 9/00
Batteries, accumulators	H01M
Waveguides, resonators or lines of the waveguide type	H01P
Line connectors, current collectors	H01R
Lasers, stimulated emission devices, e.g. semiconductor laser	H01S, H01S 5/00
Electromechanical resonators; impedance networks	H03H
Loudspeakers, microphones, gramophone pick-ups or like acoustic electromechanical transducers	H04R
Electric light sources in general	H05B
Printed circuits, hybrid circuits, casings or constructional details of electric apparatus, manufacture of assemblages of electrical components	H05K

Informative references

Attention is drawn to the following places, which may be of interest for search:

Containers merely intended for transport or storage of wafers except during manufacture or finishing devices thereon	B65D 85/30
Conveying systems for semiconductor wafers except during manufacture or treatment of semiconductor or electric solid state devices or components thereon	B65G 49/07
Micromechanical Devices (MEMS)	B81B
Processes and apparatus specially adapted for the manufacture or treatment of microstructural devices or systems	B81C
Coating Material	C23C
Non-mechanical removal of metallic material from surface	C23F
Measurement of Mechanical Vibrations or Ultrasonic, Sonic or Infrasonic Waves	G01H
Measurement of Intensity, velocity, Spectral, Content, Polarization, Phase or Pulse Characteristic of Infrared, Visible or Ultraviolet Light	G01J
Measuring Electrical or Magnetic Variables	G01P

Details of scanning-probe apparatus, in general	G01Q 10/00 - G01Q 90/00
Radio Direction-Finding; Radio Navigation; Determining Distance or Velocity by Use of Radio Waves; Locating or Presence-Detecting by Use of the Reflection or Reradiation of Radio Waves; Analogous Arrangements Using Other Waves	G01S
Measuring Nuclear or X-Radiation	G01T
Electro photography	G03G
Systems for Regulating Electrical or Magnetic Variables	G05F
Digital Computers	G06F
Static Stores	G11C
Conductive and Insulating Materials	H01B
Electric discharge tubes or discharge lamps	H01J
Amplifiers	H03F
Pictorial Communication, e.g. Television	H04N

Special rules of classification

In this subclass, Indexing Codes are mainly attributed with a view to allow retrieval of documents comprising a combination of technical characteristics, some of them being unimportant per se, and, hence, identified as additional information rather than invention information.

In this subclass, both the process and apparatus for the manufacture or treatment of a device and the device itself are classified, whenever both of these are described sufficiently to be of interest.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

assembly of a device	the "assembly" of a device is the building up of the device from its component constructional units and includes the provision of fillings in containers.
complete device	a "complete device" is a device in its fully assembled state which may or may not require further treatment, e.g. electro-forming, before it is ready for use but which does not require the addition of further structural units.
component	a "component" is one electric circuit element of a plurality of elements formed in or on a common substrate.
container	a "container" is an enclosure forming part of the complete device and is essentially a solid construction in which the body of the device is placed, or which is formed around the body without forming an intimate layer thereon.
device	the term "device" refers to an electric circuit element; where an electric circuit element is one of a plurality of elements formed in or on a common substrate it is referred to as a "component".

electrodes	"electrodes" are regions in or on the body of the device (other than the solid-state body itself), which exert an influence on the solid-state body electrically, whether or not an external electrical connection is made thereto. An electrode may include several portions and the term includes metallic regions which exert influence on the solid-state body through an insulating region (e.g. capacitive coupling) and inductive coupling arrangements to the body. The dielectric region in a capacitive arrangement is regarded as part of the electrode. In arrangements including several portions only those portions which exert an influence on the solid-state body by virtue of their shape, size or disposition or the material of which they are formed are considered to be part of the electrode. The other portions are considered to be "arrangements for conducting electric current to or from the solid-state body" or "interconnections between solid state components formed in or on a common substrate", i.e. leads.
encapsulation	an "encapsulation" is an enclosure which consists of one or more layers formed on the body and in intimate contact therewith.
integrated circuit	an "integrated circuit" is a device where all components, e.g. diodes, resistors, are built up on a common substrate and form the device including interconnections between the components.
integration process	processes for the manufacture of at least two different components where the process is especially adapted to their integration, e.g. to take advantage of the integration or to reduce their manufacturing cost. Example: in a CMOS process, the same ion implant dopes the p-MOS gate and the n-MOS source and drain. Consequently, a process for the manufacture of a component per se is not considered as an integration process, even though that component will be part of an integrated circuit.
interconnection	refers to the arrangement of conductive and insulating regions aimed at electrically connecting the respective electrodes of at least two device units, e.g. two transistors.
parts	the term "parts" includes all structural units which are included in a complete "device".
solid state body	the expression "solid state body" refers to the body of material within which, or at the surface of which, the physical effects characteristic of the device occur. In thermoelectric devices it includes all materials in the current path.
wafer	a "wafer" means a slice of semiconductor or crystalline substrate material, which can be modified by impurity diffusion (doping), ion implantation or epitaxy, and whose active surface can be processed into arrays of discrete devices or integrated circuits.

Synonyms and Keywords

In patent documents, the following words/expressions are often used with the meaning indicated:

package	container, encapsulation.

H01L 21/00

Processes or apparatus adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof

Definition statement

This place covers:

Processes and apparatus that are specially adapted for the manufacturing of semiconductor or solid state devices belonging to the type:

- Integrated circuit devices, e.g. CMOS integrated devices, DRAM, EPROM, CCD;
- Semiconductor devices (e.g. field-effect, bipolar) adapted for rectifying, amplifying, oscillating or switching, e.g. diodes, transistors, thyristors;

This main group includes;

- Manufacture or treatment of the above semiconductor devices or of parts thereof
- Manufacture or treatment of solid state devices other than semiconductor devices, or of parts thereof
- Apparatus specially adapted for handling semiconductor or electric solid state devices during manufacture or treatment thereof; Apparatus specially adapted for handling wafers during manufacture or treatment of semiconductor or electric solid state devices or components
- Manufacture or treatment of devices consisting of a plurality of solid state components formed in or on a common substrate or of parts thereof; manufacture of integrated circuit devices or of parts thereof

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Processes for applying liquids or other fluent materials	B05D 1/00
Liquid cleaning (in general)	B08B 3/00
Machines, Devices, or Processes for Grinding or Polishing	B24B
Containers, packaging elements or packages specially adapted for particular articles or materials	B65D 85/00
Shaped ceramic Products	C04B 35/00
Polishing compositions	C09G 1/00
Cleaning Compositions	C11D
Coating by vacuum evaporation, by sputtering or by ion implantation of the coating forming material	C23C 14/00
Chemical coating by decomposition of gaseous compounds, without leaving reaction products of surface material in the coating (CVD)	C23C 16/00
Chemical coating by decomposition of either liquid compounds or solutions of the coating forming compounds,without leaving reaction products of surface material in the coating	C23C 18/00
Etching metallic material by chemical means	C23F 1/00
Processes for the Electrolytic or Electrophoretic Production of Coatings	C25D
Single Crystal Growth; Epitaxy	C30B
Testing individual semiconductor devices	G01R 31/00

Preparation of originals for the photomechanical production of textured or patterned surfaces	G03F 1/00
Photolithographic, production of textured or patterned surfaces	G03F 7/00
Registration or positioning of originals, masks, frames, photographic sheets or textured or patterned surfaces	G03F 9/00
Discharge tubes with provision for introducing objects or material to be exposed to the discharge (plasma etching; ion implantation)	H01J 37/00
Apparatus or processes specially adapted for manufacturing or adjusting assemblages of electric components	H05K 13/00
Processes or apparatus specially adapted for the manufacture or treatment of devices or parts thereof	H10B, H10D, H10F, H10H, H10K or H10N

Special rules of classification

Single mono-steps for which a provision exists elsewhere in CPC need not to be classified in H01L 21/00, except if they are specific to the fabrication of semiconductor devices as defined under H01L 21/00. E.g., apparatuses which are not specific to the fabrication of these devices, e.g. apparatuses for depositing layers, are classified in C23C or C30B.

Direct pre-treatment or direct post-treatment of a specific step is classified under the specific step if no other place exists in H01L 21/00. Example: annealing after layer coating is classified together with the coating. Exception: cleaning, see H01L 21/02041

In H01L 21/00, poly-silicon is generally considered as a conductive material for classification purposes, except for its deposition (H01L 21/02365) where it is considered as semiconducting.

Polishing or chemical-mechanical polishing are not distinguished for classification.

Machines and apparatuses for which a provision exists somewhere else in CPC are not classified In H01L 21/00. For example apparatus for deposition of materials are classified in C23C or C30B.

Machines and apparatuses for which no particular provision exists in CPC are classified in H01L 21/67 and subgroups. See also the notes under H01L 21/67.

Processes mainly consisting of features of the use of the elements of the apparatus and which are necessary to operate said apparatus (like for example rotating the turntable of a polisher, evacuating the chamber of a plasma appraratus etc...) need not to be classified in H01L 21/00.

Subject matter relating to processes and apparatus which are clearly suitable for manufacture or treatment of devices whose bodies comprise elements of the fourth group of the Periodic Table (silicon, germanium), and where the material used is not explicitly specified, is classified in the subgroups relating to semiconductors of the fourth group of the Periodic Table (silicon, germanium).

For multistep processes, a junction between two regions of the same material but in a different crystalline state, e.g. amorphous silicon or polysilicon emitters on single crystalline silicon, is not considered as a heterojunction.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Dry Process	refers to processes wherein only gases or vapours are provided on the surface of a substrate, e.g. a wafer, irrespective of the physical state of the reaction products, gaseous, liquid or solid.

Wet Process	refers to processes wherein only liquids are provided at the surface of a wafer, including the condensation on the surface of a wafer of gaseous components.
Pre-, post-treatment	direct, for example in situ, treatment, preceding or following a main technological step, aimed at improving said main technological step or its result. Not considered as a technological step per se. Examples: - annealing or crystallisation after deposition of insulating layers, - cleaning before or after a technological step, - modifying an insulating layer just after its formation, e.g. implantation after deposition
After treatment	Subsequent main technological step. Examples: - patterning or polishing of a layer after deposition- modifying an insulating layer after a step which is not the formation of the insulating layer

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

CVD	Chemical vapour deposition
PECVD	Plasma enhanced CVD
LPCVD	Low pressure CVD
PVD	Physical Vapour Deposition
ALD	Atomic layer deposition
ALE	Atomic layer epitaxy
CMP	Chemical mechanical polishing
ECMP	Electrochemical CMP
SOI	Silicon on Insulator
BESOI	Bonded and Etched-Back Silicon-On-Insulator
SOS	Silicon on Sapphire
HSG	Hemispherical grain
RIE	Reactive ion etching
BSG	boron silicate glass
PSG	phosphorous silicate glass
BPSG	boron phosphorous silicate glass
USG	Undoped silicate glass
FSG	Fluorine silicate glass
PZT	Lead zirconate titanate
BST	Barium strontium titanate
HSQ	Hydrogen silsesquioxane
MBE	Molecular beam epitaxy
ELO	Epitaxial lateral overgrowth
MIS	Metal-insulator-semiconductor
MOS	Metal-oxide-semiconductor
CMOS	Complementary MOS

DMOS	Double diffused MOS
VDMOS	Vertical DMOS
LDMOS	Lateral DMOS
IMPATT	Impact Ionization Avalanche Transit Time
TRAPATT	Trapped Plasma Avalanche Triggered Transistor
SITh	Static induction thyristor
FCTh	Field controlled thyristor
IGBT	Insulated Gate Bipolar Transistor
HET	Hot electron transistor
SET	Single electron transistor
SIT	Static Induction Transistor
MBT	Metal base transistor
RHET	Resonant tunnelling hot electron transistor
RTT	Resonant tunnelling transistor
BBT	Bulk barrier transistor
PBT	Permeable Base Transistor
HFET	Heterostructure FET
HIGFET	Heterostructure Insulated Gate FET
SISFET	Semiconductor-insulator-semiconductor FET
HJFET	Hetero Junction FET
MISFET	Metal-insulator-semiconductor FET
JFET	Junction FET
FinFET	FET with Fin-type channel
MuGFET	Multi Gate FET
HEMT	High Electron Mobility Transistor
PDBT	Planar doped barrier transistor
CHINT	Charge injection transistor
LDD	lightly doped drain
DDD	Double diffused drain
EPIC	Epitaxial Passivated Integrated Circuit
LOCOS	Local Oxidation of Silicon
SWAMI	Side Wall Masked Isolation
SILO	Sealed Isolation LOCOS
SIMOX	Separation by Implantation of Oxygen
FIPOS	Full Isolation by porous oxidized silicon
ELTRAN	Epitaxial Layer Transfer
SEG	Selective Epitaxial Growth
DRAM	Dynamic RAM
CCD	Charge Coupled Device

H01L 21/02002

{Preparing wafers}

Definition statement

This place covers:

Multi-step processes for the manufacture of semiconductor wafers for the fabrication of semiconductor devices as defined under H01L 21/00, prior to the fabrication of any device or part of device, i.e. between the sawing of ingots (covered by B28D) and the cleaning of the wafers (H01L 21/02041), e.g. grinding followed by lapping and polishing.

Covers the preparation of bulk semiconductor wafers (e.g. bulk silicon wafers).

Relationships with other classification places

See also H10D 84/00, which has been used for classifying the fabrication of substrates containing parts of Group-IV and Group AIII-BV semiconductors.

See also C30B 33/00.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thermal smoothening	H01L 21/324
Fabrication of inhomogeneous wafer, e.g. SOI	H01L 21/76
Marking of wafers	H01L 23/544
Forming flats	C30B 33/00

H01L 21/02005

{Preparing bulk and homogeneous wafers}

Definition statement

This place covers:

Bulk, homogeneous wafers:

- Group IV, Si, Ge,
- Group III-V, GaAs, InP,

H01L 21/0201

{Specific process step}

Definition statement

This place covers:

Multistep process for preparing wafers where the accent is put on a specific step.

H01L 21/02013

{Grinding, lapping}

Definition statement

This place covers:

Multistep process for preparing wafers where the accent is put on the grinding or lapping, e.g. multiple grinding steps.

H01L 21/02016

{Backside treatment}

Definition statement

This place covers:

Multistep process for preparing wafers where the accent is put on the backside treatment.

Includes backside treatment for recognition purposes

H01L 21/02019

{Chemical etching}

Definition statement

This place covers:

Multistep process for preparing wafers where the accent is put on the chemical etching step or steps.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Chemical or electrical treatment, e.g. electrolytic etching	H01L 21/306

H01L 21/02021

{Edge treatment, chamfering}

Definition statement

This place covers:

Multistep process for preparing wafers where the accent is put on the edge treatment, e.g. chamfering.

References

Limiting references

This place does not cover:

Does not cover the processing of edges of Smart Cut donor substrates, classified in reclaiming/reprocessing	H01L 21/02032

H01L 21/02024

{Mirror polishing}

Definition statement

This place covers:

Multistep process for preparing wafers where the accent is put on the mirror polishing.

Special rules of classification

In case a mechanical mirror polishing is completed by a chemical flattening step, e.g. a gaseous flattening step, the latter is classified independently.

H01L 21/02027

{Setting crystal orientation}

Definition statement

This place covers:

Multistep processes for preparing wafers having a specific orientation planes as useful plane, or a specific orientation plane in a plane parallel to the surface.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Single-crystal growth by pulling from a melt characterised by the seed, e.g. its crystallographic orientation	C30B 15/36

H01L 21/0203

{Making porous regions on the surface}

Definition statement

This place covers:

Making a surface of the wafer porous. Includes formation of internal porous regions.

References

Limiting references

This place does not cover:

Localized formation (using e.g. masks) of porous regions	H01L 21/306, H01L 21/3063

H01L 21/02032

{by reclaiming or re-processing}

Definition statement

This place covers:

Multistep processes for reclaiming or re-processing, a wafer containing more than a cleaning process. Also contains the re-processing of Smart-Cut donor substrates.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Specific cleaning for reclaiming or reprocessing	H01L 21/02079

H01L 21/02035

{Shaping}

Definition statement

This place covers:

Processes adapted to change the shape of a wafer, either in the surface plane (e.g. square, rectangular wafers), or in cross section (bone cross section).

References

Limiting references

This place does not cover:

The provision of flats, classified with the fabrication of the ingot	C30B

H01L 21/02041

{Cleaning}

Definition statement

This place covers:

Cleaning of wafers before or during manufacturing;

Cleaning is the removal of entities which were always unwanted, like particles, impurities, stringers, fences etc. Also includes the removal of edge beads or unwanted coatings on edges or backside of the wafers etc., except photoresist edge beads and photoresist on backside.

Removal of entities which have had a use or a function (sidewalls, resists etc.) is not considered to be a cleaning.

Includes the removal of natural oxide, see also the section "Special rules for classification within this group" below.

Starts with the deep cleaning carried out before first fabrication step (Piranha-RCA) up to cleaning after singulation.

Relationships with other classification places

Rinsing and drying are seen as a post-treatment of a wet cleaning, classified together with wet cleaning in H01L 21/02052.

References

Limiting references

This place does not cover:

Does not cover the transformation of an impurity or contaminant in something else remaining on the device, e.g. passivation, classified with passivation in general	H01L 21/28247
Processes for the removal of only photoresists, classified in	H01L 21/31127
Removal of excess metal after silicidation, classified in	H01L 21/3213
Does not cover processes for the removal of photoresists edge beads after coating	G03F 7/168, G03F 7/2028

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cleaning apparatus	H01L 21/67005
Cleaning by methods involving the use of tools, brushes, or analogous members, the use or presence of liquid or steam, the use of air flow or gas flow; Cleaning by electrostatic means	B08B 1/00 - B08B 7/00
Detergent compositions, e.g. cleaning solutions or liquids	C11D

Special rules of classification

Removal of only natural oxide is also classified in H01L 21/311 if the process is of special relevance for thick oxides.

Removal of impurities, e.g. side walls after RIE, together with the photoresist is classified in H01L 21/02041, and additionally in H01L 21/311, if the resist removal method is peculiar.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

RCA	standard clean composed of SC-1 and SC-2 at least, with piranha and HF or DHF
SC-1	standard clean 1: NH4OH-H2O2
SC-2	standard clean 2: HCl, H_2O_2
DHF	diluted HF
Piranha	H_2SO_4-peroxide

H01L 21/02043

{Cleaning before device manufacture, i.e. Begin-Of-Line process}

Definition statement

This place covers:

Cleaning of the wafer before any manufacturing step for the device is carried out.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Does not cover the transformation of an impurity or contaminant in something else remaining on the device, e.g. passivation	H01L 21/28247
Processes for the removal of only photoresist	H01L 21/31127
Removal of excess metal after silicidation	H01L 21/3213
Does not cover processes for the removal of photoresist edge beads after coating	G03F 7/168, G03F 7/2028

H01L 21/02046

{Dry cleaning only (H01L 21/02085 takes precedence)}

Definition statement

This place covers:

All cleaning steps are dry, or when the invention is focussed on a dry cleaning aspect, the cleaning also containing more classical wet steps, like RCA.

References

Limiting references

This place does not cover:

Cleaning of diamond	H01L 21/02085

H01L 21/02052

{Wet cleaning only (H01L 21/02085 takes precedence)}

Definition statement

This place covers:

Wet cleaning.

References

Limiting references

This place does not cover:

Cleaning of diamond	H01L 21/02085

Special rules of classification

Rinsing and drying are seen as a post-treatment of a wet cleaning, classified together with wet cleaning in H01L 21/02052.

H01L 21/02054

{combining dry and wet cleaning steps (H01L 21/02085 takes precedence)}

Definition statement

This place covers:

The sequence of combining wet and dry steps.

References

Limiting references

This place does not cover:

Cleaning of diamond	H01L 21/02085

Special rules of classification

Rinsing and drying are seen as a post-treatment of a wet cleaning, classified together wet cleaning in H01L 21/02052.

H01L 21/02057

{Cleaning during device manufacture}

Definition statement

This place covers:

Cleaning when at least a fabrication step for a device (for example, first oxidation) has been carried out.

H01L 21/0206

{during, before or after processing of insulating layers}

Definition statement

This place covers:

- Cleaning after etching gate sidewalls and etching of gate oxide.
- Cleaning after formation of a resist pattern

H01L 21/02079

{Cleaning for reclaiming}

Definition statement

This place covers:

Reclaiming of semiconductor wafers as well as donor semiconductor wafers, e.g. donors in Smart-Cut®

References

Limiting references

This place does not cover:

Etching for reclaiming	H01L 21/02032

H01L 21/02082

{product to be cleaned}

Definition statement

This place covers:

Special products to be cleaned, including particular materials as well as substrates comprising particular features, like vertical features, isolated sidewalls, etc.

H01L 21/02087

{Cleaning of wafer edges}

Definition statement

This place covers:

Removal of edge beads.

References

Limiting references

This place does not cover:

Removal of photoresist edge beads	G03F 7/16, G03F 7/20

H01L 21/0209

{Cleaning of wafer backside}

Definition statement

This place covers:

Removal of impurities or unwanted materials on backside, including parasitic coatings.

References

Limiting references

This place does not cover:

Removal of photoresist edge beads	G03F 7/16, G03F 7/20

H01L 21/02096

{only mechanical cleaning}

Definition statement

This place covers:

The group covers inventions wherein the mechanical aspect is of particular importance. Does not exclude some enhancement by chemical means.

H01L 21/02098

{only involving lasers, e.g. laser ablation}

Definition statement

This place covers:

Covers processes wherein the laser action has a primary function, with or without chemical, mechanical or electrical assistance.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cleaning using a laser per se	B08B 7/0042

H01L 21/02101

{only involving supercritical fluids}

Definition statement

This place covers:

Covers processes wherein the supercritical fluid has a primary function, with or without chemical, mechanical or electrical assistance.

H01L 21/02104

{Forming layers (deposition in general C23C; crystal growth in general C30B)}

Definition statement

This place covers:

Processes for the formation of inorganic and organic layers on a substrate, except photoresist layers (see H01L 21/027), for the fabrication of semiconductor devices as defined under H01L 21/00.

In situ pre- and post-treatments of these processes.

Processes for the formation of a multiplicity of these layers.

Relationships with other classification places

Processes for coating materials in general: C23C

Processes for the electrolytic coating of materials in general: C25D

Processes for the single-crystal growth of materials in general: C30B

References

Limiting references

This place does not cover:

Processes for forming photoresist layers, covered in	H01L 21/027
Processes for forming conductive layers, covered by	H01L 21/283, H01L 21/285, H01L 21/288, H01L 21/3205

Informative references

Attention is drawn to the following places, which may be of interest for search:

Groups and their subdivisions for general aspects of formation of layers.	C23C, C25D, C30B
Photoresist per se	G03F 7/00

Special rules of classification

- Multistep processes for fabricating laminates of insulating and conductive layers, for example insulated gates or capacitors, are classified in the corresponding application, H01L 21/28 for the insulated gates, H10D 1/041 for the capacitors etc. and do not need to be systematically classified in H01L 21/02107. However a group symbol in H01L 21/02107 may be given in case the process for forming the insulating layer is considered of general interest.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

ALD	atomic layer deposition
ALE	atomic layer epitaxy
MBE	molecular beam epitaxy
PECVD	plasma enhanced chemical vapour deposition
PVD	physical vapour deposition
CVD	chemical vapour deposition

H01L 21/02107

{Forming insulating materials on a substrate}

Definition statement

This place covers:

Processes for the formation of inorganic and organic insulating layers on a substrate, except photoresist layers (see H01L 21/027), for the fabrication of semiconductor devices as defined under H01L 21/00.

In situ pre- and post-treatments of these processes.

Processes for the formation of a multiplicity of these layers.

Includes fabrication of insulating

- porous layers,
- organic layers, like polyimide, cyclobutenes etc.
- Spin On Glass layers,
- silicate layers,
- inorganic layers, like SiO_2, Si_3N_4, Al_2O_3, high-k layers, perovskites etc.

Relationships with other classification places

Processes for coating materials in general, including insulating materials: C23C

Processes for the electrolytic coating of materials in general: C25D

Organic or polymer layer composition: see C08G

References

Limiting references

This place does not cover:

Processes for forming photoresist layers	H01L 21/027

Informative references

Attention is drawn to the following places, which may be of interest for search:

Photoresist per se	G03F 7/00

Special rules of classification

The process must be adapted or specific to the fabrication of semiconductor devices as defined under H01L 21/00. The mere mentioning of an intended use in semiconductor fabrication does not require that the document being given a group symbol in H01L 21/02107.

If the deposition is specifically adapted to a specific application, with details as to this specific application, e.g. the fabrication of a MIS or MOS electrode or interconnections, the document should additionally be classified in this specific application, for example in H01L 21/28 for the MIS or MOS aspect.

H01L 21/02112

{characterised by the material of the layer}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Layers comprising sub-layers, i.e. multi-layers, are additionally classified in	H01L 21/022
Porous layers are additionally classified in	H01L 21/02203

H01L 21/02115

{the material being carbon, e.g. alpha-C, diamond or hydrogen doped carbon}

References

Limiting references

This place does not cover:

Carbon Nitride.	H01L 21/02118

H01L 21/02118

{carbon based polymeric organic or inorganic material, e.g. polyimides, poly cyclobutene or PVC (polymers per se C08G, photoresist per se G03F)}

Definition statement

This place covers:

Carbon Nitride.

Carbon based polymeric material

H01L 21/02129

{the material being boron or phosphorus doped silicon oxides, e.g. BPSG, BSG or PSG}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Halogen doped silicon oxides, e.g. fluorine, containing BPSG, PSG, BSG	H01L 21/02131

Special rules of classification

Halogen containing materials, e.g. fluorine, containing BPSG, PSG, BSG, are additionally classified in H01L 21/02131

H01L 21/02164

{the material being a silicon oxide, e.g. SiO_2}

Definition statement

This place covers:

The formation of silicon oxide layers is classified in this group regardless of the precursor or of the process of formation.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

In case of explicit statements on doping, on rest-groups, or on material components, see	H01L 21/02126
Deposition of silicon oxide from organic precursors without further statements on film composition is classified here and in	H01L 21/02205

H01L 21/02167

{the material being a silicon carbide not containing oxygen, e.g. SiC, SiC:H or silicon carbonitrides (H01L 21/02126 and H01L 21/0214 take precedence)}

References

Limiting references

This place does not cover:

The formation of material containing Si, O and C, with or without additional elements	H01L 21/02126
The formation of material containing Si, O and N, with or without additional elements	H01L 21/0214

H01L 21/0217

{the material being a silicon nitride not containing oxygen, e.g. SixNy or SixByNz (H01L 21/02126 and H01L 21/0214 take precedence)}

References

Limiting references

This place does not cover:

The formation of material containing Si, N and C, with or without additional elements	H01L 21/02126
The formation of material containing Si, O and N, with or without additional elements	H01L 21/0214

H01L 21/02172

{the material containing at least one metal element, e.g. metal oxides, metal nitrides, metal oxynitrides or metal carbides (materials containing silicon H01L 21/02123; metal silicates H01L 21/02142)}

References

Limiting references

This place does not cover:

Materials containing silicon	H01L 21/02123

Metal silicates	H01L 21/02142

H01L 21/02175

{characterised by the metal (H01L 21/02197 takes precedence)}

References

Limiting references

This place does not cover:

Materials having a perovskite structure, e.g. $BaTiO_3$	H01L 21/02197

H01L 21/02197

{the material having a perovskite structure, e.g. $BaTiO_3$}

Special rules of classification

Perovskites are not classified in H01L 21/02175 and subgroups thereof.

H01L 21/022

{the layer being a laminate, i.e. composed of sublayers, e.g. stacks of alternating high-k metal oxides (adhesion layers or buffer layers H01L 21/02304, H01L 21/02362)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Adhesion or buffer layers	H01L 21/02304, H01L 21/02362

H01L 21/02214

{the compound comprising silicon and oxygen}

References

Limiting references

This place does not cover:

Mixtures of silane and oxygen	H01L 21/02211

H01L 21/02216

{the compound being a molecule comprising at least one silicon-oxygen bond and the compound having hydrogen or an organic group attached to the silicon or oxygen, e.g. a siloxane}

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Alkoxysilane	siloxane

H01L 21/02219

{the compound comprising silicon and nitrogen}

References

Limiting references

This place does not cover:

Mixtures of silane and oxygen	H01L 21/02211

H01L 21/02227

{formation by a process other than a deposition process}

Special rules of classification

Subject matter classified in the range H01L 21/0223 - H01L 21/02249 is additionally classified in H01L 21/02252, H01L 21/02255, and H01L 21/02258 depending on the type of reaction.

H01L 21/02252

{formation by plasma treatment, e.g. plasma oxidation of the substrate (after treatment of an insulating film by plasma H01L 21/3105 and subgroups)}

References

Limiting references

This place does not cover:

After treatment of an insulating film by plasma	H01L 21/3105

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of an insulating film by introduction of substances into an already existing insulating film is covered by	H01L 21/02318

H01L 21/02255

{formation by thermal treatment (H01L 21/02252 takes precedence; after treatment of an insulating film H01L 21/3105 and subgroups)}

References

Limiting references

This place does not cover:

Formation of insulating layers by plasma treatment, e.g. plasma oxidation of the substrate	H01L 21/02252
After treatment of an insulating film by plasma	H01L 21/3105

H01L 21/02263

{deposition from the gas or vapour phase}

Definition statement

This place covers:

Deposition methods in which the gas or vapour is produced by physical means, e.g. ablation from targets or heating of source materials.

H01L 21/02266

{deposition by physical ablation of a target, e.g. sputtering, reactive sputtering, physical vapour deposition or pulsed laser deposition}

Definition statement

This place covers:

Deposition methods in which the gas or vapour is produced by physical means, i.e. by ablation from targets.

H01L 21/02269

{deposition by thermal evaporation (H01L 21/02293 takes precedence)}

Definition statement

This place covers:

- Deposition methods in which the gas or vapour is produced by heating of source materials.
- Molecular beam epitaxy

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of epitaxial insulating films by a deposition method also under	H01L 21/02293

H01L 21/02271

{deposition by decomposition or reaction of gaseous or vapour phase compounds, i.e. chemical vapour deposition (H01L 21/02266 takes precedence)}

References

Limiting references

This place does not cover:

Deposition by physical ablation of a target, like sputtering, reactive sputtering, physical vapour deposition, pulsed laser deposition	H01L 21/02266

H01L 21/0228

{deposition by cyclic CVD, e.g. ALD, ALE, pulsed CVD}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Deposition by decomposition or reaction of gaseous or vapour phase compounds in the presence of a plasma (PECVD)	H01L 21/02274

Special rules of classification

Subject matter relating to cyclic plasma CVD is additionally classified in H01L 21/02274

H01L 21/02288

{printing, e.g. ink-jet printing (per se B41J)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Printing in general	B41J

H01L 21/02293

{formation of epitaxial layers by a deposition process (epitaxial growth per se C30B)}

References

Limiting references

This place does not cover:

Formation of non-epitaxial layers by MBE	H01L 21/02269
Atomic layer epitaxy [ALE]	H01L 21/0228

Informative references

Attention is drawn to the following places, which may be of interest for search:

Epitaxial growth in general	C30B

H01L 21/02296

{characterised by the treatment performed before or after the formation of the layer (H01L 21/02227 and subgroups take precedence)}

Definition statement

This place covers:

Treatments, carried out just before or just after the formation of an insulating layer, which do not participate in the formation of the layer itself, but which are directly linked to the layer formation.

References

Limiting references

This place does not cover:

Processes participating to the formation of a layer, for example oxidation or nitridation of silicon to form an oxide or nitride layer	H01L 21/02227
After treatments like - etching - cleaning - planarising	H01L 21/311, H01L 21/02041, H01L 21/31051

Special rules of classification

Pre- or post treatments of general nature (pre-, post-cleaning, pre-, post conditioning etc.) without details or routine annealing steps, i.e. thermal treatment without further features as to a special atmosphere, presence of a plasma, thermally induced chemical reactions, change of phase or crystal structure, need not to be given this group symbol.

H01L 21/02299

{pre-treatment}

Definition statement

This place covers:

- Treatments to improve adhesion or change the surface termination

References

Limiting references

This place does not cover:

Treatments by etching	H01L 21/306, H01L 21/311

H01L 21/02301

{in-situ cleaning}

References

Limiting references

This place does not cover:

Ex situ cleaning, covered by	H01L 21/02041

H01L 21/02318

{post-treatment}

Definition statement

This place covers:

The definition should read "post-treatment" instead of after-treatment.

Only covers processes that are part of the layer formation.

References

Limiting references

This place does not cover:

After- treatments performed after completion of the insulating layer	H01L 21/3105

Special rules of classification

Functionalization just after formation should be classified here.

In case the process would also be of interest as an after treatment (H01L 21/3105), both group symbols should be given.

H01L 21/02321

{introduction of substances into an already existing insulating layer (H01L 21/02227 and subgroups take precedence)}

Definition statement

This place covers:

Processes for introducing substances into the formed insulating layer e.g. introduction of phosphorus into silicon oxide, or introduction of nitrogen into silicon nitride to change stoichiometry.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

For the method of introduction of the dopant	H01L 21/02337, H01L 21/02343, H01L 21/02345

Special rules of classification

Introduction of substances into the formed insulating layer is classified both here and in H01L 21/3115

H01L 21/02326

{into a nitride layer, e.g. changing SiN to SiON}

Definition statement

This place covers:

Oxidation of silicon nitride to form silicon oxynitride.

H01L 21/02332

{into an oxide layer, e.g. changing SiO to SiON}

Definition statement

This place covers:

Nitridation of silicon oxide to form silicon oxynitride.

H01L 21/02334

{in-situ cleaning after layer formation, e.g. removing process residues}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Subject matter relating to cleaning processes for semiconductor device fabrication	H01L 21/02041
Cleaning in general	B08B
Cleaning compositions in general	**C30D**

H01L 21/02365

{Forming inorganic semiconducting materials on a substrate}

Definition statement

This place covers:

Processes for the formation of inorganic semiconductors on a substrate.

Processes for forming doped inorganic semiconductors.

In situ pre-and post-treatments of inorganic semiconductor materials.

Processes for the formation of multiple layers of inorganic semiconductors, comprising heterostructures.

The formed semiconductor layer may be crystalline (mono-, poly-, microcrystalline) or amorphous.

Relationships with other classification places

Attention is drawn to the groups C23C, C25D, C30B and their subdivisions for general aspects of these techniques.

References

Limiting references

This place does not cover:

Nanosized carbon materials, e.g. fullerenes, carbon nanotubes	C01B 32/15
Processes for forming layers only characterized by the purely chemical aspects of the used precursors	C23C, C30B

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of inorganic semiconductors for light	H10F 71/00
Processes specially adapted for the manufacture or treatment of organic semiconductor or solid state devices or of parts thereof	H10K 71/00
Fullerenes used in semiconductor or solid state devices	H10K 85/211

H01L 21/02606

{Nanotubes (carbon nanotubes H10K 85/211)}

References

Limiting references

This place does not cover:

Carbon nanotubes used in semiconductor or solid state devices	H10K 85/221

H01L 21/02658

{Pretreatments (cleaning in general H01L 21/02041)}

References

Limiting references

This place does not cover:

Ex situ cleaning	H01L 21/02041

H01L 21/02664

{Aftertreatments (planarisation in general H01L 21/304)}

References

Limiting references

This place does not cover:

After-treatments for improving the planarity of the layers, e.g. thermal smoothening of layers	H01L 21/324

H01L 21/02697

{Forming conducting materials on a substrate}

Special rules of classification

This group is not used for classification; subject matter relating to the formation of conductive material on a semiconductor substrate is classified in H01L 21/283 - H01L 21/288, H01L 21/3205 and H01L 21/768.

H01L 21/027

Making masks on semiconductor bodies for further photolithographic processing not provided for in group H01L 21/18 or H01L 21/34 {(photographic masks or originals per se G03F 1/00; registration or positioning of photographic masks or originals G03F 9/00; photographic cameras G03B; control of position G05D 3/00)}

Definition statement

This place covers:

Formation of masks to be used for etching or patterning, formed out of a layer formed or deposited on the wafer. Includes inorganic masks (metallic or insulating materials) as well as organic masks.

Relationships with other classification places

Composition of photosensitive polymers, see G03F 7/00.

Photographic masks of the stencil tape or originals per se: G03F 1/00

Registration or positioning of photographic masks or originals: G03F 9/00

Photographic cameras G03B

Control of position G05D 3/00

References

Limiting references

This place does not cover:

masks for selective growth	H01L 21/02639
masks for implantation	H01L 21/266
masks for forming insulating layers	H01L 21/322

Formation and use of stencil masks	G03F 1/00
Masks per se, e.g. free standing mask, stencil mask	G03F 1/86, G03F 7/12
Formation of photoresist masks per se	G03F 7/00
Formation of masks for non patterning purposes:	

Informative references

Attention is drawn to the following places, which may be of interest for search:

Photographic cameras	G03B
Photographic masks or originals per se	G03F 1/00
Registration or positioning of photographic masks or originals	G03F 9/00
Control of position	G05D 3/00

Special rules of classification

In main group H01L 21/00 and subgroup thereof, a mask is defined as a layer, which is coated directly onto the surface of the wafer.

A free standing mask (stencil mask) laid on the wafer is not considered as a mask in the sense of H01L 21/00.

Masks are classified in H01L 21/00 only under the condition that its treatment or structure has been specially adapted to the fabrication of a device covered by H01L 21/00. Examples are:

- masks used for more than one technological step during device fabrication,
- masks whose structure, formation or treatment are adapted to the nature of the layers or materials used in the fabrication of semiconductor device, or to the device itself

H01L 21/0271

{comprising organic layers}

Definition statement

This place covers:

Covers polymeric masks, including photo-sensitive masks (photoresist) as well as non photo-sensitive masks, e.g., wax, polyimide etc.

H01L 21/0273

{characterised by the treatment of photoresist layers}

Definition statement

This place covers:

Treatment of photoresist layers peculiar to fabrication of electronic devices.

H01L 21/0273 covers the treatment of photoresist which is not peculiar to the type of resist (UV, e-beam, ion beam resist), for example:

- method of reflowing the resist,
- method of hardening the resist

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Photoresists and processing of photoresists in general	G03F 7/00

Special rules of classification

- If the treatment is peculiar to the resist type (light, e-beam or ion-beam resist), then it is classified in the corresponding subgroup. If not, remains in H01L 21/0273.
- Chemical amplification is considered to be peculiar to the resist type.
- fabricating masks by irradiating a resist with different types of radiation, e.g. photons and electrons, the document is classified in H01L 21/0273.

H01L 21/0276

{using an anti-reflective coating (anti-reflective coating for lithography in general G03F 7/09)}

Definition statement

This place covers:

Anti-reflective coatings specially adapted for devices as defined under H01L 21/00.

Covers organic as well as inorganic anti-reflective coatings

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Antireflective coatings for lithography in general	G03F 7/091

H01L 21/0277

{Electrolithographic processes}

Definition statement

This place covers:

Multilayer structures and special structures adapted to evacuate charges, e.g. multilayer resists with a conductive layer.

Special rules of classification

Multilayer resists for electrolithography should additionally be classified in G03F 7/00.

H01L 21/0278

{Röntgenlithographic or X-ray lithographic processes}

Definition statement

This place covers:

Includes multilayer structures.

Special rules of classification

Multilayer resists for Röntgenlithography should additionally be classified in G03F 7/00

H01L 21/033

comprising inorganic layers

Definition statement

This place covers:

Processes for forming masks comprising inorganic layers.

Special rules of classification

This group H01L 21/033 acts as a head group for inorganic masks for patterning layers. Multiple classification with H01L 21/31144 (masks for etching insulating layers), H01L 21/32139 (masks for etching conductive layers and polysilicon layers) and H01L 21/308 (masks for etching semiconductors) is possible.

H01L 21/0331

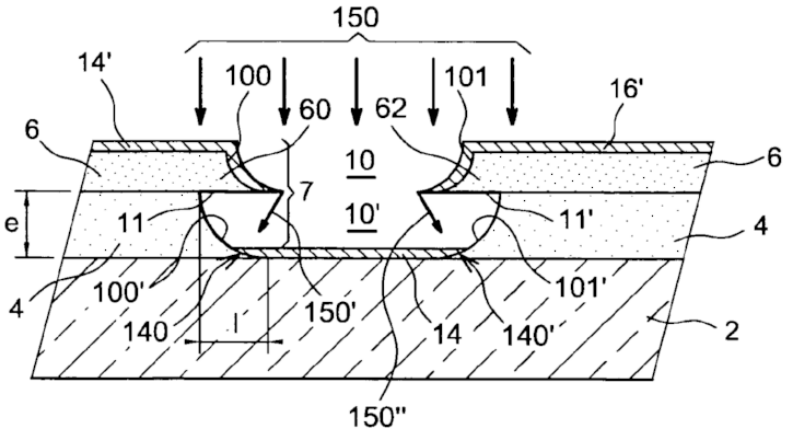
{for lift-off processes}

Definition statement

This place covers:

Processes for forming masks to be used for lifting off another layer (for example having a multilayer structure or special profile) irrespective of their fabrication process

Example:



EP2132770

References

Limiting references

This place does not cover:

Lifting off for obtaining the mask	H01L 21/0337

H01L 21/0335

{characterised by their behaviour during the process, e.g. soluble masks, redeposited masks}

Definition statement

This place covers:

Mask having a shape being directly affected by and during the patterning process, e.g. erosion or re-deposition, such that the shape of the mask changes during the patterning process.

H01L 21/0337

{characterised by the process involved to create the mask, e.g. lift-off masks, sidewalls, or to modify the mask, e.g. pre-treatment, post-treatment}

Definition statement

This place covers:

Processes for forming masks involving special processes, like lift-off, or sidewall formation, e.g. deposition on a step followed by anisotropic etching, or to modify the mask, e.g. oxidation of an Aluminium layer, hardening, before etching step.

H01L 21/0338

{Process specially adapted to improve the resolution of the mask}

Definition statement

This place covers:

Process specially adapted to provide a mask below the lithographic resolution limit.

Special rules of classification

Sidewall masks may also be classified in H01L 21/0337. As a sidewall spacer has inherently a sub lithographic size, it does not require an automatic group symbol here.

H01L 21/04

the devices having potential barriers, e.g. a PN junction, depletion layer or carrier concentration layer

Definition statement

This place covers:

The group range from H01L 21/04 - H01L 21/326 covers processes for fabrication of semiconductor devices on substrates belonging to the semiconductors of

- group IV: Si, Ge,
- group IV: carbon, diamond,
- group III-V: GaAs, GaN, InP etc.
- group IV-IV: Silicon Carbide,
- inorganic semiconductors other than the above mentioned materials, e.g. II-VI semiconductors,
- bonding or joining semiconductor bodies
- diffusion, and alloying of impurities in these semiconductor materials
- bombardment of these semiconductor materials with radiation,

- Manufacture of electrodes on these semiconductor materials,
- special treatments of these semiconductor materials, like

thermal treatments, e.g. gettering

electroforming

mechanical treatments of these semiconductor materials

hydrogenation of these materials

treatments of insulating layers formed on these materials, including planarisation, etching,

deposition conductive or resistive layers on these semiconductor materials

treatment of these conductive layers, like planarisation, oxidation, etching, doping,

treatment of the insulating or conductive layers formed thereon,

planarisation of these semiconductor materials, or of the insulating and conductive layers formed thereon

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of insulating layers on semiconductor wafers and the direct post-treatment of this formation	H01L 21/02107
Formation of SOI	H01L 21/7624
Multistep manufacturing processes for said devices	H10D 1/01, H10D 8/01, H10D 10/01, H10D 12/01, H10D 18/01, H10D 30/01, H10D 44/01, H10D 48/01
Multistep manufacturing processes for semiconductor bodies of said devices	H10D 62/01
Multistep manufacturing processes for electrodes of said devices	H10D 64/01

Special rules of classification

The presence of a potential jump barrier need not to be specified. Inventions intended to be used in the fabrication of devices having a potential barrier may be classified under H01L 21/04.

H01L 21/0405

{the devices having semiconductor bodies comprising semiconducting carbon, e.g. diamond, diamond-like carbon}

Definition statement

This place covers:

Passivation of semiconducting carbon, e.g. diamond

References

Limiting references

This place does not cover:

Fullerenes, e.g. C60, C70	H10K 85/211
Carbon nanotubes	H10K 85/221

Special rules of classification

Processes for fabricating devices having bodies of diamond not covered by H01L 21/041 - H01L 21/0425 are classified in H01L 21/18 - H01L 21/326 and are also mandatoril y classified in H10D 62/8303 as invention information or additional information whenever appropriate.

H01L 21/0445

{the devices having semiconductor bodies comprising crystalline silicon carbide}

References

Limiting references

This place does not cover:

Preparation of SiC wafers	H01L 21/02002
Etching, polishing of semiconducting SiC	H01L 21/304 - H01L 21/3065

Special rules of classification

Processes for fabricating devices having bodies comprising crystalline silicon carbide not covered by H01L 21/045 - H01L 21/048 are classified in H01L 21/18 - H01L 21/326 and are also mandatorily classified in H10D 62/8325 as invention information or additional information whenever appropriate.

H01L 21/046

{using ion implantation}

Definition statement

This place covers:

Processes where ion implantation of boron and subsequent annealing does produce a p-doped region in a silicon carbide.

Special rules of classification

Processes where ion implantation of boron and subsequent annealing does not produce a p-doped region are classified elsewhere, e.g. H01L 21/0445

H01L 21/18

the devices having semiconductor bodies comprising elements of Group IV of the Periodic Table or $A_{III}B_{V}$ compounds with or without impurities, e.g. doping materials {(H01L 21/041 - H01L 21/0425, H01L 21/045 - H01L 21/048 take precedence)}

Definition statement

This place covers:

Processes and apparatus which, by using the appropriate technology, are clearly suitable for manufacture or treatment of devices whose bodies comprise elements of the fourth group of the Periodic Table or AIII-BV compounds, even if the material used is not explicitly specified.

References

Limiting references

This place does not cover:

Making n- or p-doped regions for devices having semiconductor bodies of diamond; Changing their shape; Making electrodes	H01L 21/041 - H01L 21/0425
Making n- or p-doped regions for devices having semiconductor bodies comprising crystalline silicon carbide; Changing their shape; Making electrodes; Passivating silicon carbide surfaces	H01L 21/045 - H01L 21/048

H01L 21/185

{Joining of semiconductor bodies for junction formation}

Definition statement

This place covers:

Joining through a metal layer or eutectic layer.

References

Limiting references

This place does not cover:

Joining/bonding of semiconductor bodies through an oxide layer	H01L 21/762

H01L 21/187

{by direct bonding}

Definition statement

This place covers:

Direct bonding of semiconductor bodies without intermediate layer

H01L 21/22

Diffusion of impurity materials, e.g. doping materials, electrode materials, into or out of a semiconductor body, or between semiconductor regions; {Interactions between two or more impurities; Redistribution of impurities}

Definition statement

This place covers:

Plasma doping.

Special rules of classification

Plasma doping is considered as doping from a gas phase, as is the case in Plasma Immersion Ion Implantation. Nevertheless, plasma doping can have ion implantation aspects like the type of ions. These aspects should be classified in ion implantation, H01L 21/265. But a group symbol e.g. H01L 21/2236 or an index code e.g. H01L 21/2236 should always be allocated to track the fact it uses a plasma.

H01L 21/223

using diffusion into or out of a solid from or into a gaseous phase {(H01L 21/221 - H01L 21/222 take precedence; diffusion through an applied layer H01L 21/225)}

References

Limiting references

This place does not cover:

Diffusion of killers	H01L 21/221
Lithium-drift	H01L 21/222

Informative references

Attention is drawn to the following places, which may be of interest for search:

Diffusion through an applied layer	H01L 21/225

H01L 21/225

using diffusion into or out of a solid from or into a solid phase, e.g. a doped oxide layer {(H01L 21/221 - H01L 21/222 take precedence)}

References

Limiting references

This place does not cover:

Diffusion of killers	H01L 21/221
Lithium-drift	H01L 21/222

H01L 21/2254

{from or through or into an applied layer, e.g. photoresist, nitrides}

Special rules of classification

In the range H01L 21/2254 - H01L 21/2257 the main compositional part of the applied layer just before the diffusion step has to be considered for classification

H01L 21/228

using diffusion into or out of a solid from or into a liquid phase, e.g. alloy diffusion processes {(H01L 21/221 - H01L 21/222 take precedence)}

References

Limiting references

This place does not cover:

Diffusion of killers	H01L 21/221
Lithium-drift	H01L 21/222

H01L 21/24

Alloying of impurity materials, e.g. doping materials, electrode materials, with a semiconductor body {(H01L 21/182 takes precedence)}

References

Limiting references

This place does not cover:

Intermixing, interdiffusion or disordering of AIII-BV heterostructures	H01L 21/182

H01L 21/26

Bombardment with radiation {(H01L 21/3105 takes precedence)}

References

Limiting references

This place does not cover:

Bombardment with radiation as post-treatment of an insulating layer	H01L 21/3105

H01L 21/263

with high-energy radiation (H01L 21/261 takes precedence)

References

Limiting references

This place does not cover:

High energy radiation creating a nuclear transmutation	H01L 21/261

Special rules of classification

There is no exact border defining high energy. It is meant to cover alpha, beta, gamma, Röntgen... rays. The sub group H01L 21/2633 is incorrectly placed as a subgroup.

H01L 21/265

producing ion implantation

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thermal treatment for modifying the properties of semiconductor bodies per se	H01L 21/324
Ion beam tubes for localised treatment	H01J 37/30

H01L 21/266

using masks {(H01L 21/26586 takes precedence)}

References

Limiting references

This place does not cover:

Crystal planes or main crystal surface and ion beam present an angle	H01L 21/26586

H01L 21/28

Manufacture of electrodes on semiconductor bodies using processes or apparatus not provided for in groups H01L 21/20 - H01L 21/268

Definition statement

This place covers:

Includes processes for forming

- conductor-semiconductor,
- conductor-insulator-semiconductor, or
- conductor-insulator-conductor-insulator-semiconductor structures.

Multistep processes for manufacturing electrodes on semiconductor bodies characterised by

- a sequence of single steps, possibly including steps like deposition conductive material, alloying, silicidation,
- the structure or the shape of the electrode.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Diffusion of dopants	H01L 21/22
Alloying of electrode materials	H01L 21/24
Implantation of dopants	H01L 21/265
Etching the insulating layers	H01L 21/311
Physical or chemical etching of the layers	H01L 21/3213
Depositing or patterning electrodes for capacitors	H10D 1/042, H10D 1/043
Manufacturing electrodes for devices having potential barriers	H10D 64/01

Special rules of classification

Formation of electrodes only involving an etching of conductive materials, including silicide on polysilicon: H01L 21/3213 and subgroups.

Information peculiar to single-step processes should also be classified in the corresponding group, e.g.

- H01L 21/311 or H01L 21/3213 for etching,
- H01L 21/027, H01L 21/033, H01L 21/31144 or H01L 21/32139 for masking,
- H01L 21/3105 or H01L 21/321 for planarising.

H01L 21/28008

{Making conductor-insulator-semiconductor electrodes}

Definition statement

This place covers:

Processes for the fabrication of conductor-insulator-semiconductor structure, e.g. wherein the conductor is part of the interconnect (gate level interconnect).

References

Limiting references

This place does not cover:

Monosteps for forming insulators or conductors for which the application to gate electrodes is mentioned without further details.	H01L 21/02104, H01L 21/283

H01L 21/28017

{the insulator being formed after the semiconductor body, the semiconductor being silicon}

Definition statement

This place covers:

Deposition of the insulators, using epitaxiy

Deposition of the conductor and the insulator within the same process chamber.

H01L 21/28026

{characterised by the conductor (H01L 21/28176 takes precedence)}

References

Limiting references

This place does not cover:

Annealing, after the formation of the definitive gate conductor	H01L 21/28176

Special rules of classification

When the final conductor comprises a superconductor, subject matter is not classified according to H01L 21/28035 - H01L 21/28097, but instead it is classified in H01L 21/28026.

H01L 21/28035

{the final conductor layer next to the insulator being silicon, e.g. polysilicon, with or without impurities (H01L 21/28105 takes precedence)}

References

Limiting references

This place does not cover:

the final conductor next to the insulator having a lateral composition or doping variation, or being formed laterally by more than one deposition step	H01L 21/28105

Special rules of classification

A very thin, e.g. silicon, adhesion or seed layer is not considered as the one next to the insulator

H01L 21/28052

{the conductor comprising a silicide layer formed by the silicidation reaction of silicon with a metal layer (formed by metal ion implantation H01L 21/28044)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Silicide formed by metal ion implantation	H01L 21/28044

Special rules of classification

To assess the coverage of groups H01L 21/28052 and H01L 21/28061, barrier layers, e.g. TaSiN, are not considered]

H01L 21/28061

{the conductor comprising a metal or metal silicide formed by deposition, e.g. sputter deposition, i.e. without a silicidation reaction (H01L 21/28052 takes precedence)}

References

Limiting references

This place does not cover:

Conductors comprising a silicide layer formed by the silicidation reaction of silicon with a metal layer	H01L 21/28052

Special rules of classification

To assess the coverage of groups H01L 21/28052 and H01L 21/28061, barrier layers, e.g. TaSiN, are not considered]

H01L 21/28114

{characterised by the sectional shape, e.g. T, inverted-T}

Special rules of classification

Documents are also classified in groups H01L 21/28035 - H01L 21/28105 when the composition is also relevant

H01L 21/28123

{Lithography-related aspects, e.g. sub-lithography lengths; Isolation-related aspects, e.g. to solve problems arising at the crossing with the side of the device isolation; Planarisation aspects}

References

Limiting references

This place does not cover:

Fabrication of lithographic masks for electrodes	H01L 21/027, H01L 21/033

Informative references

Attention is drawn to the following places, which may be of interest for search:

Lift-off aspects involving multilayer masks	H01L 21/0272 or H01L 21/0331

H01L 21/28158

{Making the insulator}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Forming insulating materials on a substrate	H01L 21/02107

Special rules of classification

In case the formation of the insulator would be of general interest, a group symbol should be given in H01L 21/02107.

H01L 21/28185

{with a treatment, e.g. annealing, after the formation of the gate insulator and before the formation of the definitive gate conductor}

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

RTN	Rapid Thermal Nitridation
RPN	Rapid Plasma Nitridation

H01L 21/28211

{in a gaseous ambient using an oxygen or a water vapour, e.g. RTO, possibly through a layer (H01L 21/28194 and H01L 21/28202 take precedence)}

References

Limiting references

This place does not cover:

Evaporation, ALD, CVD, sputtering, laser deposition	H01L 21/28194
Nitride deposition, growth, oxynitridation, NH_3 nitridation, N_2O oxidation, thermal nitridation, RTN, plasma nitridation, RPN	H01L 21/28202

Special rules of classification

Thin oxidation layers used as a barrier layer or as a buffer layer, e.g. before the fomation of a high-k insulator, are classified here only if important per se.

H01L 21/28229

{by deposition of a layer, e.g. metal, metal compound or poysilicon, followed by transformation thereof into an insulating layer}

Special rules of classification

In case the transformation would be of general interest it should be classified in

- H01L 21/32105 or H01L 21/3211,
- H01L 21/02107.

H01L 21/283

Deposition of conductive or insulating materials for electrodes {conducting electric current}

Definition statement

This place covers:

H01L 21/283 - H01L 21/2885 cover the deposition of conductive layers directly in contact with the semiconductor for forming electrodes.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of electrodes of capacitors, resistors, inductors	H10D 1/01
Formation of electrodes of semiconductor devices	H10D 64/01

Special rules of classification

Application to contacts must be mentioned with details. Moreover, details of deposition processes of conductive layers covered by H01L 21/3205 are additionally classified in this group and subgroups thereof. If a document discloses information relevant for any of the groups H01L 21/768 - H01L 21/76898, one or more of these groups should also be assigned.

H01L 21/285

from a gas or vapour, e.g. condensation

Definition statement

This place covers:

Methods for depositing conductive layers using gases or vapours of metals or metal-containing precursors.

References

Limiting references

This place does not cover:

Deposition of polysilicon in contact with a semiconductor	H01L 21/02365
Formation of electrodes of capacitors, resistors, inductors	H01L 21/28

Informative references

Attention is drawn to the following places, which may be of interest for search:

Chemical coating by decomposition of gaseous compounds, without leaving reaction products of surface material in the coating, i.e. chemical vapour deposition (CVD) processes	C23C 16/00

Special rules of classification

The deposition process (PVD, CVD, ALD etc.) must be specially adapted for forming contacts or interconnects within semiconductor devices and must be disclosed in detail, i.e. include details on deposition parameters, precursor materials, particular apparatus details etc.

If a document discloses information relevant for any of the groups H01L 21/768 - H01L 21/76898, one or more of these groups should also be assigned.

H01L 21/28525

{the conductive layers comprising semiconducting material (H01L 21/28518, H01L 21/28537 take precedence)}

References

Limiting references

This place does not cover:

Conductive layers comprising silicides	H01L 21/28518
Deposition of Schottky electrodes	H01L 21/28537

Special rules of classification

Deposition of polysilicon on silicon classified there only if application to contacts is mentioned. Otherwise H01L 21/02365

H01L 21/28531

{Making of side-wall contacts}

Special rules of classification

Deposition of polysilicon on silicon classified there only if application to contacts is mentioned. Otherwise H01L 21/02365

H01L 21/288

from a liquid, e.g. electrolytic deposition

Definition statement

This place covers:

The deposition of conductive layers directly in contact with semiconductors for forming electrodes using liquid deposition techniques, e.g. electroless plating.

References

Limiting references

This place does not cover:

Formation of electrodes of capacitors, resistors, inductors	H01L 21/28

Informative references

Attention is drawn to the following places, which may be of interest for search:

Chemical coating by decomposition of either liquid compounds or solutions of the coating forming compounds, without leaving reaction products of surface material in the coating	C23C 18/00

Special rules of classification

The deposition process must be specially adapted for forming contacts or interconnects within semiconductor devices and must be disclosed in detail, i.e. include details on deposition parameters, precursor materials, particular apparatus details etc.

If a document discloses information relevant for any of the groups H01L 21/768 - H01L 21/76898, one or more of these groups should also be assigned.

H01L 21/30

Treatment of semiconductor bodies using processes or apparatus not provided for in groups H01L 21/20 - H01L 21/26 (manufacture of electrodes thereon H01L 21/28)

Definition statement

This place covers:

- mechanical treatments, like grinding, sand blasting etc.
- hydrogenation of these semiconductors
- chemical treatments, like etching,

- formation of insulating layers and after treatment of these layers, like planarisation, etching, formation of conductive layers on these insulating layers and after treatment of these conductive layers and their doping.

References

Limiting references

This place does not cover:

the treatment of II-VI compounds	H01L 21/02365
the treatment of insulating layers	H01L 21/31
the treatment of metallic	H01L 21/3205

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture of electrodes thereon	H01L 21/28

H01L 21/304

Mechanical treatment, e.g. grinding, polishing, cutting {(H01L 21/30625 takes precedence)}

Definition statement

This place covers:

Mechanical treatment of semiconductor wafers or semiconductor layers, except the mechanical treatment of insulating or conductive layers on semiconductor wafers.

Relationships with other classification places

Mechanical treatment in general:

- grinding, polishing B24B,
- abrasive blasting B24C

References

Limiting references

This place does not cover:

Polishing of semiconductor wafers	H01L 21/0201
Polishing of epitaxial layers on semiconductor wafers	H01L 21/30625
Mechanical treatment of insulating	H01L 21/3205
Conductive layers on wafers	H01L 21/321
Single step mechanical operations, like sawing, polishing, breaking etc. classified in the corresponding group in section B	B24B, B24C

Special rules of classification

The mere use of a machine is classified with the machine only.

Process for the mechanical treatment, enhanced by chemical treatment, is classified in chemical treatment, but may be given a group symbol in mechanical treatment if the mechanical treatment itself is of importance for the invention.

Purely mechanical polishing is considered as chemical-mechanical polishing, and is classified accordingly.

H01L 21/3043

{Making grooves, e.g. cutting}

Definition statement

This place covers:

Making grooves, which may result in cutting

References

Limiting references

This place does not cover:

Singulation of wafers into dies	H01L 21/78

H01L 21/306

Chemical or electrical treatment, e.g. electrolytic etching (to form insulating layers H01L 21/31)

Definition statement

This place covers:

- Chemical or electrical treatment of group IV or III-V semiconductors.
- Formation of porous semiconductors,
- Functionalisation of semiconductor surfaces

References

Limiting references

This place does not cover:

Chemical or electrical treatment to form insulating layers	H01L 21/31

H01L 21/30608

{Anisotropic liquid etching (H01L 21/3063 takes precedence)}

Definition statement

This place covers:

Anisotropic liquid etching, i.e. "crystal orientation dependant" etching, using basic (pH>7) compositions. The etch composition is often composed of KOH, amines, azines, quaternary ammonium compounds

References

Limiting references

This place does not cover:

Electrolytic etching	H01L 21/3063
Anisotropic etching for tartarising surfaces	H10F 71/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Etching for fabrication of MEMs.	B81C 1/00539

H01L 21/30621

{Vapour phase etching}

Definition statement

This place covers:

Reactive Ion Etching [RIE] of III-V

H01L 21/30625

{With simultaneous mechanical treatment, e.g. mechanico-chemical polishing}

Definition statement

This place covers:

Processes for polishing semiconductors not being part of the sequence for preparing wafers from an ingot (H01L 21/02013 or H01L 21/02024).

Covers polishing or CMP of semiconductor layers deposited on a substrate, like epitaxial layers.

References

Limiting references

This place does not cover:

Polishing or CMP of bulk wafers, wherein the polishing is part of the sequence for preparing wafers from an ingot	H01L 21/02013, H01L 21/02024
Polishing or CMP of insulating layers	H01L 21/31053
Polishing or CMP of conductive layers	H01L 21/3212

Special rules of classification

Chemical-mechanical polishing also includes purely mechanical polishing.

H01L 21/3063

Electrolytic etching

References

Limiting references

This place does not cover:

formation of porous materials by electrolysis	H01L 21/306

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electrolytic etching in general	C25F 3/12

H01L 21/3065

Plasma etching; Reactive-ion etching

Definition statement

This place covers:

- sputter etching,
- particle (electron, ion, photon) beam enhanced etching
- light assisted etching.
- plasma etching
- dry etching, i.e. using an etching gas without plasma

References

Limiting references

This place does not cover:

Reactive ion etching of III-V materials	H01L 21/30621

Informative references

Attention is drawn to the following places, which may be of interest for search:

Laser etching without reactive atmosphere per se	B23K 26/00

H01L 21/308

using masks (H01L 21/3063, H01L 21/3065 take precedence)

Definition statement

This place covers:

- Masks used for patterning semiconductors of group IV or III-V, including masks used for plasma etching/patterning, excepted masks for electrolytic etching.
- The fabrication of masks to be used for etching or patterning semiconductors (non-monocrystalline semiconductors being excluded).

References

Limiting references

This place does not cover:

Formation of masks for non patterning purposes, which are classified with the step in question: - masks for implantation - masks for forming insulating layers, - masks for selective growth, - masks for patterning semiconductors belonging to groups other than group IV and group III-V.	H01L 21/266, H01L 21/32, H01L 21/02639
Electrolytic etching	H01L 21/3063
Formation and use of stencil masks	G03F 1/00
Free standing masks, e.g. stencil masks	G03F 1/86 or G03F 7/12
Formation of photoresist masks per se, except if the formation of the photoresist mask is specific to the device to be fabricated or semiconductor substrate	G03F 7/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

General masks for patterning in the fabrication of semiconductor device	H01L 21/033
Masks for patterning insulating layers	H01L 21/31144
Masks for patterning conductors, including polycrystalline or amorphous silicon	H01L 21/32139

Special rules of classification

A mask in H01L 21/00 is formed of a layer coated directly onto the surface of the wafer.

A free standing mask (stencil mask) laid on the wafer is not considered as a mask in the sense of H01L 21/00.

Masks are classified in H01L 21/308 only under the condition that its treatment or structure has been specially adapted to the fabrication of a device covered by H01L 21/00. Examples are:

- masks used for more than one technological step during device fabrication,
- masks whose structure, formation or treatment are adapted to the nature of the layers or materials used in the fabrication of semiconductor device, or to the device itself

The takes precedence rule (stemming from IPC) pointing to H01L 21/3065 is not valid for CPC: masks for etching by plasma or reactive ion etching are given a group symbol here.

Masks for electrolytic etching are classified with the electrochemical etching in H01L 21/3063.

Using stencil masks for ion implantation is classified in H01L 21/266.

H01L 21/3085

{characterised by their behaviour during the process, e.g. soluble masks, redeposited masks}

Definition statement

This place covers:

Masks having a specific behaviour during etching process. e.g. erodible mask, shrinking mask etc.

References

Limiting references

This place does not cover:

Processes wherein the etching is interrupted to modify the mask (sequential etching), e.g. etching, followed by modifying the mask, followed by re-etching, with possible cycling of the above steps	H01L 21/30604, H01L 21/30625, H01L 21/3063, H01L 21/3065

H01L 21/3086

{characterised by the process involved to create the mask, e.g. lift-off masks, sidewalls, or to modify the mask, e.g. pre-treatment, post-treatment}

Definition statement

This place covers:

Covers pre-treatment for the formation of a mask, post treatment of the mask before etching, treatments to modify the mask before use, e.g. hardening, formation of sidewalls, multiple sidewalls etc.

References

Limiting references

This place does not cover:

Modification of the mask during etching	H01L 21/3085
Removal of the mask after use	H01L 21/31144

Informative references

Attention is drawn to the following places, which may be of interest for search:

Photoresist for lift	H01L 21/0272
Inorganic masks for lift-off	H01L 21/0331

H01L 21/3088

{Process specially adapted to improve the resolution of the mask}

Definition statement

This place covers:

Process specially adapted to go below resolution limit of lithography.

H01L 21/31

to form insulating layers thereon, e.g. for masking or by using photolithographic techniques (encapsulating layers H01L 21/56); After treatment of these layers; Selection of materials for these layers

Definition statement

This place covers:

Processes for forming insulating layers and their direct post-treatment.

To be used in any process, formation of interconnects, isolation oxides etc.when the invention is focussed on the insulator.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Insulating layers forming part of electrodes	H01L 21/28
Encapsulating layers	H01L 21/56

H01L 21/3105

After-treatment

Definition statement

This place covers:

Covers special treatments of insulating layers, wherein the special treatment is not a post-treatment as defined under H01L 21/00, i.e. the classical annealing of the insulating layer to improve its characteristics, but is for example

planarisation, patterning, functionalization after etching.

References

Limiting references

This place does not cover:

Classical annealing after formation of the insulator, classified together with the formation	H01L 21/02318

Special rules of classification

Functionalization just after formation should be classified with the formation.

In case the process would also be of interest as a post treatment, both classes should be given.

H01L 21/31051

{Planarisation of the insulating layers (H01L 21/31058 takes precedence)}

Definition statement

This place covers:

- Planarisation of insulating layers.
- Atomic scale planarisation (smoothening) of the insulating layers.
- Reflow of insulating layers.

References

Limiting references

This place does not cover:

After treatment, e.g. planarisation, of organic layers	H01L 21/31058

H01L 21/31053

{involving a dielectric removal step}

Definition statement

This place covers:

Planarisation involving a removal step not being a chemical etch step: this is the group for polishing and chemical-mechanical polishing (CMP) of insulating materials.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Polishing slurries	C09G, C09K

H01L 21/31055

{the removal being a chemical etching step, e.g. dry etching (etching per se H01L 21/311)}

Definition statement

This place covers:

Planarisation by non selective etching, e.g. by a blanket etching reducing the protrusions.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Etching per se	H01L 21/311

H01L 21/31056

{the removal being a selective chemical etching step, e.g. selective dry etching through a mask}

Definition statement

This place covers:

Processes where protrusions are selectively etched through a mask.

H01L 21/31105

{Etching inorganic layers}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Etching glass	C03C 15/00

H01L 21/31111

{by chemical means}

Definition statement

This place covers:

Etching by wet process, or by processes wherein gaseous reactants are condensed on the surface.

Special rules of classification

Gaseous etch with HF is classified in H01L 21/31116

H01L 21/31116

{by dry-etching}

Definition statement

This place covers:

- Plasma etching
- Ion beam etching

H01L 21/31127

{Etching organic layers}

Definition statement

This place covers:

Removal of organic layers or polymers, including photoresists peculiar to semiconductor wafers or devices.

References

Limiting references

This place does not cover:

The removal of silicon-containing compounds having an organic nature.	H01L 21/31105

Informative references

Attention is drawn to the following places, which may be of interest for search:

Removal of photoresist not peculiar to semiconductor wafers	G03F 7/42

Special rules of classification

Removal of photoresist being not peculiar to semiconductors is classified in G03F 7/42.

Peculiar to semiconductor devices means that particular precautions are taken to avoid influence of the removal of the photoresist on the semiconductor wafer or device.

H01L 21/31133

{by chemical means}

Definition statement

This place covers:

Etching by wet process, or by processes wherein gaseous reactants are condensed on the surface.

H01L 21/31144

{using masks}

Definition statement

This place covers:

Etching involving a specially adapted mask

Special rules of classification

In case the mask would be of general interest, it should also be classified in H01L 21/033

H01L 21/3115

Doping the insulating layers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

See also after treatment of insulating layers	H01L 21/3105
Doping with the purpose to alter resistivity or increase conductivity	H01L 21/76888

Special rules of classification

Implantation or diffusion into insulating layers is also classified under H01L 21/02318 and subgroups.

H01L 21/312 (Frozen)

Organic layers, e.g. photoresist (H01L 21/3105, H01L 21/32 take precedence; {photoresists per se G03C})

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Photoresists per se	G03C

Special rules of classification

H01L 21/312 - H01L 21/3128 are no longer used for classification of new documents, see H01L 21/02112.

H01L 21/314 (Frozen)

Inorganic layers (H01L 21/3105, H01L 21/32 take precedence)

Special rules of classification

H01L 21/314 - H01L 21/3185 are no longer used for classification of new documents. See H01L 21/02112.

H01L 21/3205

Deposition of non-insulating-, e.g. conductive- or resistive-, layers on insulating layers; After-treatment of these layers (manufacture of electrodes H01L 21/28)

Definition statement

This place covers:

Deposition of conductive layers exclusively on insulating layers, when the process of deposition is relevant.

References

Limiting references

This place does not cover:

Deposition of conductive layers on semiconductor	H01L 21/283 - H01L 21/288

Special rules of classification

When the technique of deposition is particular (CVD, PVD or electroplating), also classify in H01L 21/283, H01L 21/285 or H01L 21/288. When an interconnection is concerned, see also H01L 21/768 and subgroups.

H01L 21/321

After treatment

Definition statement

This place covers:

Treatment of formed conductive layers. Includes:

- etching by chemical or physical means,
- planarisation, including chemical-mechanical polishing,
- oxidation, nitridation, or surface treatment,
- doping.

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups.

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. After treatment of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32105

{Oxidation of silicon-containing layers}

Definition statement

This place covers:

Oxidation of non-monocrystalline silicon, e.g. polycrystalline, microcrystalline or amorphous silicon.

References

Limiting references

This place does not cover:

Oxidation of monocrystalline silicon	H01L 21/02236

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Oxidation of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/3211

{Nitridation of silicon-containing layers}

Definition statement

This place covers:

Nitridation of non-monocrystalline silicon, e.g. polycrystalline, microcrystalline or amorphous silicon.

References

Limiting references

This place does not cover:

Nitridation of monocrystalline silicon	H01L 21/02247

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Nitridation of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32115

{Planarisation}

Definition statement

This place covers:

Planarisation of conductive or resistive layers.

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Planarisation of these layers is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/3212

{by chemical mechanical polishing [CMP]}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

CMP slurries	C09G

H01L 21/3213

Physical or chemical etching of the layers, e.g. to produce a patterned layer from a pre-deposited extensive layer

Definition statement

This place covers:

Physical or chemical etching of conductive or resistive layers.

Etching of polysilicon layers

Etching of amorphous silicon layers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Machines or apparatus for liquid etching	H01L 21/67
Machines for plasma etching	H01J 37/00

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Etching of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32131

{by physical means only}

Definition statement

This place covers:

Etching processes, where no chemical reaction is involved, e.g.

sputtering, ion milling, laser ablation, pure ion beam etching.

Special rules of classification

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32132

{of silicon-containing layers}

Definition statement

This place covers:

Silicides and silicon alloys.

H01L 21/32133

{by chemical means only}

Definition statement

This place covers:

Use of Plasmas, e.g. RIE, and chemically assisted particle (ion or electron, photon) beam etching

Special rules of classification

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32134

{by liquid etching only}

Definition statement

This place covers:

Etching with supercritical fluids

H01L 21/32136

{using plasmas}

Definition statement

This place covers:

Etching assisted by electrons, ions and laser beams.

H01L 21/32137

{of silicon-containing layers}

Definition statement

This place covers:

Polysilicon, amorphous, silicides, multilayers containing silicon

H01L 21/32138

{pre- or post-treatments, e.g. anti-corrosion processes}

Definition statement

This place covers:

Pre-treatments before etching, including removal of natural oxide.

Anti-corrosion post-treatments.

References

Limiting references

This place does not cover:

Post-treatment after etching, e.g. RIE	H01L 21/02041

Special rules of classification

In case the pre-treatment is a removal of natural oxide and is of general interest, a group symbol in H01L 21/02041 should be given.

In case the post treatment is a passivation by oxidation or nitridation this step should be classified independently.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32139

{using masks}

Definition statement

This place covers:

Etching involving a mask specifically adapted to the etching operation.

References

Limiting references

This place does not cover:

Classical photoresist masks, except if submitted to a special treatment, for example hardening, fluorination, etc.	G03F 7/00

Special rules of classification

In case the mask would be of general interest, it should also be classified in H01L 21/033.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/3215

Doping the layers

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Doping of these layers is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/322

to modify their internal properties, e.g. to produce internal imperfections

Definition statement

This place covers:

- Treatments aimed at modifying the intrinsic properties of the crystals not otherwise provided for in H01L 21/00, like crystallographic defect rate.
- Formation of defects for intrinsic or extrinsic gettering

References

Limiting references

This place does not cover:

Modification of conductivity type	H01L 21/3242

H01L 21/3221

{of silicon bodies, e.g. for gettering}

Definition statement

This place covers:

Extrinsic gettering

Special rules of classification

Gettering using both extrinsic and intrinsic gettering techniques is classified in both H01L 21/3221 and H01L 21/3225.

H01L 21/3225

{Thermally inducing defects using oxygen present in the silicon body for intrinsic gettering (H01L 21/3226 takes precedence)}

Definition statement

This place covers:

Intrinsic gettering

References

Limiting references

This place does not cover:

Treatment of semiconductor bodies to modify their internal properties of silicon on insulator	H01L 21/3226

Special rules of classification

Gettering using both extrinsic and intrinsic gettering techniques is classified in both H01L 21/3221 and H01L 21/3225.

H01L 21/34

the devices having semiconductor bodies not provided for in groups H01L 21/18, H10D 48/04 and H10D 48/07, with or without impurities, e.g. doping materials

Definition statement

This place covers:

Processes for fabricating devices having semiconductor bodies not belonging to group IV, IV-IV, III-V materials, or to Se, Te, CuO.

Processes for fabricating devices having semiconductor bodies based on II-VI materials.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacturing radiation sensitive devices	H10F 71/00

Group II-IV active materials for radiation sensitive devices	H10F 77/123
Manufacturing light-emitting devices	H10H 20/01
Group II-IV active materials for light-emitting devices	H10H 20/823

H01L 21/38

Diffusion of impurity materials, e.g. doping materials, electrode materials, into or out of a semiconductor body, or between semiconductor regions

Definition statement

This place covers:

Doping of II-VI materials.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Semiconductor bodies composed of II-VI compounds for light sensitive devices	H10F 77/123

H01L 21/42

Bombardment with radiation

Definition statement

This place covers:

Radiation covers corpuscular as well as electromagnetic radiation

References

Limiting references

This place does not cover:

Bombardment with radiation for deposition purposes	H01L 21/02104
Bombardment with radiation for etching purposes	H01L 21/306, H01L 21/311 or H01L 21/3213

H01L 21/425

producing ion implantation

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Ion beam tubes for localized treatment	H01J 37/30

H01L 21/426

using masks

Definition statement

This place covers:

Processes for implantation wherein the invention is focused on the mask aspect, e.g. mask having a specific topography.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Masks in general	H01L 21/027 and H01L 21/033

H01L 21/44

Manufacture of electrodes on semiconductor bodies using processes or apparatus not provided for in groups H01L 21/38 - H01L 21/428

Definition statement

This place covers:

Electrodes on semiconductor materials as defined under H01L 21/34.

Covers the direct deposition of conductive materials on the semiconductor and on an insulating layer overlying the semiconductor (e.g. Tunnel contact).

The group H01L 21/44 includes specific treatments of the semiconductor before formation of the contact (e.g. degenerescence by bombardment etc.).

References

Limiting references

This place does not cover:

semiconductor materials of group IV or III-V	H01L 21/18

H01L 21/441

Deposition of conductive or insulating materials for electrodes

Definition statement

This place covers:

Insulating materials, only if the contact is a tunnelling contact.

H01L 21/445

from a liquid, e.g. electrolytic deposition

Definition statement

This place covers:

- Electrolytic deposition
- Electroless deposition

H01L 21/447

involving the application of pressure, e.g. thermo-compression bonding

Special rules of classification

Classification is made in this group only if specific to the semiconductor material, or adapted to the type of device.

H01L 21/449

involving the application of mechanical vibrations, e.g. ultrasonic vibrations

Special rules of classification

Classification is made in this group only if specific to the semiconductor material, or adapted to the type of device.

H01L 21/46

Treatment of semiconductor bodies using processes or apparatus not provided for in groups H01L 21/428 (manufacture of electrodes thereon H01L 21/44)

Definition statement

This place covers:

The treatment of semiconductor bodies including

- mechanical treatments, like grinding, sand blasting etc.
- chemical treatments, like etching,
- after-treatments of these semiconductors, like formation of insulating layers, planarisation or etching of these insulating layers, formation of conductive layers on these insulating layers and after treatment of these conductive layers and their doping.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture of electrodes thereon	H01L 21/44

H01L 21/465

Chemical or electrical treatment, e.g. electrolytic etching (to form insulating layers H01L 21/469)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Chemical or electrical treatment to form insulating layers thereon	H01L 21/469

H01L 21/467

using masks

References

Limiting references

This place does not cover:

Masks used for patterning group IV and group III-V semiconductors	H01L 21/308

H01L 21/469

to form insulating layers thereon, e.g. for masking or by using photolithographic techniques (encapsulating layers H01L 21/56); After-treatment of these layers

References

Limiting references

This place does not cover:

Encapsulating layers	H01L 21/56

Informative references

Attention is drawn to the following places, which may be of interest for search:

Layers forming electrodes	H01L 21/44

H01L 21/47

Organic layers, e.g. photoresist (H01L 21/475, H01L 21/4757 take precedence)

References

Limiting references

This place does not cover:

Forming insulating layers using masks	H01L 21/475
After-treatment	H01L 21/4757

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of photoresist masks	H01L 21/027, G03F 7/00

H01L 21/4763

Deposition of non-insulating, e.g. conductive -, resistive -, layers on insulating layers; After-treatment of these layers (manufacture of electrodes H01L 21/28, {H01L 21/44})

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture of electrodes	H01L 21/28

H01L 21/48

Manufacture or treatment of parts, e.g. containers, prior to assembly of the devices, using processes not provided for in a single one of the groups H01L 21/18 - H01L 21/326 or H10D 48/04 - H10D 48/07

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Insulating sealing of leads in bases	H01L 21/50
Apparatus therefor	H01L 21/67
Containers, encapsulations, fillings or mountings per se	H01L 23/00
Marking of parts	H01L 23/544
Arrangements for connecting or disconnecting semiconductor or other solid-state bodies, or methods related thereto, other than those	H01L 24/00

Special rules of classification

In this group, the expression "treatment" also covers the removal of leads from parts.

H01L 21/50

Assembly of semiconductor devices using processes or apparatus not provided for in a single one of the groups H01L 21/18 - H01L 21/326 or H10D 48/04 - H10D 48/07 {e.g. sealing of a cap to a base of a container}

References

Limiting references

This place does not cover:

Arrangements for connecting or disconnecting semiconductor or other solid state bodies, or methods related thereto, other than those	H01L 24/00

H01L 21/67

Apparatus specially adapted for handling semiconductor or electric solid state devices during manufacture or treatment thereof; Apparatus specially adapted for handling wafers during manufacture or treatment of semiconductor or electric solid state devices or components {; Apparatus not specifically provided for elsewhere (processes per se H01L 21/30, H01L 21/46, H01L 23/00; simple temporary support means, e.g. using adhesives, electric or magnetic means H01L 21/68, H01L 21/302; apparatus for manufacturing arrangements for connecting or disconnecting semiconductor or solid-state bodies and for methods related thereto H01L 24/74;)}

Definition statement

This place covers:

the apparatus of the title and also the use of those apparatus

References

Limiting references

This place does not cover:

Welding apparatus	B23K 20/00
Polishing apparatus	B24B 1/00
Apparatus for cutting semiconductor ingot	B28D 5/00
Coating apparatus	C23C 14/00, C23C 16/00
Electroplating apparatus	C25D 7/12
Optical measuring apparatus	G01N 21/00
Testing apparatus	G01R 31/00
Lithographic apparatus	G03F 7/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cleaning in general	B08B 1/00, B08B 3/00, B08B 5/00, B08B 6/00, B08B 7/00
Cutting in general	B23K 26/00
Robots in general	B25J 9/00
Conveying in general	B65G 49/00
Electrostatic holders in general	H02N 13/00

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Substrate	a substrate suitable for semiconductor or electric solid state devices or semiconductor or electric solid state components, e.g. a wafer

H01L 21/67017

{Apparatus for fluid treatment (H01L 21/67126, H01L 21/6715 take precedence)}

Definition statement

This place covers:

- Fluid delivery or exhaust systems (like plumbing, heat exchanger, valves systems, flow regulations means, pumping means) in direct connection with semiconductor manufacture or handling systems.
- Atmosphere control systems in relation with semiconductor industry

References

Limiting references

This place does not cover:

Apparatus for sealing, encapsulating, glassing, decapsulating	H01L 21/67126
Apparatus for applying a liquid, a resin, an ink	H01L 21/6715
Details relating to the exhausts (e.g. pumps, filters, scrubber) of coating apparatus	C23C 16/4412

Informative references

Attention is drawn to the following places, which may be of interest for search:

Containers with atmosphere control	H01L 21/67389

H01L 21/67028

{for cleaning followed by drying, rinsing, stripping, blasting or the like}

Definition statement

This place covers:

- Apparatus dealing with at least two processing steps taking place successively (like cleaning, drying, rinsing, stripping or blasting) are classified in this group.
- Systems for only dry cleaning.

H01L 21/67092

{Apparatus for mechanical treatment (or grinding or cutting, see the relevant groups in subclasses B24B or B28D)}

Definition statement

This place covers:

- apparatus for dividing wafers into a plurality of parts (dicing),
- apparatus for exerting a pressure on a substrate (like apparatus for bonding two wafers together),
- apparatus for separating two bonded wafers.

References

Limiting references

This place does not cover:

Cutting apparatus per se	B23K 26/00
Polishing apparatus	B24B 1/00
Apparatus for cutting semiconductor ingot	B28D 5/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Division of the substrate into plural individual devices	H01L 21/78

H01L 21/67103

{mainly by conduction}

Definition statement

This place covers:

- Apparatus where the substrate is in direct contact with the heating element
- Heating elements with specific thermal properties (like thermal conductivity), e.g. materials of the heating element.

H01L 21/67109

{mainly by convection}

Definition statement

This place covers:

- Apparatus where the substrate is not in direct contact with the heating element
- Thermal apparatus with cooling means, e.g. for temperature regulation

H01L 21/67115

{mainly by radiation}

Definition statement

This place covers:

Thermal apparatus comprising lamps, infrared light irradiation means or ultraviolet light irradiation means

H01L 21/67126

{Apparatus for sealing, encapsulating, glassing, decapsulating or the like (processes H01L 23/02, H01L 23/28)}

Definition statement

This place covers:

- Sealing arrangements (like O-ring) for a process chamber, a holding or transporting device
- Slit valves or gates for closing the opening of a chamber

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Containers; Seals for semiconductor devices	H01L 23/02
Encapsulations, e.g. encapsulating layers, coatings for protection	H01L 23/28

H01L 21/67132

{Apparatus for placing on an insulating substrate, e.g. tape}

Definition statement

This place covers:

- All apparatus dealing with tapes (tape removal apparatus, tape placing apparatus)
- Apparatus for removing dies from an adhesive tape (on which a severed wafer is placed).

H01L 21/67144

{Apparatus for mounting on conductive members, e.g. leadframes or conductors on insulating substrates}

Definition statement

This place covers:

Pick and Place apparatus (picking a die from a wafer and placing it on a different location).

H01L 21/6715

{Apparatus for applying a liquid, a resin, an ink or the like (H01L 21/67126 takes precedence)}

References

Limiting references

This place does not cover:

Apparatus for sealing, encapsulating, glassing, decapsulating	H01L 21/67126

H01L 21/67213

{comprising at least one ion or electron beam chamber (coating by ion implantation C23C; ion or electron beam tubes H01J 37/00)}

References

Limiting references

This place does not cover:

Coating by ion implantation	C23C

Informative references

Attention is drawn to the following places, which may be of interest for search:

Ion or electron beam tubes	H01J 37/00

H01L 21/67219

{comprising at least one polishing chamber (polishing apparatuses B24B)}

References

Limiting references

This place does not cover:

Polishing apparatuses per se	B24B

H01L 21/67225

{comprising at least one lithography chamber (lithographic apparatuses G03F 7/00)}

References

Limiting references

This place does not cover:

Lithographic apparatuses per se	G03F 7/00

H01L 21/6723

{comprising at least one plating chamber (electroless plating apparatuses C23C, electroplating apparatuses C25D)}

References

Limiting references

This place does not cover:

Electroless plating apparatuses	C23C
Electroplating apparatuses	C25D

H01L 21/67242

{Apparatus for monitoring, sorting or marking (testing or measuring during manufacture H01L 22/00, marks per se H01L 23/544; testing individual semiconductor devices G01R 31/26)}

References

Limiting references

This place does not cover:

Electrical testing individual semiconductor devices	G01R 31/26

Informative references

Attention is drawn to the following places, which may be of interest for search:

Testing or measuring	H01L 22/00
Marks per se	H01L 23/544

H01L 21/67276

{Production flow monitoring, e.g. for increasing throughput (program-control systems per se G05B 19/00, e.g. total factory control G05B 19/418)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Program-control systems per se	G05B 19/00
Total factory control	G05B 19/418

H01L 21/673

using specially adapted carriers {or holders; Fixing the workpieces on such carriers or holders (holders for supporting a complete device in operation H01L 23/32)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Holders for supporting a complete device in operation	H01L 23/32

H01L 21/67333

{Trays for chips (magazine for components H05K 13/0084)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Magazine for components	H05K 13/0084

H01L 21/6734

{specially adapted for supporting large square shaped substrates (containers and packaging elements for glass sheets B65D 85/48, transporting of glass products during their manufacture C03B 35/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Containers and packaging elements for glass sheets	B65D 85/48
Transporting of glass products during their manufacture	C03B 35/00

H01L 21/67363

{specially adapted for containing substrates other than wafers (H01L 21/67356, H01L 21/67359 take precedence)}

References

Limiting references

This place does not cover:

Closed carriers specially adapted for containing chips, dies or ICs	H01L 21/67356
Closed carriers specially adapted for containing masks, reticles or pellicles	H01L 21/67359

H01L 21/67366

{characterised by materials, roughness, coatings or the like (materials relating to an injection moulding process B29C 45/00; chemical composition of materials C08L 51/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Materials relating to an injection moulding process	B29C 45/00
Chemical composition of macromolecular compounds	C08L 51/00

H01L 21/67706

{Mechanical details, e.g. roller, belt (H01L 21/67709 takes precedence)}

References

Limiting references

This place does not cover:

Conveying using magnetic elements	H01L 21/67709

H01L 21/67721

{the substrates to be conveyed not being semiconductor wafers or large planar substrates, e.g. chips, lead frames (H01L 21/6773 takes precedence)}

References

Limiting references

This place does not cover:

Conveying cassettes, containers or carriers	H01L 21/6773

H01L 21/67742

{Mechanical parts of transfer devices (robots in general in B25J)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Robots in general	B25J

H01L 21/67763

{the wafers being stored in a carrier, involving loading and unloading (H01L 21/6779 takes precedence)}

References

Limiting references

This place does not cover:

The workpieces being stored in a carrier, involving loading and unloading	H01L 21/6779

H01L 21/67766

{Mechanical parts of transfer devices (robots in general in B25J)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Robots in general	B25J

H01L 21/67784

{using air tracks}

Definition statement

This place covers:

Apparatus for moving substrates on a liquid track

H01L 21/67796

{with angular orientation of workpieces (H01L 21/67787 and H01L 21/67793 take precedence)}

References

Limiting references

This place does not cover:

Conveying with angular orientation of the workpieces	H01L 21/67787

Conveying with orientating and positioning by means of a vibratory bowl or track	H01L 21/67793

H01L 21/68

for positioning, orientation or alignment

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Conveying	H01L 21/677

H01L 21/682

{Mask-wafer alignment (in general G03F 7/70, G03F 9/70)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Alignment in general	G03F 7/70, G03F 9/70

H01L 21/683

for supporting or gripping (for conveying H01L 21/677, for positioning, orientation or alignment H01L 21/68)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Conveying	H01L 21/677
Positioning, orientation or alignment	H01L 21/68

H01L 21/6835

{using temporarily an auxiliary support}

References

Limiting references

This place does not cover:

Temporary protection of the devices or parts of the devices during manufacture	B81C 2201/05

H01L 21/6836

{Wafer tapes, e.g. grinding or dicing support tapes (adhesive tapes in general C09J 7/20)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Adhesive tapes in general	C09J 7/20

H01L 21/687

using mechanical means, e.g. chucks, clamps or pinches {(using elecrostatic chucks H01L 21/6831)}

References

Limiting references

This place does not cover:

Using electrostatic chucks	H01L 21/6831

H01L 21/70

Manufacture or treatment of devices consisting of a plurality of solid state components formed in or on a common substrate or of parts thereof; Manufacture of integrated circuit devices or of parts thereof ({multistep manufacturing processes of assemblies consisting of a plurality of individual semiconductor or other solid state devices H01L 25/00; } manufacture of assemblies consisting of preformed electrical components H05K 3/00, H05K 13/00)

Definition statement

This place covers:

- Process for the integration of a plurality of solid state devices in or on a common substrate.
- Processes for making isolation regions between components (e.g. LOCOS, STI etc.)
- Processes for fabricating SOI substrates.
- Processes for making interconnections between the solid state devices, on the surface of the substrate, or buried in the substrate, including specific treatments of these interconnections.
- Processes for cutting wafers to singulate the devices, dicing.
- Processes to fabricate devices consisting of a plurality of solid state components or integrated circuits of the bipolar, Field-Effect type and memories.
- Process for the assembly on a common substrate of two or more components.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture of assemblies consisting of preformed electrical components	H05K 3/00, H05K 13/00

H01L 21/71

Manufacture of specific parts of devices defined in group H01L 21/70 ({H01L 21/0405, H01L 21/0445} , H01L 21/28, H01L 21/44, H01L 21/48 take precedence)

Definition statement

This place covers:

- Multistep processes for the fabrication of buried regions, also used as buried connections between zones,
- Multistep processes for the fabrication of zones providing electrical isolation between adjacent components,
- Multistep processes for the fabrication of SOI wafers, for which the fabrication of devices has not started yet,
- Multistep processes for the fabrication of interconnections between devices,
- Multistep, processes for the fabrication of integrated circuits, bipolar technology, field-effect technology, CMOS, memories, IC based on combinations of these technologies,
- Multistep processes for dicing wafers into individual devices.

References

Limiting references

This place does not cover:

Processing of parts of devices based on carbon or diamond	H01L 21/0405
Processing of parts of devices based on crystalline Silicon Carbide	H01L 21/0445
Multistep processes for the manufacture of electrodes	H01L 21/28 or H01L 21/44
Manufacture or treatment of parts prior to assembly of the devices, like leads, heat-sinks, etc.	H01L 21/48

Informative references

Attention is drawn to the following places, which may be of interest for search:

Wire-like connections	H01L 24/00

H01L 21/74

Making of {localized} buried regions, e.g. buried collector layers, internal connections {substrate contacts}

Definition statement

This place covers:

Multistep processes for the fabrication of buried regions, like buried collector layers, buried connections between zones, substrate contacts, as part of a component, e.g. formation of buried silicides.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Diffusing impurities	H01L 21/22
Implanting impurities	H01L 21/265

H01L 21/743

{Making of internal connections, substrate contacts}

Definition statement

This place covers:

Fabrication of buried metallic or near metallic regions, like buried silicides, buried eutectic conductors.

H01L 21/76

Making of isolation regions between components

Definition statement

This place covers:

- Fabrication of zones aimed at providing electrical isolation between adjacent components, i.e. dielectric regions (LOCOS, trench, shallow trench), air gaps, p-n junction or field effect.
- Fabrication of SOI wafers, for which the fabrication of devices has not started yet.

Special rules of classification

For subject matter classified in the range H01L 21/76 - H01L 21/765, when the isolation combines several techniques, both techniques are given a group symbol.

When the combination of several techniques involves the fabrication of SOI, a group symbol within the range H01L 21/76264 - H01L 21/76291 is given.

Single steps, like etching a trench, when they present a general interest or are specifically disclosed, should be given a group symbol in the corresponding single step covered by H01L 21/02 and sub groups.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

horizontal	in the plane of the wafer
vertical	in a direction perpendicular to the plane of the wafer

H01L 21/762

Dielectric regions {, e.g. EPIC dielectric isolation, LOCOS; Trench refilling techniques, SOI technology, use of channel stoppers}

Definition statement

This place covers:

Covers the formation of dielectric regions by

- Oxidation of the substrate, or
- Deposition of a dielectric, for example in a trench.
- Formation of dielectric regions buried in the substrate, SOI

H01L 21/76224

{using trench refilling with dielectric materials (trench filling with polycristalline silicon H01L 21/763; together with vertical isolation, e.g. trench refilling in a SOI substrate H01L 21/76264)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Trench filling with vertical isolation, e.g. trench refilling in a SOI substrate	H01L 21/76264
Trench filling with polycrystalline silicon	H01L 21/763

H01L 21/7624

{using semiconductor on insulator [SOI] technology}

Definition statement

This place covers:

The groups H01L 21/7624 - H01L 21/76291 cover the fabrication of a buried isolation region

References

Limiting references

This place does not cover:

Dielectric isolation using EPIC techniques, i.e. epitaxial passivated integrated circuit	H01L 21/76297

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture of integrated circuits on insulating substrates	H10D 86/01
Silicon on sapphire (SOS) technology	H10D 86/03

H01L 21/768

Applying interconnections to be used for carrying current between separate components within a device {comprising conductors and dielectrics}

Definition statement

This place covers:

Multi-steps processes for manufacturing interconnections on the surface of a device or through the wafer.

References

Limiting references

This place does not cover:

Fabrication of contacts	H01L 21/28
Internal interconnections	H01L 21/743
Fabrication of fuses and anti-fuses	H01L 23/525

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cleaning	H01L 21/02041
Formation of insulating layers	H01L 21/02107
Formation or use of masks	H01L 21/027, H01L 21/033, H01L 21/31144, H01L 21/32139
Planarising insulating or conductive layers	H01L 21/3105, H01L 21/321
Etching of insulating or conductive layers	H01L 21/311, H01L 21/3213

Special rules of classification

Information peculiar to single-step processes should also be classified in the corresponding sub group of H01L 21/02 (see informative references below).

Processes for fabricating fuses and anti-fuses are classified with the fuses and anti-fuses in H01L 23/525.

H01L 21/76804

{by forming tapered via holes}

Definition statement

This place covers:

Methods specially adapted for forming via or contact holes having a wider top or bottom region, e.g. "cup-shaped" vias

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Etching insulating layers per se	H01L 21/311

H01L 21/76805

{the opening being a via or contact hole penetrating the underlying conductor}

Definition statement

This place covers:

Methods of forming via or contact holes including a step of etching the conductor at the bottom of the hole so as to form e.g. a gouging feature;

methods of forming contact holes having a portion reaching into conductive regions (e.g. source and drain) of the semiconductor substrate

H01L 21/76808

{involving intermediate temporary filling with material}

Definition statement

This place covers:

Methods of dual damascene processing involving intermediate temporary filling of the opening first formed in the process with material, e.g. planarisation to facilitate lithography of the second opening

Examples:

- After formation of the via, the via is filled with a resin film 12 to provide for planarisation:::

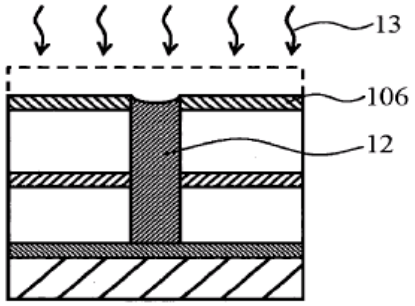


FIG. 2B

US2006094221.

- The dual damascene structure of a lower metal level 200 is filled with a sacrificial material 140 (see the figure below), then another metal level 202 having dual damascene structures 232 is fabricated. Finally, the sacrificial layer 140 is removed and all metal levels are metalized simultaneously:

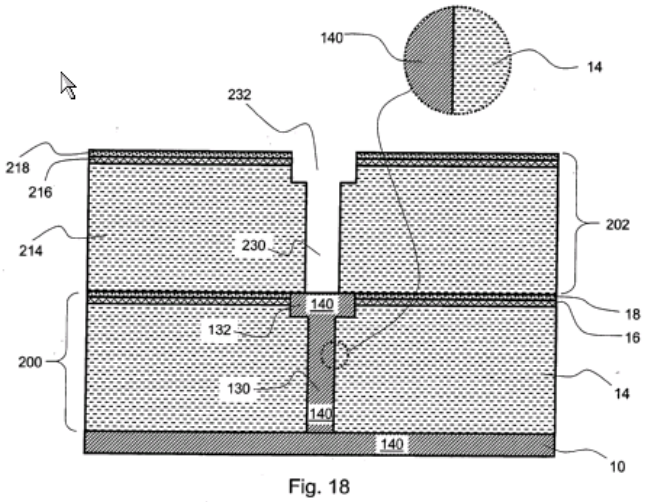


Fig. 18

US2005110145

References

Limiting references

This place does not cover:

Conventional trench-first dual damascene methods in which the photoresist for forming the via hole fills the trench	H01L 21/76807

H01L 21/7681

{involving one or more buried masks}

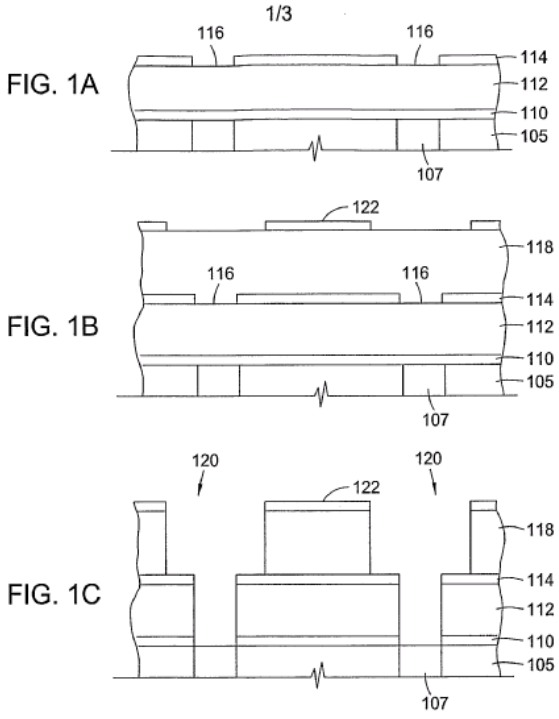
Definition statement

This place covers:

Methods of dual damascene processing involving one or more buried masks, i.e. one or more pre-patterned mask or etch stop layers are fabricated prior to deposition of the trench-level dielectric.

Examples:

- The etch stop 114 is pre-patterned and buried under ILD 118 (see the figure below):



WO2005109473

H01L 21/76811

{involving multiple stacked pre-patterned masks}

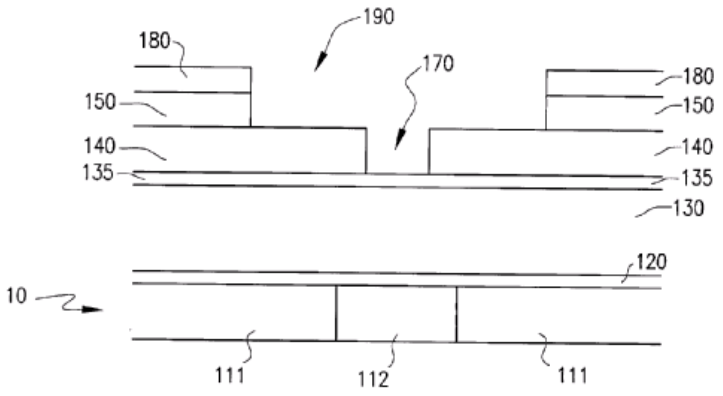
Definition statement

This place covers:

Methods of dual damascene processing involving multiple stacked pre-patterned masks on the trench-level dielectric, i.e. mask stacks pre-defining the trench and via patterns before the actual etching process

Examples:

Layers 135, 140, 150 are hardmask layers, layer 180 is a photoresist for patterning layer 150. The dual damascene structure is transferred into the ILD 130 with the help of the stack of pre-patterned hardmasks 135, 140, 150:



US2003207207

H01L 21/76813

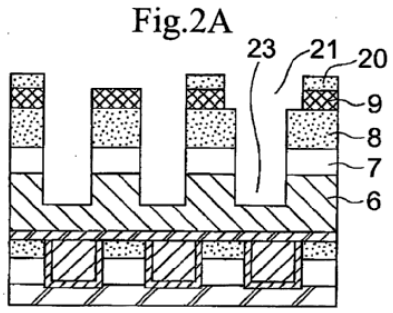
{involving a partial via etch}

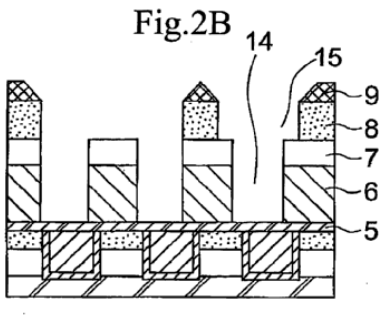
Definition statement

This place covers:

All dual damascene processes in which in an early stage a via is formed partially through the dielectric stack. The via etch is completed later in the process, e.g. during the etching step for forming the trench.

Examples:





US2006166482

First, the via is partially etched into the dielectric stack. In a later step, the via etch is completed together with the trench etch.

Special rules of classification

Dual damascene processing also involving a stack of pre-patterned hard mask layers, the group symbol H01L 21/76811 is also assigned.

If the partial via process also includes a step of intermediate filling the partial via with a planarising material, the document needs to be classified in H01L 21/76808, too.

H01L 21/76814

{post-treatment or after-treatment, e.g. cleaning or removal of oxides on underlying conductors}

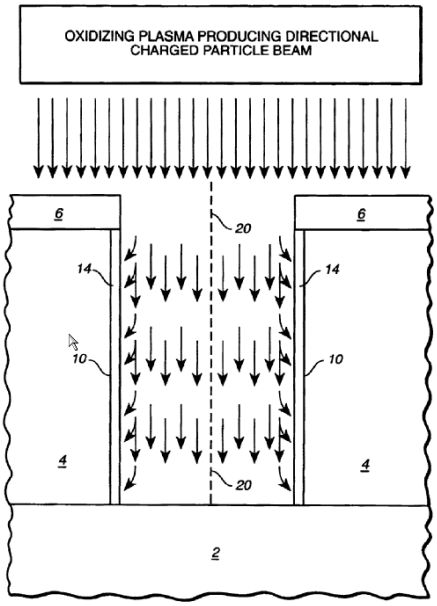
Definition statement

This place covers:

Particular method steps designed for improving the result of a process of forming an interconnect opening in a dielectric, e.g. removal of oxides from the surface of a conductor at the bottom of a via hole, removal of etching residues, or treatments restoring the dielectric at the sidewalls.

Examples:

After formation of the opening 10, the photoresist mask and etch residues are removed using a reducing plasma. During this treatment an undesired coating layer 14 forms on the sidewalls of opening 10. Layer 14 is eventually removed by the directional beam of charged oxidizing particles having its main axis 20 parallel to the sidewalls of opening 10:



US6673721

Note that in this case the sidewall layer 14 is an undesired by-product of a plasma treatment process. The document should therefore not be classified in H01L 21/76831.

After forming an opening in a low-k dielectric, a degassing treatment and a plasma treatment are carried out in order to remove methyl groups from the dielectric and an oxide from the underlying conductor 22A:

FIG.6D

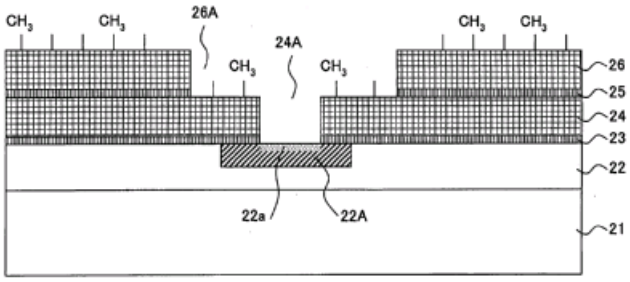
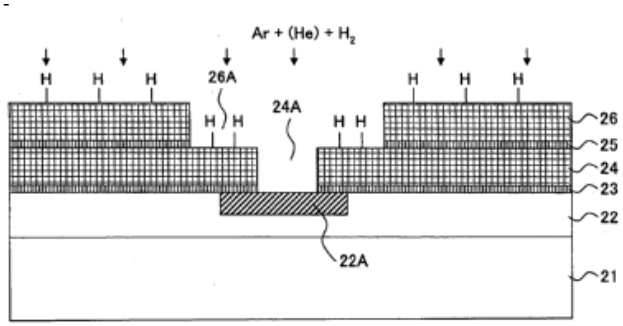


FIG.6E



US2005272247

References

Limiting references

This place does not cover:

After-treatment steps leading to the formation of modified sidewall layers	H01L 21/76831

Special rules of classification

If the method of after-treatment comprises aspects which are classified in any one of the subgroups H01L 21/76822+ (see below), the corresponding group should also be given. If the after-treatment leads to the formation of a sidewall layer in the opening comprising modified dielectric material, the group H01L 21/76831 should also be assigned (note, however, that if the sidewall insulation is formed by a conventional deposition step, H01L 21/76831 is the only relevant group).

H01L 21/76814 is essentially a multistep group, i.e. the after treatment step is only one of several steps to be carried out in order to form an interconnection. If a document exclusively relates to cleaning of openings in dielectrics (in a single-step fashion), the main group symbol is H01L 21/02063.

H01L 21/76816

{Aspects relating to the layout of the pattern or to the size of vias or trenches (layout of the interconnections per se H01L 23/528; CAD of ICs G06F 30/00)}

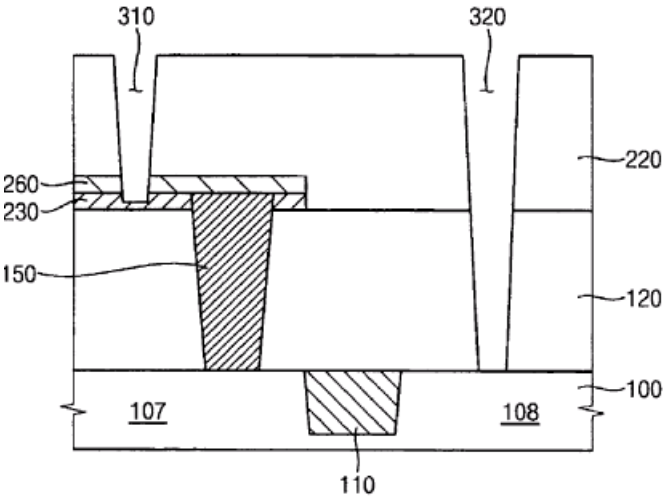
Definition statement

This place covers:

The geometrical "aspects" to be classified in this group are mainly methodological aspects, e.g. step sequences leading to a reduction of the pitch between via holes, step sequences for incorporating a plurality of vias of different depth, methods of forming vias having a particular cross-sectional shape.

Examples:

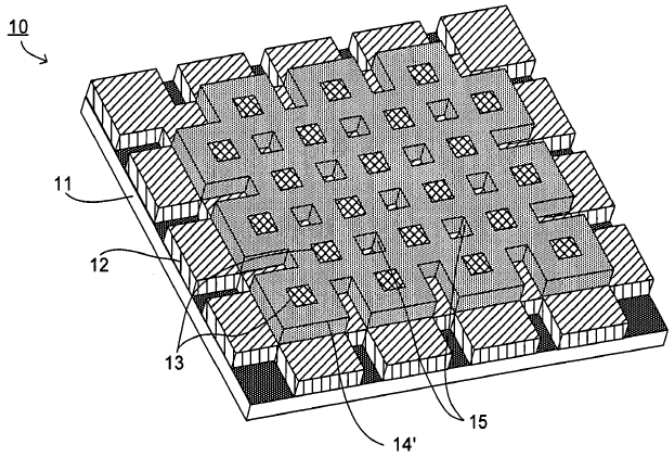
Layer 230 is introduced into the structure to enable the simultaneous formation of a deep and a not-so-deep via. Although the formation of the vias themselves contains no special features at all, there is an aspect related "to the size of the vias":



US2006281290

Method for decreasing the pitch between adjacent contact holes by using a sequence of steps involving among other things a sacrificial pattern (13 in the figure below) and a conformal hardmask layer (14') to create an array of vias having a pitch below what is possible by standard lithography:

Fig. 4



EP1818977

References

Limiting references

This place does not cover:

Geometrical aspects relating to "tapered" vias, i.e. vias having a wider part somewhere	H01L 21/76804

H01L 21/76817

{using printing or stamping techniques}

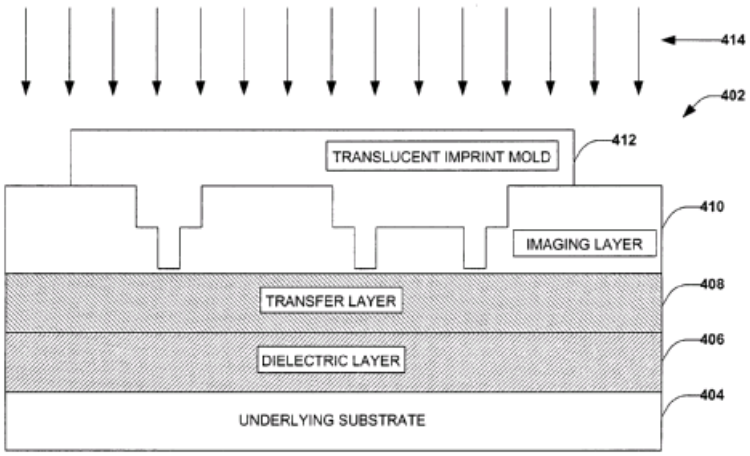
Definition statement

This place covers:

Imprinting or stamping techniques for forming openings in dielectrics.

Methods using a stamp either to pattern a mask, e.g. a resist mask, for forming the opening or to imprint the opening directly into a dielectric

Example:



US7148142

H01L 21/76819

{Smoothing of the dielectric (planarisation of insulating materials per se H01L 21/31051)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Planarisation of insulating materials per se	H01L 21/31051

H01L 21/76822

{Modification of the material of dielectric layers, e.g. grading, after-treatment to improve the stability of the layers, to increase their density etc.}

Definition statement

This place covers:

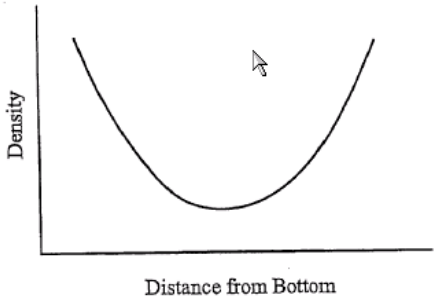
All aspects related to forming or after-treatment steps which lead to a modification of the material of a dielectric layer within an interconnection structure.

Manufacture of "graded" dielectric layers having a varying composition throughout its thickness, no matter if said grading is achieved by a modified deposition process or an after-treatment.

Examples:

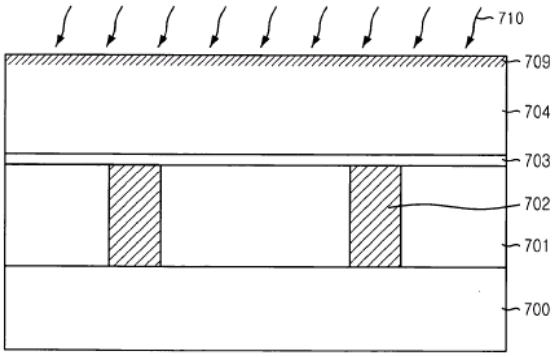
Graded dielectric layer: density and permittivity characteristics vary uniformly from a top portion to a bottom portion of the layer. The variation is achieved through varying deposition parameters such as

flow rate of constituent process gases or deposition chamber pressure, or through a post deposition treatment, such as plasma treatment or curing:



US2006003598

The surface of the PSG layer 704 is made hydrophilic by a "scrubbing treatment" 710:



US2006003582

Special rules of classification

It is not important whether the various treatment steps are conducted on a "main" interlevel or intralevel dielectric or on a "thin functional dielectric layer" as defined in H01L 21/76829 and subgroups.

If the treatment involves a patterned layer including an opening, the group H01L 21/76814 should also be given.

H01L 21/76823

{transforming an insulating layer into a conductive layer}

Definition statement

This place covers:

Processes designed for rendering a dielectric layer of an interconnect stack conductive

Examples:

A diamond etch-stop layer (66 in the figure below) is rendered conductive by implanting Ti followed by thermal treatment.

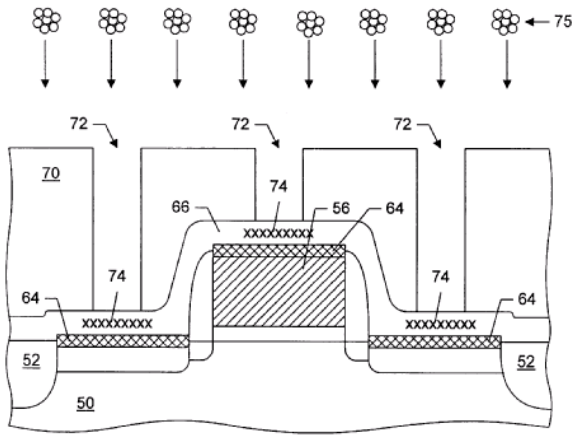


FIG. 6a

US5990493

Special rules of classification

A document classified in this group is additionally classified in H01L 21/76822 and subgroups thereof, whenever appropriate, the method of conversion involves a plasma treatment, or an ion implantation.

H01L 21/76825

{by exposing the layer to particle radiation, e.g. ion implantation, irradiation with UV light or electrons etc. (plasma treatment H01L 21/76826)}

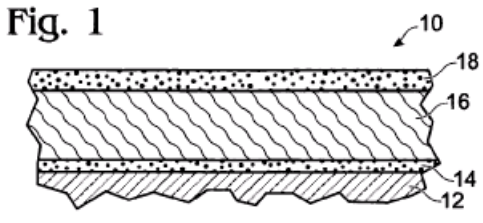
Definition statement

This place covers:

After-treatment or post-treatment process of dielectric layers of the interconnect stack involving particle radiation, e.g. removal of moisture etc. by UV or e-beam radiation, processes for modifying the dielectric constant of the layer, introduction of dopants into the dielectric by particle irradiation.

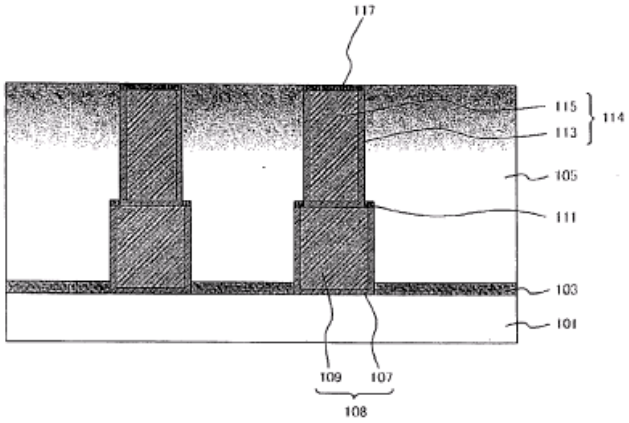
Examples:

A layer of silane is deposited onto a polymer dielectric layer 16. This layer is then exposed to UV light to initiate polymerization of the silane molecules to form an adhesion promoter layer 18 (or an etch stop or hard mask layer), and to react the adhesion promoter layer with low dielectric constant polymer layer 16:



US2005221606

The upper surface of the porous MSQ film 105 is treated by electron beam irradiation or by UV irradiation to reinforce the upper portion in the film 105:



US2006211235

References

Limiting references

This place does not cover:

Removal of porogens for manufacturing porous dielectrics	H01L 21/7682
Plasma treatment	H01L 21/76826

Special rules of classification

If the treatment is performed to form or modify a "thin functional" dielectric layer, e.g. an etch stop, one of the groups H01L 21/76829 is additionally assigned.

Curing of a dielectric precursor material is generally not considered an "after-treatment" but characterizes the formation of the dielectric layer per se, covered by H01L 21/02348.

H01L 21/76826

{by contacting the layer with gases, liquids or plasmas}

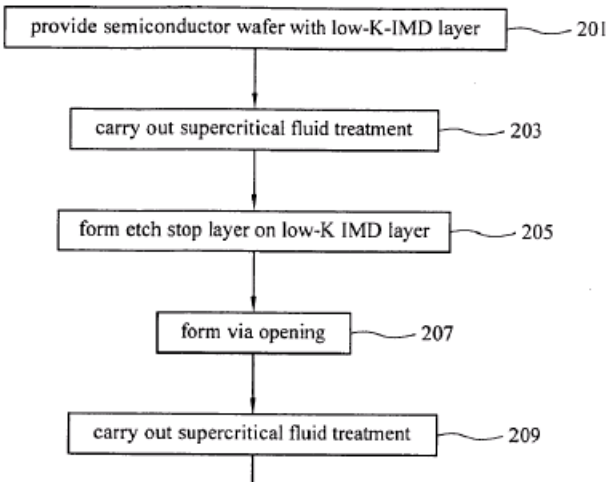
Definition statement

This place covers:

Processes involving contacting a dielectric of an interconnect stack with gases, liquids or plasmas in order to modify the internal structure and/or properties of the dielectric, e.g. nitridation, removal of organic groups from the layer, introduction of dopants into the dielectric using gases, liquids or plasmas.

Examples:

a low-k dielectric is treated in a supercritical fluid after deposition, after via etching, to improve mechanical strength or repair plasma damage:



US2006073697

Plasma treatment 130 is carried out in order to decrease the C- or F- concentration in an upper layer 120a of the ILD 120:

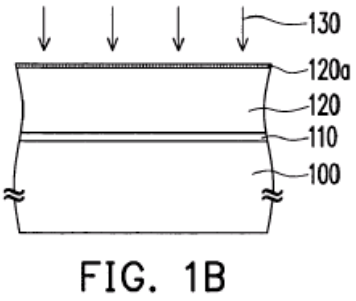


FIG. 1B

US2006286793

Plasma treatment is carried out in order to modify the sidewalls of a damascene opening 218:

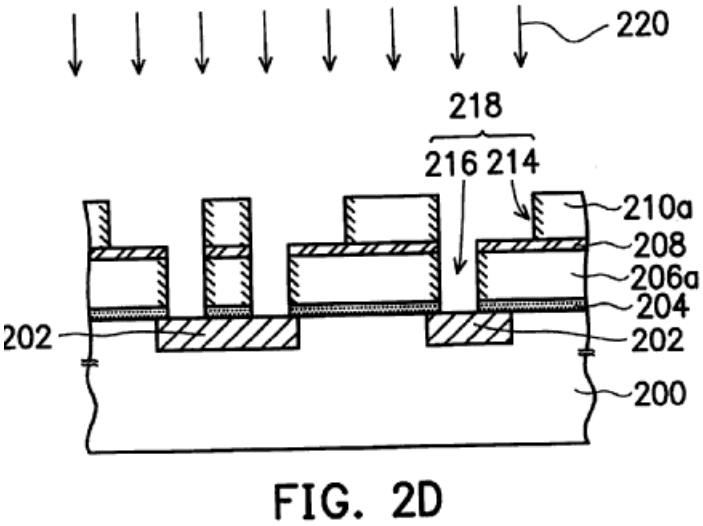


FIG. 2D

US6013581

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Supercritical fluid treatment after a via hole formation	H01L 21/76814
Plasma treatment is carried out to form a modified sidewall layer in an opening	H01L 21/76831

Special rules of classification

If the plasma treatment is carried out to form a modified sidewall layer in an opening, the group symbol H01L 21/76831 must also be assigned.

H01L 21/76828

{thermal treatment}

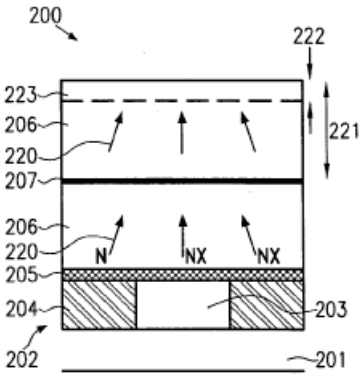
Definition statement

This place covers:

Thermal treatment for modifying the internal structure and/or properties of the dielectric of an interconnect stack, e.g. removal of moisture.

Example:

After completion of the deposition, the low-k dielectric layer 206 is subjected to a heat treatment in a nitrogen-free atmosphere to promote the out-gassing of the volatile materials 220 and especially of nitrogen and nitrogen compounds:



US2004121265

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Plasma annealing	H01L 21/76826

Special rules of classification

If the heat treatment is carried out in reactive atmospheres, i.e. inevitably involves modification of the dielectric material by e.g. introducing a further chemical element into the layer, e.g. plasma annealing, the group symbol H01L 21/76826 is additionally assigned.

H01L 21/76829

{characterised by the formation of thin functional dielectric layers, e.g. dielectric etch-stop, barrier, capping or liner layers}

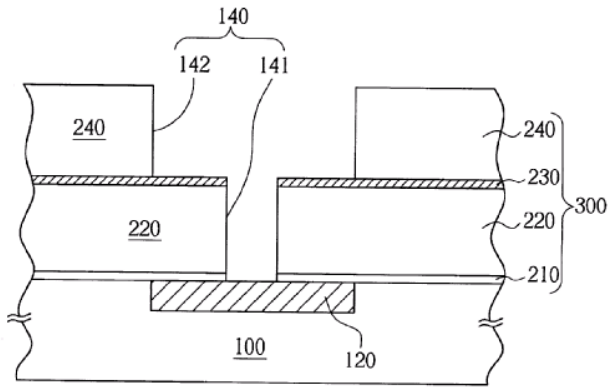
Definition statement

This place covers:

All aspects related to the formation and the geometry of so-called "thin functional dielectric layers", e.g. etch-stop films or dielectric barrier or liner layers.

Examples:

Fabrication of an oxygen-doped low-k SiC etch-stop layer 230:



US2003085408

Nitride liner 130 imparts tensile stress in the underlying semiconductor to improve carrier mobility:

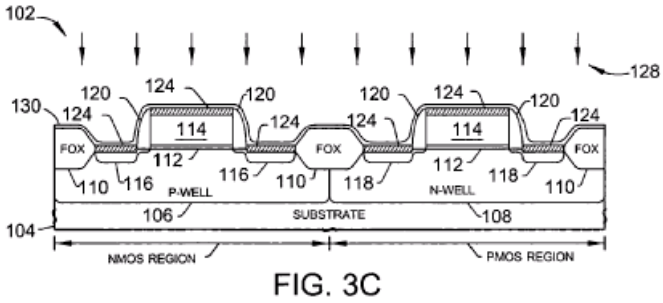
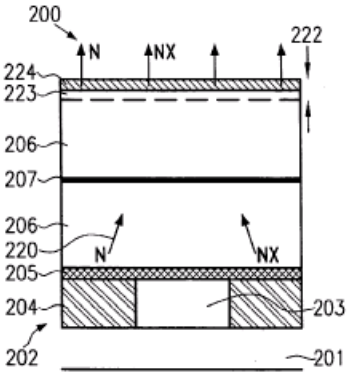


FIG. 3C

US2005233514

Silicon oxide layer 224 is formed on top of a low-k dielectric. Layer 224 serves as a sacrificial cap layer:



US2004121265

Special rules of classification

If a document dealing with a thin functional dielectric layer also contains after-treatment aspects as defined in H01L 21/76822+, one (or more) of the latter groups should also be assigned to this document.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

"Thin" layer as used herein means thin compared with the "main" interlevel or intralevel dielectric. In cases of doubt as to whether the layer is "thin" in the above sense, the criterion "functional layer" takes precedence, i.e. documents relating to layers, which may not exactly be "thin" in the above sense but serve some particular purpose except from merely isolating conductors, should also be classified here.

H01L 21/76831

{in via holes or trenches, e.g. non-conductive sidewall liners}

Definition statement

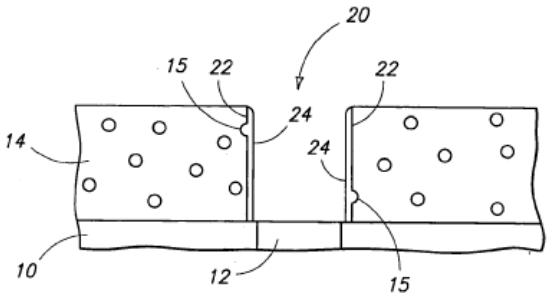
This place covers:

Sidewall layers that are formed by direct deposition

Sidewall liners obtained by treatment of the sidewalls of the opening.

Examples:

Sidewalls of a porous dielectric are plasma-treated in order to form a carbon sealing layer 24 on via sidewalls 22:



US2006046472

Non-metallic layer 15, e.g. silicon carbide or boron carbide is deposited in a dual damascene opening and etched back to form sidewall spacers 19:

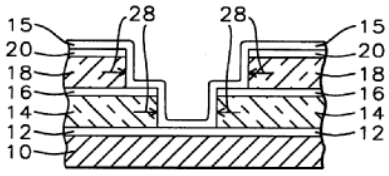


FIG. 5

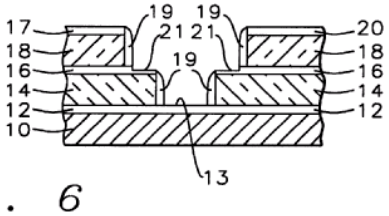


FIG. 6

US6284657

Special rules of classification

If the treatment has characteristics relating to any of the groups H01L 21/76822+, one (or more) of the latter groups should also be assigned.

H01L 21/76832

{Multiple layers}

Definition statement

This place covers:

Stacks of two or more thin "functional" dielectric layers, e.g. multiple etch stop layers, multiple trench liners.

Examples:

Composite adhesion/etch-stop multilayer (SiC layer 104 and SiOC layer 106) is formed; layer 104 is for improving adhesion between layers 100 and 106:

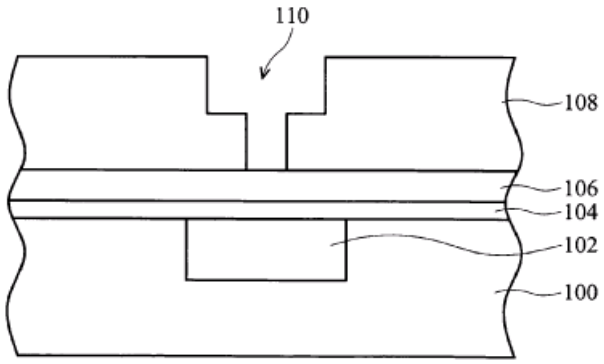
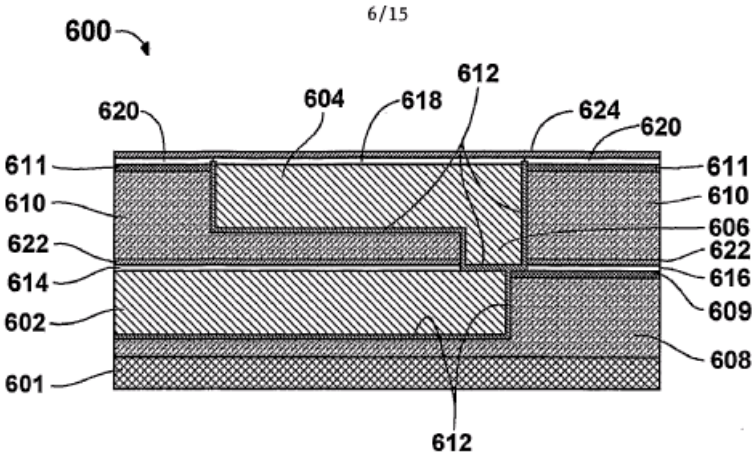


FIG. 2

US2006110912

Multiple dielectric capping layers 616/622 and 620/624 are formed by gas cluster ion beam "infusion":



WO2006052958

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

"multiple"	two or more layers in direct contact with each other.

H01L 21/76834

{formation of thin insulating films on the sidewalls or on top of conductors (H01L 21/76831 takes precedence)}

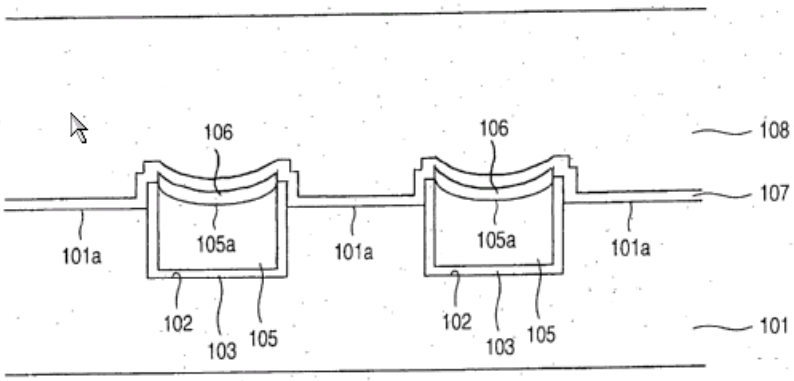
Definition statement

This place covers:

Insulating film covering some part of the conductor regardless of whether the conductor is "free-standing" or an inlaid conductor.

Example:

Dielectric film 107 covers the top and part of the sidewalls of inlaid conductors 105:



US2005087871

Temporary sacrificial encapsulation layer (206 in fig. 5, 306 in fig. 6) is formed in a dual damascene opening and covering an exposed underlying conductor in order to form a protective layer for subsequent cleaning steps:

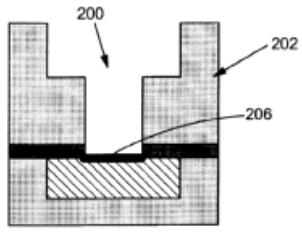


FIG. 5

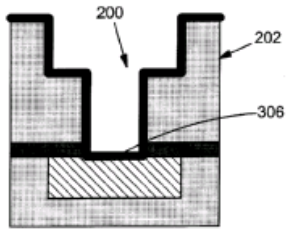


FIG. 6

US2006292863

References

Limiting references

This place does not cover:

Dielectric sidewall liners in openings	H01L 21/76831

H01L 21/76835

{Combinations of two or more different dielectric layers having a low dielectric constant (H01L 21/76832 takes precedence)}

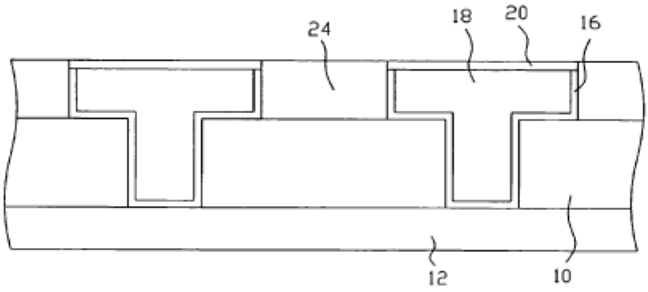
Definition statement

This place covers:

Dielectric layer stacks in which e.g. the via-level dielectric and the trench-level dielectric comprise different low-k materials or in which e.g. the structure contains a low-k etch-stop or adhesion layer separating two dielectrics of which at least one must be a low-k dielectric.

Examples:

Trench-level dielectric (spin-on low-k dielectric 24) and via-level dielectric (CVD SiOC layer 10) are different low-k materials:



US2005130407

Via-level and trench-level dielectrics (204 and 212) are made of the same low-k material, but the etch-stop layer 206 is made of a different low-k material:

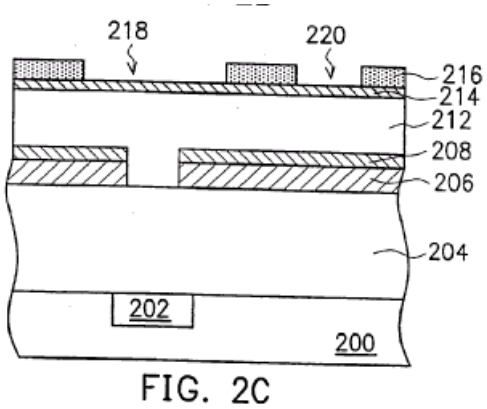


FIG. 2C

US2005263876

Posts (40) are made of a non-porous low-k dielectric whereas the material filling the spaces between the posts is a porous low-k dielectric:

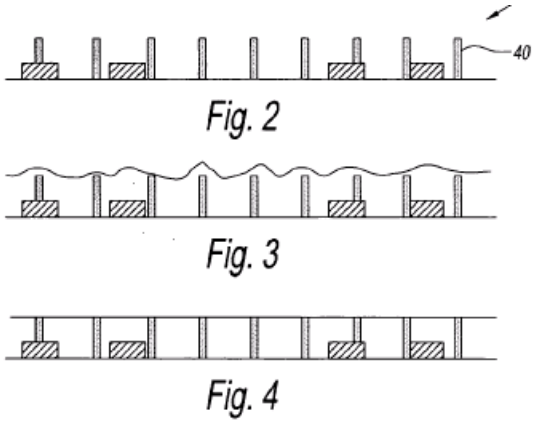


Fig. 2

Fig. 3

Fig. 4

US2005227480

References

Limiting references

This place does not cover:

Middle etch-stop layer being a multilayer system	H01L 21/76832

H01L 21/76837

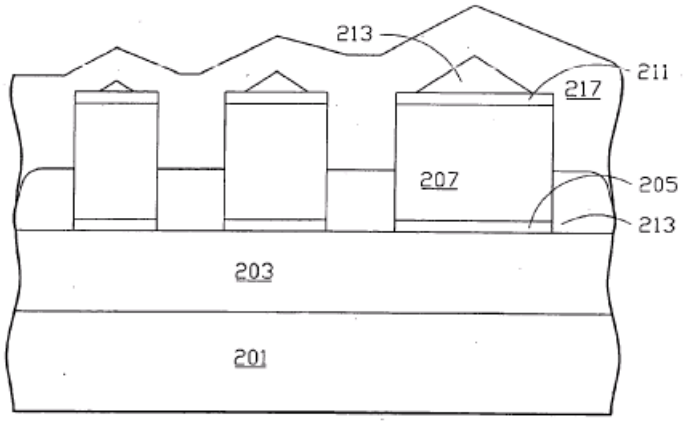
{Filling up the space between adjacent conductive structures; Gap-filling properties of dielectrics}

Definition statement

This place covers:

Special measures for improving the gap-filling properties of a dielectric, wherein said "gap" is formed between conductive structures. The term "gap" is also intended to include vertical gaps.

Example:



US2005186796:

a first dielectric (213) is deposited over conductive structures 207 and etched back (the figure above shows the layer 213 after etch-back) so as to partially fill the gap and reduce its aspect ratio, a second dielectric (217) fills the remaining gap.

H01L 21/76838

{characterised by the formation and the after-treatment of the conductors (etching for patterning the conductors H01L 21/3213)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

When the interconnect is also used as the conductor part of a conductor-insulator-semiconductor electrode (gate level interconnections)	H01L 21/28026
Etching for patterning conductors	H01L 21/3213

Special rules of classification

Information peculiar to single-step processes should also be classified in the corresponding group(s), e.g.

- H01L 21/02041 for cleaning;
- H01L 21/02697, H01L 21/283 - H01L 21/288 and H01L 21/3105 for the formation of conductive layers;
- H01L 21/3213 for etching;
- H01L 21/027, H01L 21/033 and H01L 21/32139 for masking;
- H01L 21/321 for planarising, etc.

H01L 21/76843

{formed in openings in a dielectric}

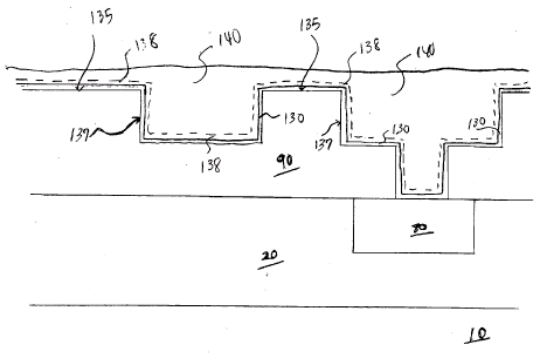
Definition statement

This place covers:

Thin conductive film being formed in an opening in a dielectric, e.g. barrier, adhesion, nucleation, seed or liner layers.

Example:

a barrier layer comprising e.g. Ru, Ir etc. or one of their (conducting) oxides is deposited in a trench or a dual damascene opening:



US2005206000

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thin films serving as seed layer for electroplating	H01L 21/76873

Special rules of classification

All documents dealing with the formation of thin conductive films in openings should be classified in this group or one of its subgroups even if the fact that the thin film is formed in an opening is not an important aspect of the disclosure under consideration.

If the deposition method of the thin functional layer is disclosed in some detail (PVD, CVD, ALD, plating etc.), the corresponding groups H01L 21/28512 - H01L 21/2885 should also be assigned.

H01L 21/76844

{Bottomless liners}

Definition statement

This place covers:

At least one of the conductive thin films in the opening does not cover the bottom of the opening in its entirety, i.e. even when the thin film is removed from only a part of the bottom of the openings.

Examples:

a set of conductive barrier layers is deposited over the sidewalls of a porous dielectric and subsequently removed from the via floor by sputtering:

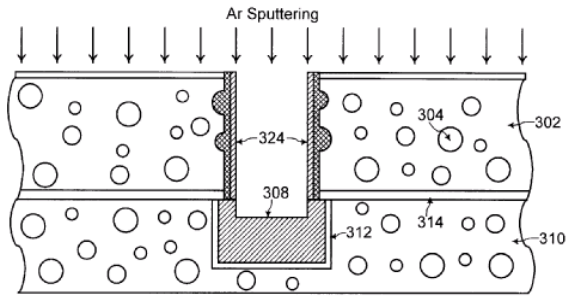


FIG. 27

US6528409

Barrier layers covering only part of the sidewalls:

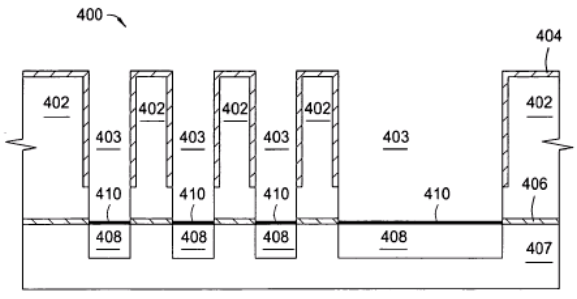
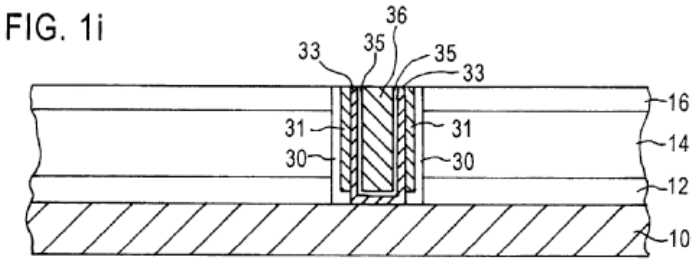


FIG. 4C

US2006246699

Multiple liner layers (30, 31, 33, 35) are deposited in a via of which only the outermost layers (30, 31) are removed from the via bottom:



US6555461

H01L 21/76846

{Layer combinations}

Definition statement

This place covers:

Layer combinations, i.e. arrangements of more than one layer, in the openings, e.g. combinations of particular materials other than the "standard" barrier combinations Ti/TiN, TaN/Ta or W/WN.

Superlattices comprising a multitude of layers comprising "standard" materials (Ti/TiN, TaN/Ta or W/WN), e.g. a TaN/Ta/TaN/Ta... superlattice.

Graded layers, e.g. a stack of infinitely thin multiple layers with varying composition.

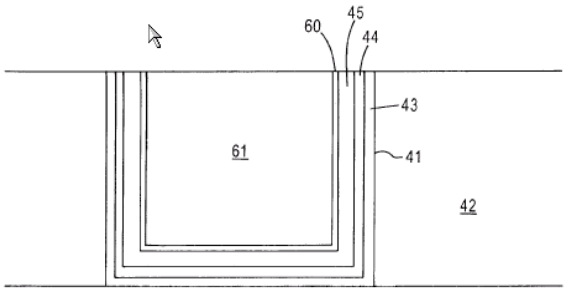
Conductive thin film having a graded composition

Layer combinations formed on top of an inlaid conductor

In these cases the thin film is still considered as being formed "in an opening of a dielectric", see the further explanation and example (i) under point 1.4 below).

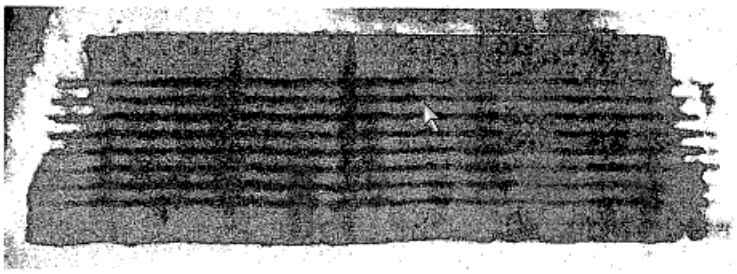
Examples:

43 is a TaN layer, 44 is a TaN layer having a graded content of N, 45 is an alpha-Ta layer:



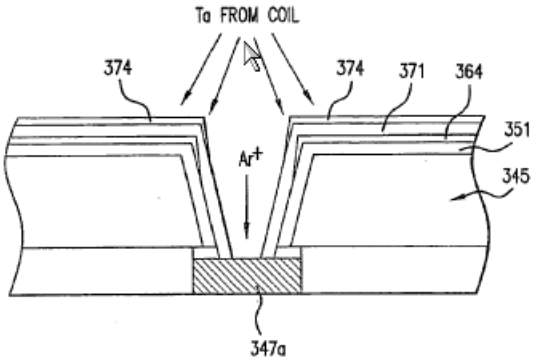
US7033940

TaN/W/TaN/W/... nanolaminates, fabricated by ALD:



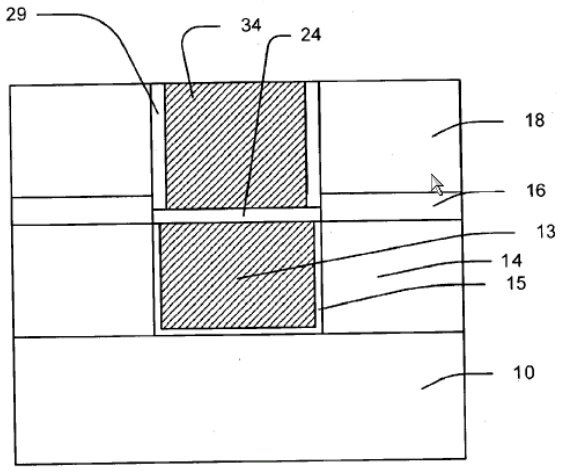
US2006079090

TaN/Ta/TaN/Ta stack:



US2005255691

Different barrier materials on the sidewalls and on the bottom of the via hole (α-phase Ta layer 24 is provided on the via bottom, while the sidewalls are covered with a β-phase Ta layer 29):



US 2004131878

H01L 21/76847

{the layer being positioned within the main fill metal}

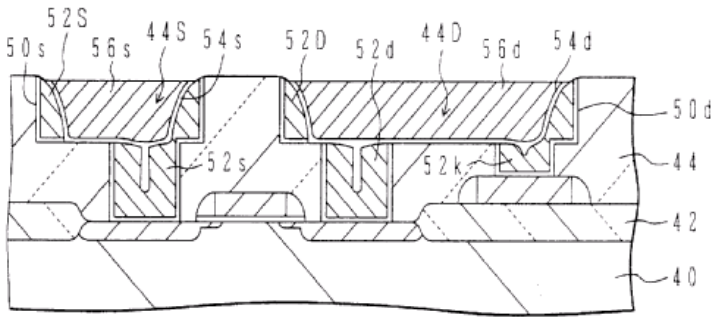
Definition statement

This place covers:

Conductive thin film formed within the "main" conductor filling the opening or where the opening is filled by a sequence of thin films. It is important, however, that said thin film does not comprise the same material as the main fill material.

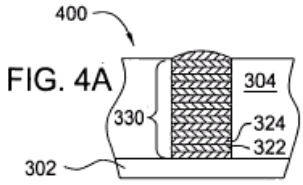
Examples:

Barrier layer 54s, 54d separates two layers of fill metal:



US6028362

Trench filled by alternating layers 322, 324, comprising e.g. Co and Ni:



US2006264043

References

Limiting references

This place does not cover:

Multistep plating forming a sequence of thin Cu films	H01L 21/76877

H01L 21/76849

{the layer being positioned on top of the main fill metal}

Definition statement

This place covers:

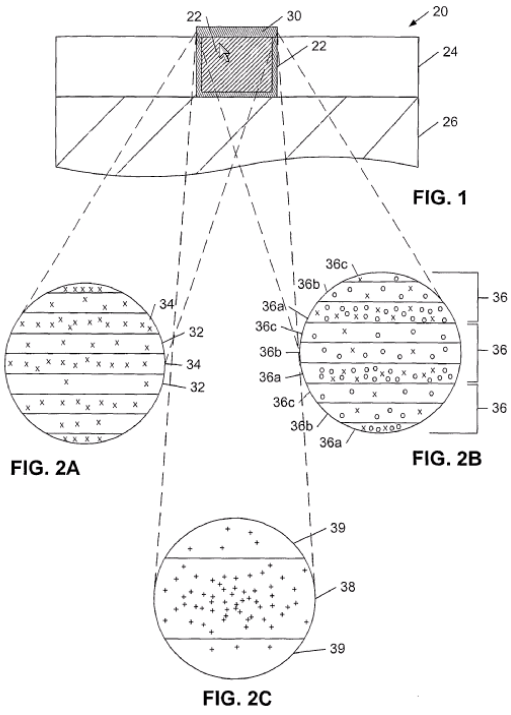
Conductive thin films, e.g. barrier, liner or adhesion layers, formed on top of an inlaid (i.e. damascene) conductor

Manufacture of electroless Co(Ni)WP capping layers on damascene conductors

CuSiN by siliciding and nitriding the surface of a Cu damascene conductor

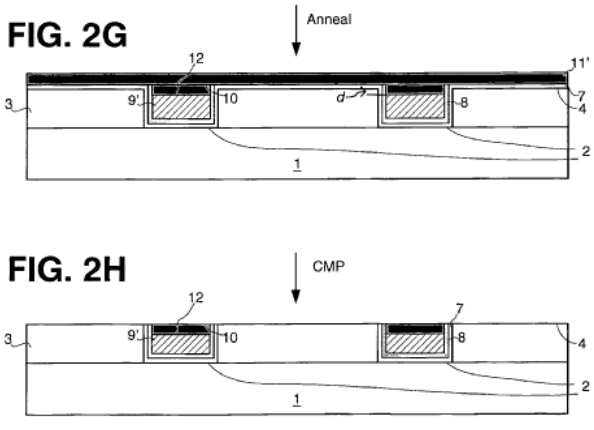
Examples:

Cap layer 30 (CoWP layer) comprises multiple layers having periodic variations in the concentration of chemical elements:



WO2006020566

Electromigration barrier formed by depositing a metal layer 11, diffusing the metal into the underlying conductor and removing the remainder of layer 11:



WO03052798

H01L 21/7685

{the layer covering a conductive structure (H01L 21/76849 takes precedence)}

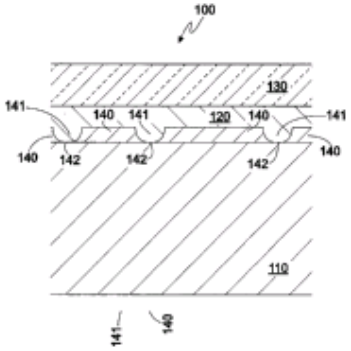
Definition statement

This place covers:

Thin functional conductive films covering interconnects not formed in an opening of a dielectric, e.g. on subtractive metal lines, e.g. a Ti/TiN adhesion/barrier stack on Al wiring.

Example:

Formation of a TiN layer (141) on an Al conductor (110). The method of fabrication avoids the formation of an unintentional Ti layer (140):



US2006099800

References

Limiting references

This place does not cover:

Barrier or adhesion layers being positioned on top of the main fill metal, e.g. thin films formed on top of inlaid conductors	H01L 21/76849

H01L 21/76852

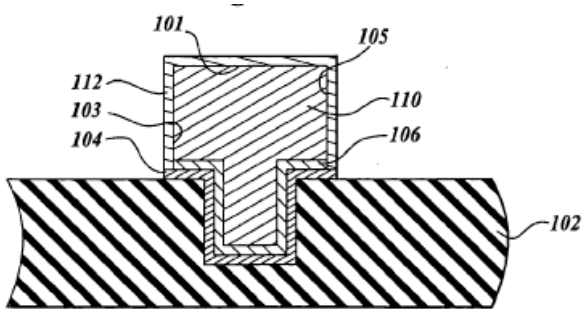
{the layer also covering the sidewalls of the conductive structure}

Definition statement

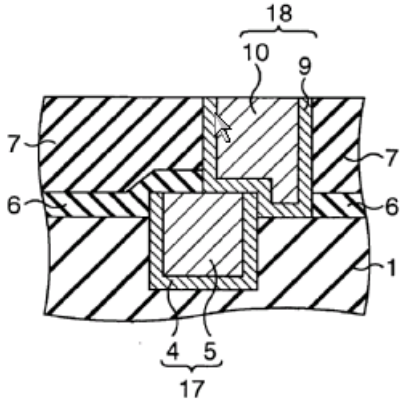
This place covers:

Barrier, adhesion or other liner layers on the sidewalls or on top and on the sidewalls of a freestanding, e.g. subtractive, interconnect.

Examples:



US2005230262



US 2006180920

H01L 21/76853

{characterized by particular after-treatment steps}

Definition statement

This place covers:

Conductive thin film treated in some way after it has been deposited. The resulting film must still be a conductive film.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Methods of formation of barrier layers other than PVD, CVD or deposition from a liquids	H01L 21/76867
Modifying permanently or temporarily the pattern or the conductivity of conductive members, e.g. formation of alloys, reduction of contact resistances	H01L 21/76886

H01L 21/76855

{After-treatment introducing at least one additional element into the layer}

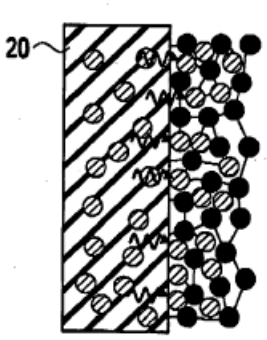
Definition statement

This place covers:

All methods introducing a new chemical element into the thin film, e.g. the reaction of the layer with the semiconductor substrate to form a silicide.

Example:

a titanium layer (black circles in the figure below) is deposited on the sidewalls of a dielectric layer, the Ti layer reacts with the oxygen (cross-hatched circles) contained in the dielectric during a later thermal step:



US2006214305

H01L 21/76856

{by treatment in plasmas or gaseous environments, e.g. nitriding a refractory metal liner}

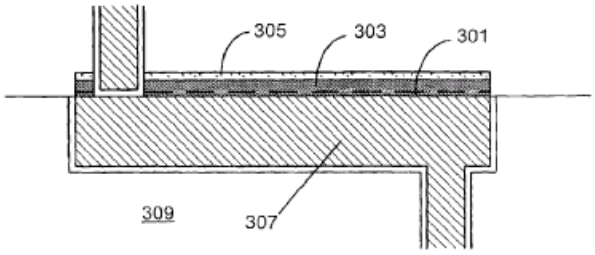
Definition statement

This place covers:

Contacting the thin film with a gas or a plasma so as to modify the composition of the layer, e.g. plasma nitriding.

Examples:

Refractive metal cap layer 303 is plasma nitrided to form a refractive metal nitride layer 305:



US6844258

Ru barrier layer 650b and a seed layer 666 are deposited in a trench, the seed layer is partially oxidized by exposing it to an oxidizing ambient. The oxide layer 667 serves as a protective layer and is dissolved when contacted with a plating bath:

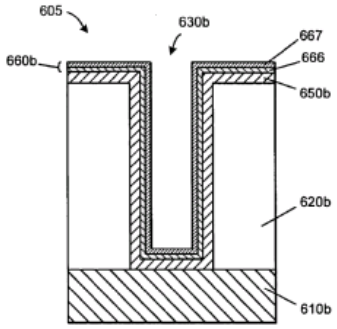


FIG. 6A

US2006223310

H01L 21/76858

{by diffusing alloying elements}

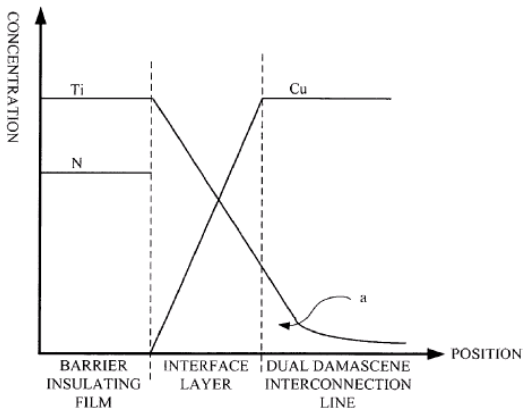
Definition statement

This place covers:

Introducing alloying elements, i.e. metallic elements, by diffusion into or reaction with pre-fabricated conductive thin film into.

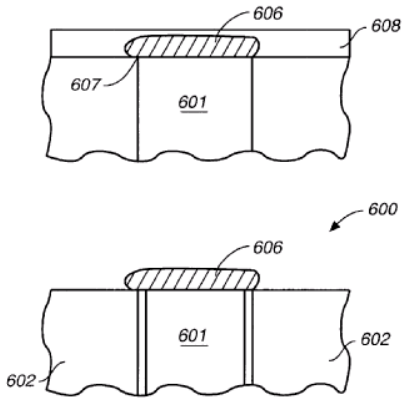
Examples:

A barrier layer, an adhesion layer (Ti), a seed layer and a Cu fill are formed in a dual damascene opening; after planarisation, a thermal treatment is carried out to react the adhesion layer with the Cu thereby forming an interface layer having a graded Cu content:



US2006154465

Conductive thin film 608 (Ca film) is formed over an inlaid Cu line (601) and heat treatment is performed to diffuse Cu from the line into the Ca layer thereby forming a CuCa capping layer (606). The unreacted material of layer 608 is subsequently removed:



US6566262

References

Limiting references

This place does not cover:

Layers itself being fabricated by the diffusion of alloying elements	H01L 21/76867

Special rules of classification

Diffusion is a bi-directional process, i.e. there can be cases where it cannot be unambiguously determined whether the final layer is the result of diffusing elements into the layer (which would constitute an example for the present class) or if the final film is the result of diffusing elements out of an original thin film, e.g. into the bulk conductor (this would pertain to H01L 21/76867, see the examples given there). In such cases both classes H01L 21/76858 and H01L 21/76867 should be assigned.

H01L 21/76859

{by ion implantation}

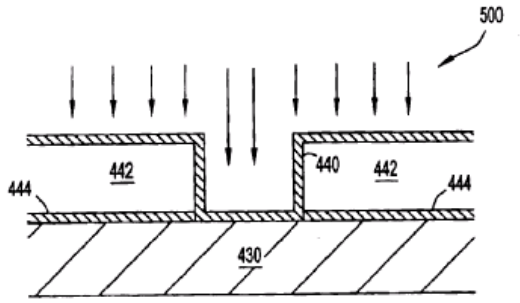
Definition statement

This place covers:

Implantation methods, i.e. methods allowing for precise control of the energy of the implanted ions as well as of the implantation depth.

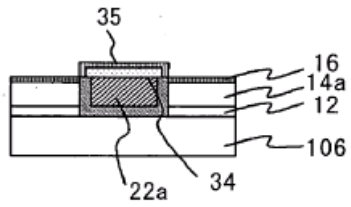
Examples:

Sn ions are implanted into barrier layer (440) in order to render the barrier amorphous and to introduce dopants having favourable electromigration properties:



US6835655

the surface of a CoWP capping layer (34) is nitrided by N2 ion implantation:



US2006175708

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Implantation in semiconductors	H01L 21/265
implantation in insulating layers	H01L 21/3105 or H01L 21/3115

H01L 21/76861

{Post-treatment or after-treatment not introducing additional chemical elements into the layer}

Definition statement

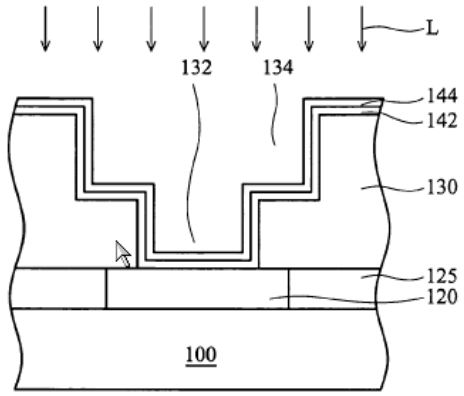
This place covers:

Methods for removing contaminants, e.g. oxides, from thin functional conductive films.

Methods for transforming their grain structure.

Example:

Oxides and other contaminants of a Cu seed layer (144) are removed by a wet-chemical treatment:



US2005245072

H01L 21/76862

{Bombardment with particles, e.g. treatment in noble gas plasmas; UV irradiation}

Definition statement

This place covers:

Contacting the film with plasmas or particles, e.g. high energy photons, while not introducing a new element into the film, e.g. treatment by UV irradiation for the removal of oxides.

Examples:

Barrier layer (Ti/TiN layer 118) is plasma treated to roughen the surface of the layer in the region 120. As a result, the number of nucleation sites is increased which slows down the growth of W layer 124:

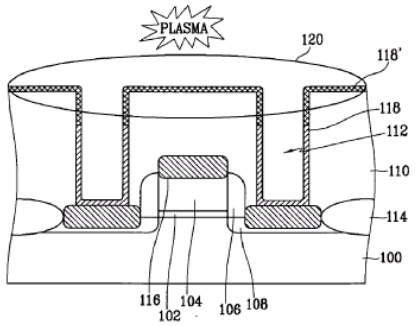
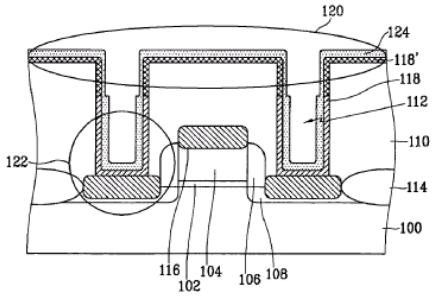


FIG.1D



US2005014358

Barrier layer (52) is subjected to a two-step redistribution process, i.e. overhanging portions (60) are removed and redistributed to reinforce sidewall regions (32, 34) where the PVD barrier is not

thick enough. In a first step, this redistribution is achieved by bombardment with Ar and Ta ions with simultaneous deposition of Ta, in the second step, only Ar is used for material redistribution:

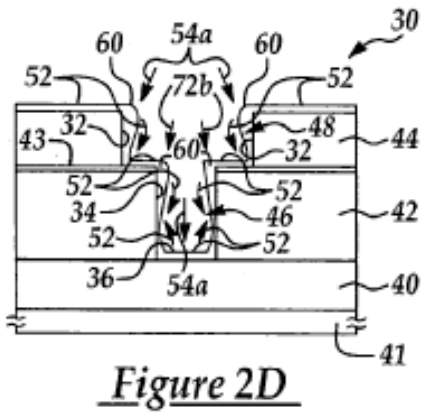


Figure 2D

US2005260851

H01L 21/76864

{Thermal treatment}

Definition statement

This place covers:

Thermal treatment of thin functional films not introducing additional elements into the film, e.g. plasma annealing

Examples:

a Cu seed layer (228) is locally heat treated in order to induce grain growth in the seed layer:

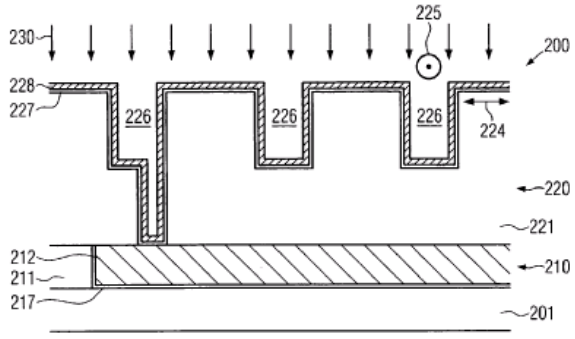
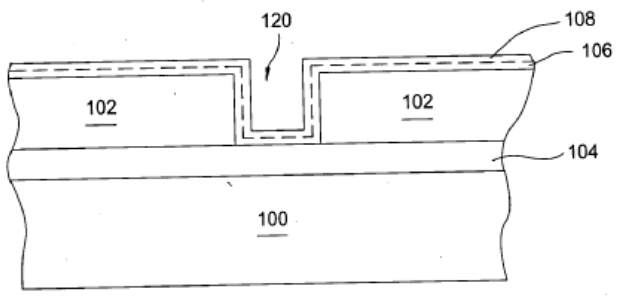


FIG. 2a

US2006223311

a Ru barrier/seed layer (108) is annealed after deposition to remove oxides or other contaminants prior to plating:



US2005274622

References

Limiting references

This place does not cover:

Film stacks, e.g. Ti/TiN and W, TaN/Ta and Cu, subjected to annealing after filling the contact hole	H01L 21/76877

Informative references

Attention is drawn to the following places, which may be of interest for search:

Seed layers treated by an annealing step	H01L 21/76873

Special rules of classification

"Plasma annealing" should be classified here and in H01L 21/76862.

Note that for assigning this group symbol it is important that it is the thin film per se which is subjected to the thermal treatment. Thermal treatment of the main conductor is classified in H01L 21/76838 or, if the main conductor is formed in an opening in a dielectric, in H01L 21/76883.

Thermal treatments for driving an alloying element into the thin metal film are not classified here but in H01L 21/76858.

H01L 21/76865

{Selective removal of parts of the layer (H01L 21/76844 takes precedence)}

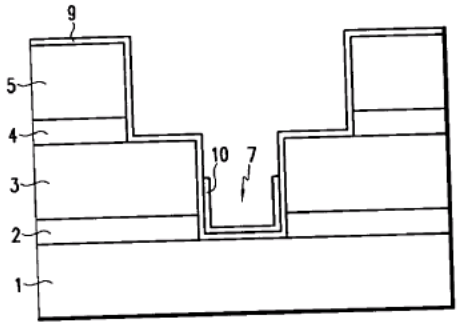
Definition statement

This place covers:

Removal of overhanging or "necking" portions of conductive thin films at the upper regions of via holes, or all cases where sputter etching and sputter deposition are carried out simultaneously.

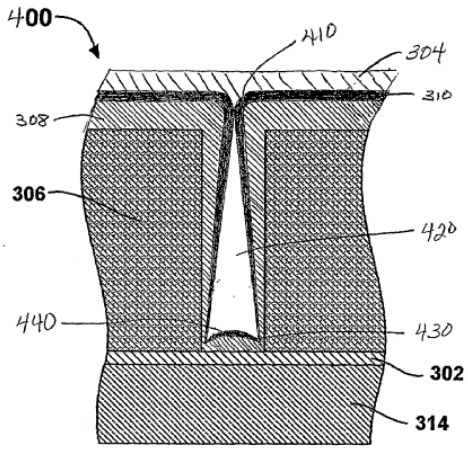
Examples:

Seed layer (10) is removed so as to provide a base layer for selective filling of the dual damascene trench;



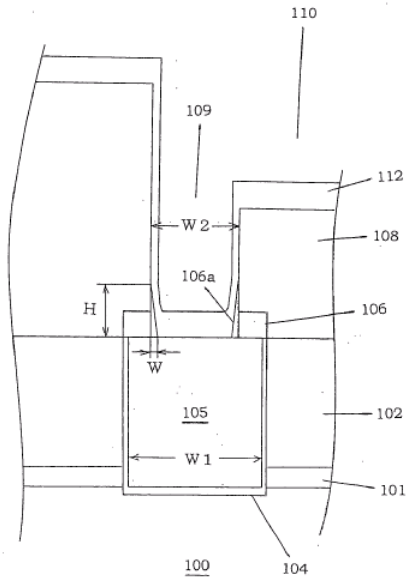
US2006094220

Overhanging portions of a barrier layer 308 and/or a Cu seed layer (310) are removed and redistributed by gas cluster ion beam (GCIB) processing:



WO2004044954

Capping layer (106) on an underlying conductor (105) is partially etched off by sputtering; the sputtered material of barrier (106) is redistributed on the via sidewalls to form a bottomless first barrier:



US2006264030

References

Limiting references

This place does not cover:

Forming a bottomless barrier	H01L 21/76844

Informative references

Attention is drawn to the following places, which may be of interest for search:

Selective removal of a seed layer for electroplating	H01L 21/76873

H01L 21/76867

{characterized by methods of formation other than PVD, CVD or deposition from a liquids (PVD H01L 21/2855; CVD H01L 21/28556; deposition from liquids H01L 21/288)}

Definition statement

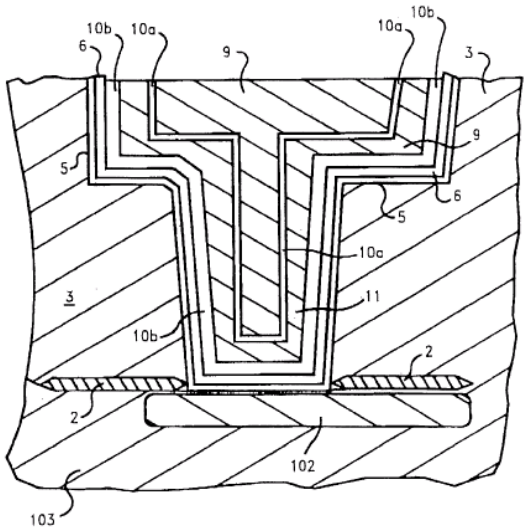
This place covers:

Formation of a functional conductive thin film, e.g. barrier, liner, adhesion or seed layers, by diffusing alloying elements such that they segregate at the surfaces of a conductor.

Diffusion of material from an initial thin film into a surface portion of the conductor, optionally followed by the removal of said initial thin film.

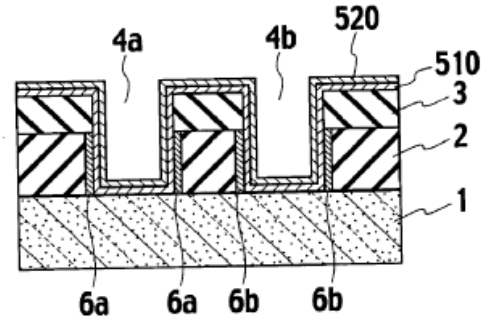
Examples:

A layer stack comprising a first barrier layer (6) and a metal layer (Hf, Zr, or Ti) suitable for forming an intermetallic compound with Cu is deposited in a dual damascene trench. A heat treatment forms layer (10b) comprising a compound of Cu and Hf, Zr, or Ti, while at the same time another compound layer (10a) is formed within the main conductor by diffusion of Hf, Zr, or Ti:



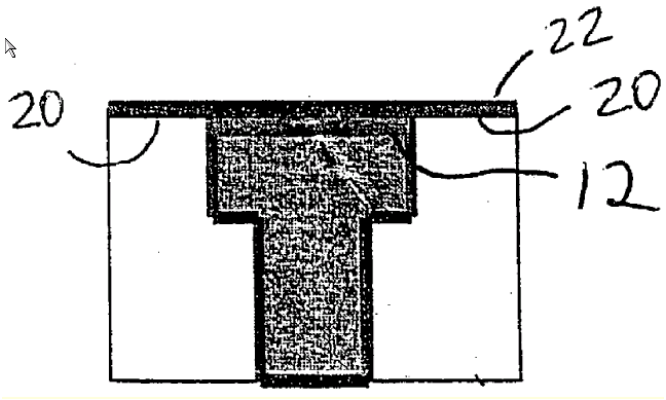
EP0881673

Barrier layer sections 6a, 6b are formed by diffusing material of the barrier layer 510 into the porous dielectric 2:



US2006154464

Al from Al layer 22 is diffused into inlaid Cu in order to form a CuAl electromigration barrier 12; the remaining unreacted Al layer is removed:



US2004207093

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

PVD	H01L 21/2855
CVD	H01L 21/28556
Deposition from liquids	H01L 21/288

H01L 21/76868

{Forming or treating discontinuous thin films, e.g. repair, enhancement or reinforcement of discontinuous thin films}

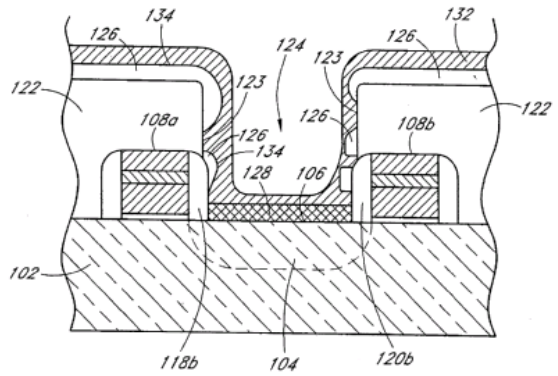
Definition statement

This place covers:

Methods specially adapted for either forming a discontinuous thin functional conductive film or for treating a discontinuous film so as to make it continuous, e.g. repair of seed layers.

Example:

Ti layer 126 is formed only incompletely on the sidewalls of contact hole 124; the TiSix layer 132 repairs the discontinuities in layer 126:



US2005233577

H01L 21/7687

{Thin films associated with contacts of capacitors}

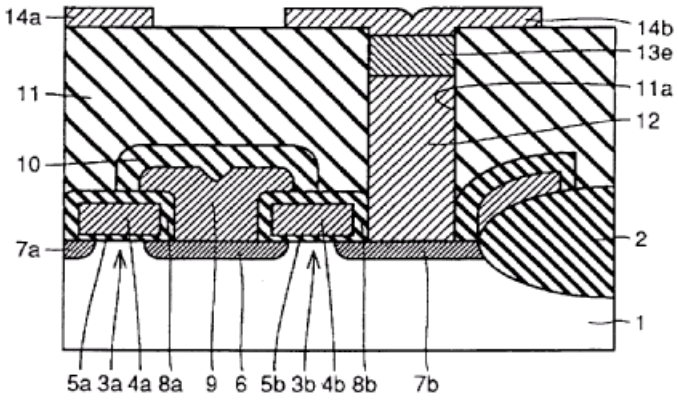
Definition statement

This place covers:

Thin conductive films formed in conjunction with the manufacture of contacts for capacitors

Example:

Formation of the barrier layer (13e):



US5699291

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Capacitor electrodes themselves	H10D 1/041, H10D 1/692

Special rules of classification

This group is intended to sort of "filter out" all documents related to capacitor contacts providing a solution to the very specific problems encountered during the manufacture of capacitors. The groups H01L 21/76843, H01L 21/7685, H01L 21/76853, H01L 21/76867 should also be given, provided "interesting" aspects which might also be of importance in the context of more conventional barriers are disclosed.

H01L 21/76871

{Layers specifically deposited to enhance or enable the nucleation of further layers, i.e. seed layers}

Definition statement

This place covers:

Formation of seed, wetting, nucleation or catalyst layers.

Special rules of classification

Whenever any one of the structural aspects covered by H01L 21/76843 or H01L 21/7685 applies the corresponding group symbol should be given in addition to the seed layer groups with the only

exception that "layer combinations", i.e. structures containing stacks of seed layers, are not classified in H01L 21/76846.

Whenever any one of the after-treatment or manufacturing aspects covered by H01L 21/76853, H01L 21/76867 or H01L 21/76868 applies the corresponding group should also be given.

Documents related to seed layers are classified in the head group H01L 21/76871 only if it is not clear which deposition method is envisaged or if the corresponding seed layer is suitable for all three of the deposition methods listed below.

H01L 21/76874

{for electroless plating}

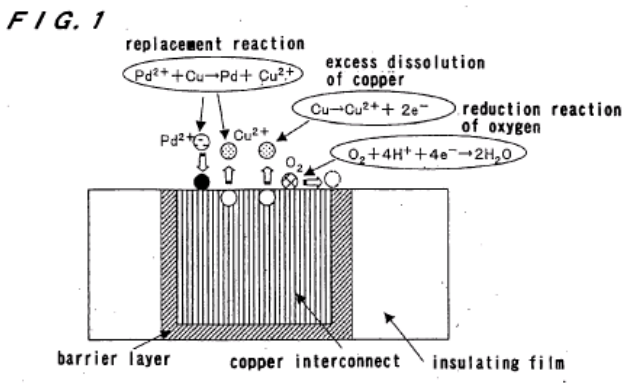
Definition statement

This place covers:

Seed layers specifically adapted for facilitating the deposition of conductive films by electroless plating

Examples:

Formation of a Pd catalyst layer for electroless CoWP deposition on top of an inlaid Cu interconnect:



EP1496542

Formation of a Pd catalyst layer for electroless Cu plating (The Pd seed is formed by plasma-immersion ion implantation into a TaN barrier layer):

FIG. 3B

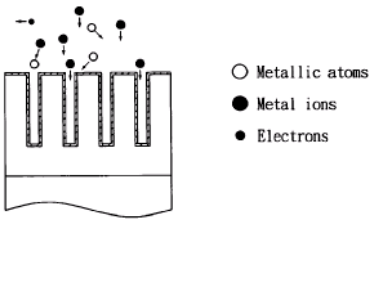


FIG. 3C

US2006040065

H01L 21/76879

{by selective deposition of conductive material in the vias, e.g. selective C.V.D. on semiconductor material, plating (plating on semiconductors in general H01L 21/288)}

Definition statement

This place covers:

Methods for selectively filling of vias or trenches in a dielectric layer with a conductive material, e.g. bottom up fill of a damascene opening not leading to a metal overburden on the field regions surrounding the opening.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Plating on semiconductors in general	H01L 21/288

Special rules of classification

If the deposition method is disclosed in some detail and includes one or more of PVD, CVD, ALD or liquid deposition, the corresponding group symbol H01L 21/2855, H01L 21/28556, H01L 21/28562, H01L 21/288 or H01L 21/2885 should also be assigned.

H01L 21/7688

{by deposition over sacrificial masking layer, e.g. lift-off (lift-off per se H01L 21/0272)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Lift-off of resists	H01L 21/0272
Lift-off of other layers	H01L 21/0331

H01L 21/76883

{Post-treatment or after-treatment of the conductive material}

Definition statement

This place covers:

After-treatment for improving or modifying the result of the process of filling an opening in a dielectric layer, e.g. a via hole or a damascene trench, with conductive material.Thermal treatments before or after polishing, e.g. to induce grain growth, removal of metal residues, plasma cleaning

References

Limiting references

This place does not cover:

Plasma treatment specifically adapted for forming a thin layer on the surface of the conductor	H01L 21/76849, H01L 21/76886
Reflowing the conductor or applying pressure so as to better fill the opening	H01L 21/76882
Oxidation or otherwise rendering (parts of) the conductor non-conductive	H01L 21/76888

Special rules of classification

The after-treatment is part of a multi-step process for forming a conductor in an opening in a dielectric. Cleaning of conductors per se is classified in H01L 21/02068 - H01L 21/02074.

H01L 21/76885

{By forming conductive members before deposition of protective insulating material, e.g. pillars, studs}

Definition statement

This place covers:

Conductors formed by through-mask plating

References

Limiting references

This place does not cover:

Formation of pillars, studs, bumps etc. for connecting the semiconductor substrate to other substrates	H01L 24/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Doping	H01L 21/265, H01L 21/38

H01L 21/76886

{Modifying permanently or temporarily the pattern or the conductivity of conductive members, e.g. formation of alloys, reduction of contact resistances}

Definition statement

This place covers:

Methods in which the properties of an otherwise completed conductive member of an interconnect, i.e. the main conductor, are modified, e.g. by introducing dopants into the conductor, alloying the main conductor with another metal

References

Limiting references

This place does not cover:

Smoothing; Planarisation	H01L 21/7684
Modification of thin functional conductive films such as barrier, adhesion, liner or seed layers	H01L 21/76855 - H01L 21/76864
Processes for fabricating fuses and anti-fuses are classified with the fuses and anti-fuses in	H01L 23/525

H01L 21/76897

{Formation of self-aligned vias or contact plugs, i.e. involving a lithographically uncritical step}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Self aligned silicidation on field effect transistors	H10D 30/0212

H01L 21/76898

{formed through a semiconductor substrate}

Definition statement

This place covers:

Establishing a conductive path extending through the substrate from the top surface to the bottom surface, e.g. through-silicon vias

Example

FIG. 1A

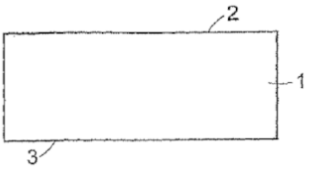


FIG. 1B

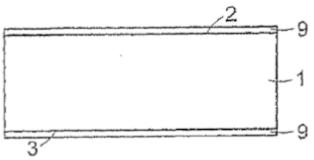


FIG. 1C

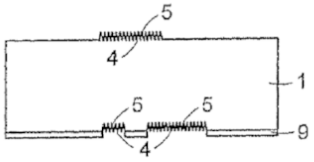


FIG. 1D

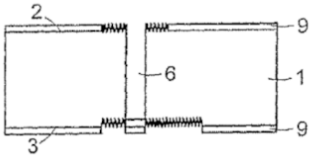


FIG. 1E

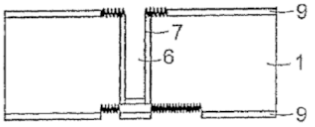


FIG. 1F

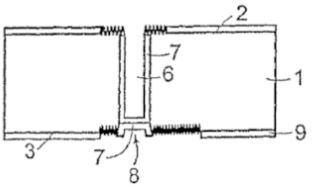
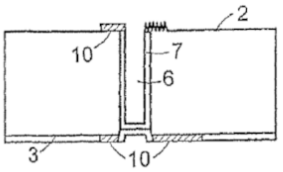


FIG. 1G



EP2426710A2

H01L 21/77

Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in, or on, a common substrate (manufacture or treatment of electronic memory devices H10B)

Definition statement

This place covers:

Processes for the division of a substrate into a plurality of individual devices.

References

Limiting references

This place does not cover:

Multistep methods for manufacturing random access memories [RAM] structures	H10B

H01L 21/78

with subsequent division of the substrate into plural individual devices (cutting to change the surface-physical characteristics or shape of semiconductor bodies H01L 21/304)

Definition statement

This place covers:

Multistep processes for singulating devices.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Single mechanical steps like cutting semiconductors	H01L 21/304
Laser dicing	B23K 26/00
Single mechanical steps of grinding, lapping and polishing in general	B24B
Fine working of crystals, e.g. semiconductors	B28D 5/00
Devices sensitive to light	H10F 39/00
Light emitting devices	H10H 20/00

H01L 21/7806

{involving the separation of the active layers from a substrate}

Definition statement

This place covers:

Separation of layers comprising active devices from the substrate, e.g. splitting after Epitaxial Lift-Off

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

ELO	Epitaxial Lift-Off

H01L 22/00

{Testing or measuring during manufacture or treatment; Reliability measurements, i.e. testing of parts without further processing to modify the parts as such; Structural arrangements therefor}

Definition statement

This place covers:

Application of testing and/or measuring procedures during the manufacturing processes of devices as defined under H01L 21/00, with the aim to

- detect defects, repair defects, sort defective devices / wafers
- control the semiconductor device fabrication process,
- with or without corrective action on the process,

which are specific to semiconductor device fabrication, e.g. end point determination.

Covers the measuring of a single parameter or variable

Relationships with other classification places

Processes which are not specific to semiconductor device fabrication or processes, where the semiconductor devices are included in a larger system, are typically not classified in H01L 22/00, but are classified in the relevant place for the processes or testing in general, e.g. G01N or G01R.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Detecting parts, counting parts, handling parts	H01L 21/67
Marks on wafers, test patterns on wafers	H01L 23/544
Means for detecting end-point in lapping or polishing machines	B24B 37/013
Analysing materials by determining their chemical or physical properties	G01N
Optical characterization of semiconductors	G01N 21/9501
Measuring electrical or magnetic variables	G01R
Multiple probes for testing, e.g. probe cards	G01R 1/073
Testing of individual devices, including on wafers, after manufacture	G01R 31/26
Testing of integrated circuits, including on wafers, after manufacture	G01R 31/28
Contactless testing of integrated circuits	G01R 31/302
Testing and controlling photoresist and lithographic patterns	G03F 7/70633
Multiple probes for testing, e.g. probe cards	G05B 19/418
Inspection of images, flaw detection	G06T 7/0002
Testing storing means, like memories, including repair	G11C 29/00
Measuring and control of plasma parameters	H01J 37/00, G01N

Controlling gas-filled discharge tubes, e.g. plasma machines, by information coming from substrate; end-point detection	H01J 37/32963
Testing of photovoltaic systems	H02S 50/00

H01L 22/10

{Measuring as part of the manufacturing process (burn-in G01R 31/2855)}

Definition statement

This place covers:

Methods for measurement of structural or electrical parameters as part of the device manufacturing process.

Measuring as part of the manufacturing process; the parameter may be for example the thickness of layers, refractive index of layers, line width, warp of wafers, bond strength, defect concentration, metallurgic parameters, diffusion depth, dopant concentration.

Relationships with other classification places

Measurement of parameters wherein the fabrication of semiconductor devices is not particularly relevant to the invention, or wherein the measurement of the parameter could equally be applied to the fabrication of other products than semiconductor products are typically not classified.

References

Limiting references

This place does not cover:

Procedures, i.e. sequence of activities consisting of a plurality of measurement and correction, marking or sorting steps	H01L 22/20

Informative references

Attention is drawn to the following places, which may be of interest for search:

Measurement of parameters which is not part of the device fabrication processMeasurement of parameters wherein the fabrication of semiconductor devices is not particularly relevant to the invention, and wherein the measurement of the parameter could equally be applied to the fabrication of other products than semiconductor devices	G01N or G01R.
Burn-in	G01R 31/2855

Special rules of classification

In H01L 22/00, the method for measuring a parameter is classified in H01L 22/20 as soon as it is part of a testing or controlling procedure.

H01L 22/12

{for structural parameters, e.g. thickness, line width, refractive index, temperature, warp, bond strength, defects, optical inspection, electrical measurement of structural dimensions, metallurgic measurement of diffusions (electrical measurement of diffusions H01L 22/14)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electrical measurement of diffusion regions	H01L 22/14

H01L 22/20

{Sequence of activities consisting of a plurality of measurements, corrections, marking or sorting steps}

Definition statement

This place covers:

Multi-step processes comprising at least a measuring step followed by a correcting, marking or sorting step.

References

Limiting references

This place does not cover:

Semiconductor factory control	G05B 19/418

Informative references

Attention is drawn to the following places, which may be of interest for search:

Procedures applied to semiconductor fabrication but wherein the fabrication of semiconductor devices is not particularly relevant to the invention and wherein the procedure could equally be applied to the fabrication of products other than semiconductor devices are typically classified in	G01N or G01R.

H01L 22/24

{Optical enhancement of defects or not directly visible states, e.g. selective electrolytic deposition, bubbles in liquids, light emission, colour change (voltage contrast G01R 31/311)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Voltage contrast	G01R 31/311

H01L 22/26

{Acting in response to an ongoing measurement without interruption of processing, e.g. endpoint detection, in-situ thickness measurement (endpoint detection arrangements in CMP apparatus B24B 37/013, in discharge apparatus H01J 37/32)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

methods for plasma etching end point control	H01J 37/32

Special rules of classification

End point process detection, when it is exclusively based on the use of a machine which has been designed for that purpose, need not to be classified in H01L 22/00.

H01L 22/34

{Circuits for electrically characterising or monitoring manufacturing processes, e. g. whole test die, wafers filled with test structures, on-board-devices incorporated on each die, process control monitors or pad structures thereof, devices in scribe line (switching, multiplexing, gating devices G01R 19/25; process control with lithography, e.g. dose control, G03F 7/20; structures for alignment control by optical means G03F 7/70633)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Process control influencing process steps in general, e.g. CD correction by etch or diffusion	H01L 22/20
Switching, multiplexing, gating devices	G01R 19/25
Process control with lithography, e.g. dose control	G03F 7/20
Structures for alignment control by optical means	G03F 9/7073

H01L 23/00

Details of semiconductor or other solid state devices (H01L 25/00 takes precedence {; structural arrangements for testing or measuring during manufacture or treatment, or for reliability measurements H01L 22/00; arrangements for connecting or disconnecting semiconductor or solid-state bodies, or methods related thereto H01L 24/00; finger print sensors G06V 40/12})

Definition statement

This place covers:

- Details of semiconductor or other solid state devices including

- Structural arrangements for protection of semiconductor or other solid state devices against mechanical damage or moisture
- Containers or seals
- Mountings
- Fillings or auxiliary members in containers of encapsulations
- Encapsulations
- Holders for supporting the complete device in operation
- Arrangements for cooling, heating, ventilating or temperature compensation
- Arrangements for conducting electric current to or from the solid state body in operation
- Arrangements for conducting electric current within the solid state body in operation
- Marks applied to semiconductor or other solid state devices
- Protection against radiation of semiconductor or other solid state devices
- Structural electrical arrangements for semiconductor or other solid state devices not otherwise provided for

References

Limiting references

This place does not cover:

Arrangements for connecting or disconnecting semiconductor or solid-state bodies, and methods related thereto	H01L 24/00
Assemblies consisting of a plurality of individual semiconductor or other solid state devices	H01L 25/00
Microstructural devices or systems, e.g. micromechanical devices	B81B
Solid state devices using organic materials as the active part, or using a combination of organic materials with other materials as the active part	H10K 99/00
Details peculiar to thermo-electric devices comprising a junction of dissimilar materials	H10N 10/00
Details peculiar to thermoelectric devices without a junction of dissimilar materials	H10N 15/00
Details peculiar to piezoelectric devices; electrostrictive devices; magnetostrictive devices	H10N 30/00
Details peculiar to devices using galvano-magnetic or similar magnetic effects	H10N 50/00
Details peculiar to devices using superconductivity	H10N 60/00
Details peculiar to solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier	H10N 70/00
Details peculiar to bulk negative resistance effect devices	H10N 80/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Non-electric welding by applying impact or other pressure, with or without the application of heat, e.g. cladding or plating	B23K 20/00
Laser working of semiconductors	B23K 26/0006, B23K 2101/40, B23K 2103/56

Rods, electrodes, materials, or media, for use in soldering, welding, or cutting	B23K 35/00
Injection moulding of electrical components	B29C 45/14639
Optical interconnections, e.g. light guides	G02B 6/00
Photolithography	G03F 7/00
Record carriers for use with machines and containing semiconductor elements (credit cards, id cards)	G06K 19/067
Structure or manufacture of flux-sensitive heads using magneto-resistive devices or effects	G11B 5/39
Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor	G11C 11/00
Apparatus or processes specially adapted for manufacturing, assembling, maintaining, or repairing of line connectors or current connectors or for joining electric conductors (soldering / welding)	H01R 43/00
Details peculiar to semiconductor devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation	H10F 39/00
Details peculiar to semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission	H10H 20/00

Special rules of classification

The use of Indexing Codes of the indexing scheme H01L 23/00 - H01L 23/66 is mandatory for additional information.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Parts	All structural units which are included in a complete device
Container	Enclosure forming part of the complete device and is essentially a solid construction in which the body of the device is placed, or which is formed around the body without forming an intimate layer thereon. Generally comprises a base, a lid and leads for electrical connection
Encapsulation	Enclosure which consists of one or more layers formed on the body and in intimate contact therewith

H01L 23/02

Containers; Seals (H01L 23/12, H01L 23/34, H01L 23/48, H01L 23/552, {H01L 23/66} take precedence; {for memories G11C})

References

Limiting references

This place does not cover:

Mountings	H01L 23/12

Arrangements for cooling, heating, ventilating or temperature compensation	H01L 23/34
Arrangements for conducting electric current to or from the solid state body in operation	H01L 23/48
Protection against radiation	H01L 23/552
High-frequency adaptations	H01L 23/66

Informative references

Attention is drawn to the following places, which may be of interest for search:

Housings for MEMs	B81B 7/0032
Housings for sensors in general	G01D 11/24
Housings for acceleration sensors	G01P 15/0802
Housings for computers	G06F 1/16
Housings for record carriers, e.g. memory cards	G06K 19/077
Housings for memories	G11C 5/04

H01L 23/055

the leads having a passage through the base {(H01L 23/057 takes precedence)}

References

Limiting references

This place does not cover:

The leads being parallel to the base	H01L 23/057

H01L 23/12

Mountings, e.g. non-detachable insulating substrates

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Chip carriers per se	H01L 23/498
Multi-chip modules in general	H01L 25/00
Printed circuit boards	H05K 1/00

H01L 23/147

{Semiconductor insulating substrates (semiconductor conductive substrates H01L 23/4926)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Semiconductor conductive substrates	H01L 23/4926

H01L 23/16

Fillings or auxiliary members in containers {or encapsulations}, e.g. centering rings (H01L 23/42, H01L 23/552 take precedence)

Definition statement

This place covers:

Additional parts and fillings within container or encapsulation, e.g. stiffeners, spacing layers.

References

Limiting references

This place does not cover:

Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling	H01L 23/42
Protection against radiation	H01L 23/552

H01L 23/20

gaseous at the normal operating temperature of the device

References

Limiting references

This place does not cover:

Materials for absorbing or reacting with moisture or other undesired substances	H01L 23/26

H01L 23/22

liquid at the normal operating temperature of the device

References

Limiting references

This place does not cover:

Materials for absorbing or reacting with moisture or other undesired substances	H01L 23/26

H01L 23/24

solid or gel at the normal operating temperature of the device {(H01L 23/3135 takes precedence)}

References

Limiting references

This place does not cover:

Materials for absorbing or reacting with moisture or other undesired substances	H01L 23/26
Double encapsulation or coating and encapsulation	H01L 23/3135

H01L 23/28

Encapsulations, e.g. encapsulating layers, coatings, {e.g. for protection} (H01L 23/552 takes precedence; {insulating layers for contacts or interconnections H01L 23/5329})

References

Limiting references

This place does not cover:

Protection against radiation	H01L 23/552

Informative references

Attention is drawn to the following places, which may be of interest for search:

Insulating layers for contacts or interconnections	H01L 23/5329

H01L 23/295

{containing a filler (H01L 23/296 takes precedence)}

References

Limiting references

This place does not cover:

Organo-silicon compounds	H01L 23/296

H01L 23/3157

{Partial encapsulation or coating (mask layer used as insulation layer H01L 21/31)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Mask layer used as insulation layer	H01L 21/31

H01L 23/3178

{Coating or filling in grooves made in the semiconductor body}

References

Limiting references

This place does not cover:

Fillings of grooves in memory cells (e.g. capacitors of RAMs)	H10B 12/00

H01L 23/32

Holders for supporting the complete device in operation, i.e. detachable fixtures (H01L 23/40 takes precedence)

References

Limiting references

This place does not cover:

Mountings or securing means for detachable cooling or heating arrangements	H01L 23/40

Informative references

Attention is drawn to the following places, which may be of interest for search:

Connectors, e.g. sockets, in general	H01R
For printed circuits	H05K

H01L 23/34

Arrangements for cooling, heating, ventilating or temperature compensation {; Temperature sensing arrangements (thermal treatment apparatus H01L 21/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thermal treatment apparatus	H01L 21/67098
Temperature control of computers	G06F 1/20
Thermal control of PCBs	H05K 1/0201

H01L 23/36

Selection of materials, or shaping, to facilitate cooling or heating, e.g. heatsinks {(H01L 23/28, H01L 23/40, H01L 23/42, H01L 23/44, H01L 23/46 take precedence; heating H01L 23/345)}

References

Limiting references

This place does not cover:

Encapsulations	H01L 23/28
Mountings or securing means for detachable cooling or heating arrangements	H01L 23/40
Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling	H01L 23/42
The complete device being wholly immersed in a fluid other than air	H01L 23/44
Involving the transfer of heat by flowing fluids	H01L 23/46

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for heating	H01L 23/345

H01L 23/367

Cooling facilitated by shape of device {(H01L 23/38, H01L 23/40, H01L 23/42, H01L 23/44, H01L 23/46 take precedence)}

References

Limiting references

This place does not cover:

Cooling arrangements using the Peltier effect	H01L 23/38

Mountings or securing means for detachable cooling or heating arrangements	H01L 23/40
Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling	H01L 23/42
Cooling arrangements with the complete device being wholly immersed in a fluid other than air	H01L 23/44
Cooling arrangements involving the transfer of heat by flowing fluids	H01L 23/46

H01L 23/3672

{Foil-like cooling fins or heat sinks (being part of lead-frames H01L 23/49568)}

References

Limiting references

This place does not cover:

Heat sinks being part of lead-frames	H01L 23/49568

H01L 23/3731

{Ceramic materials or glass (H01L 23/3732, H01L 23/3733, H01L 23/3735, H01L 23/3737, H01L 23/3738 take precedence)}

References

Limiting references

This place does not cover:

Cooling facilitated by selection of materials: diamonds	H01L 23/3732
Cooling facilitated by selection of materials: having a heterogeneous or anisotropic structure	H01L 23/3733
Cooling facilitated by selection of materials: laminates or multilayers	H01L 23/3735
Cooling facilitated by selection of materials: organic materials with or without a thermoconductive filler	H01L 23/3737
Cooling facilitated by selection of materials: semiconductor materials	H01L 23/3738

H01L 23/3732

{Diamonds}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Diamond per se	C30B 29/04

H01L 23/3733

{having a heterogeneous or anisotropic structure, e.g. powder or fibres in a matrix, wire mesh, porous structures (H01L 23/3732, H01L 23/3737 take precedence)}

References

Limiting references

This place does not cover:

Cooling facilitated by selection of materials: diamonds	H01L 23/3732
Cooling facilitated by selection of materials: organic materials with or without a thermoconductive filler	H01L 23/3737

H01L 23/3736

{Metallic materials (H01L 23/3732, H01L 23/3733, H01L 23/3735, H01L 23/3737, H01L 23/3738 take precedence)}

References

Limiting references

This place does not cover:

Cooling facilitated by selection of materials: diamonds	H01L 23/3732
Cooling facilitated by selection of materials: having a heterogeneous or anisotropic structure	H01L 23/3733
Cooling facilitated by selection of materials: laminates or multilayers	H01L 23/3735
Cooling facilitated by selection of materials: organic materials with or without a thermoconductive filler	H01L 23/3737
Cooling facilitated by selection of materials: semiconductor materials	H01L 23/3738

H01L 23/4012

{for stacked arrangements of a plurality of semiconductor devices (assemblies per se H01L 25/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Assemblies consisting of a plurality of individual semiconductor or other solid-state bodies	H01L 25/00

H01L 23/42

Fillings or auxiliary members in containers {or encapsulations} selected or arranged to facilitate heating or cooling

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Heating	H01L 23/345
Selection of materials for the device	H01L 23/373

H01L 23/427

Cooling by change of state, e.g. use of heat pipes {(by liquefied gas H01L 23/445)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cooling by liquefied gas	H01L 23/445

H01L 23/4334

{Auxiliary members in encapsulations (H01L 23/49568 takes precedence)}

References

Limiting references

This place does not cover:

Leadframes specifically adapted to facilitate heat dissipation	H01L 23/49568

H01L 23/44

the complete device being wholly immersed in a fluid other than air {(H01L 23/427 takes precedence)}

References

Limiting references

This place does not cover:

Cooling by change of state	H01L 23/427

H01L 23/46

involving the transfer of heat by flowing fluids (H01L 23/42, H01L 23/44 take precedence)

References

Limiting references

This place does not cover:

Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling	H01L 23/42
Cooling arrangements with the complete device being wholly immersed in a fluid other than air	H01L 23/44

H01L 23/467

by flowing gases, e.g. air {(H01L 23/473 takes precedence)}

References

Limiting references

This place does not cover:

Cooling involving the transfer of heat by flowing liquids	H01L 23/473

H01L 23/473

by flowing liquids {(H01L 23/4332, H01L 23/4338 take precedence)}

References

Limiting references

This place does not cover:

Auxiliary members in containers: bellows	H01L 23/4332
Auxiliary members in containers: pistons	H01L 23/4338

H01L 23/4735

{Jet impingement (H01L 23/4336 takes precedence)}

References

Limiting references

This place does not cover:

Auxiliary members in containers: in combination with jet impingement	H01L 23/4336

H01L 23/48

Arrangements for conducting electric current to or from the solid state body in operation, e.g. leads, terminal arrangements {; Selection of materials therefor}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for connecting or disconnecting semiconductor or other solid-state bodies, and methods related thereto	H01L 24/00
Terminals, leads in general	H01R

H01L 23/482

consisting of lead-in layers inseparably applied to the semiconductor body {(electrodes)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electrodes of semiconductor devices	H10D 64/00

H01L 23/485

consisting of layered constructions comprising conductive layers and insulating layers, e.g. planar contacts {(H01L 23/4821, H01L 23/4822, H01L 23/4824, H01L 23/4825 take precedence; materials H01L 23/532, bond pads H01L 24/02, bump connectors H01L 24/10)}

References

Limiting references

This place does not cover:

Lead-in layers inseparably applied to the semiconductor body: bridge structures with air gap	H01L 23/4821
Lead-in layers inseparably applied to the semiconductor body: beam leads	H01L 23/4822
Lead-in layers inseparably applied to the semiconductor body: pads with extended contours	H01L 23/4824
Lead-in layers inseparably applied to the semiconductor body: for devices consisting of semiconductor layers on insulating or semi-insulating substrates	H01L 23/4825
Materials	H01L 23/532
Bond pads	H01L 24/02
Bump connectors	H01L 24/10

H01L 23/488

consisting of soldered {or bonded} constructions {(bump connectors H01L 24/01)}

References

Limiting references

This place does not cover:

Bump connectors	H01L 24/01

H01L 23/495

Lead-frames {or other flat leads (H01L 23/498 takes precedence; lead frame interconnections between components H01L 23/52)}

References

Limiting references

This place does not cover:

Leads on insulating substrates	H01L 23/498

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnections between components using lead-frames	H01L 23/52

H01L 23/49506

{an insulative substrate being used as a diepad, e.g. ceramic, plastic (H01L 23/49531 takes precedence)}

References

Limiting references

This place does not cover:

Lead-frames with additional leads being a wiring board	H01L 23/49531

H01L 23/49544

{Deformation absorbing parts in the lead frame plane, e.g. meanderline shape (H01L 23/49562 takes precedence)}

References

Limiting references

This place does not cover:

Lead-frames: geometry for individual devices of subclass H10D	H01L 23/49562

H01L 23/49548

{Cross section geometry (H01L 23/49562 takes precedence)}

References

Limiting references

This place does not cover:

Lead-frames: geometry for individual devices of subclass H10D	H01L 23/49562

H01L 23/49572

{consisting of thin flexible metallic tape with or without a film carrier (H01L 23/49503 - H01L 23/49568 and H01L 23/49575 - H01L 23/49579 take precedence)}

References

Limiting references

This place does not cover:

Thin flexible metallic tape with or without a film carrier provided in the context of subject-matter covered by groups H01L 23/49503 - H01L 23/49568 and H01L 23/49575 - H01L 23/49579	H01L 23/49503 - H01L 23/49568 and; H01L 23/49575 - H01L 23/49579

H01L 23/498

Leads, {i.e. metallisations or lead-frames} on insulating substrates, {e.g. chip carriers (shape of the substrate H01L 23/13)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Shape of the substrate	H01L 23/13

H01L 23/49811

{Additional leads joined to the metallisation on the insulating substrate, e.g. pins, bumps, wires, flat leads (H01L 23/49827 takes precedence)}

References

Limiting references

This place does not cover:

Leads on insulating substrates: via connections through the substrates	H01L 23/49827

H01L 23/49822

{Multilayer substrates (multilayer metallisation on monolayer substrate H01L 23/498)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multilayer metallisation on monolayer substrate	H01L 23/498

H01L 23/49827

{Via connections through the substrates, e.g. pins going through the substrate, coaxial cables (H01L 23/49822, H01L 23/49833, H01L 23/4985, H01L 23/49861 take precedence)}

References

Limiting references

This place does not cover:

Leads on insulating substrates: multilayer substrates	H01L 23/49822
Leads on insulating substrates: consisting of a plurality of insulating substrates	H01L 23/49833
Leads on insulating substrates: flexible insulating substrates	H01L 23/4985
Leads on insulating substrates: lead-frames fixed on or encapsulated in insulating substrates	H01L 23/49861

H01L 23/4985

{Flexible insulating substrates (H01L 23/49572 and H01L 23/49855 take precedence)}

References

Limiting references

This place does not cover:

Lead-frames consisting of thin flexible metallic tape with or without a film carrier	H01L 23/49572
Leads on insulating substrates: for flat-cards, e.g. credit cards	H01L 23/49855

H01L 23/49855

{for flat-cards, e.g. credit cards (cards per se G06K 19/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cards per se	G06K 19/00

H01L 23/49861

{Lead-frames fixed on or encapsulated in insulating substrates (H01L 23/4985, H01L 23/49805 take precedence)}

References

Limiting references

This place does not cover:

Leads on insulating substrates: the leads being also applied on the sidewalls or the bottom of the substrate	H01L 23/49805
Leads on insulating substrates: flexible insulating substrates	H01L 23/4985

H01L 23/49866

{characterised by the materials (materials of the substrates H01L 23/14, of the lead-frames H01L 23/49579)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Materials of the substrates	H01L 23/14
Materials of the lead-frames	H01L 23/49579
Conductive materials for PCBs	**H05K/09D**

H01L 23/49877

{Carbon, e.g. fullerenes (superconducting fullerenes H10N 60/853)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Superconducting fullerenes	H10N 60/853

H01L 23/49883

{the conductive materials containing organic materials or pastes, e.g. for thick films (for printed circuits H05K 1/092)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

For printed circuits	H05K 1/092

H01L 23/50

for integrated circuit devices, {e.g. power bus, number of leads} (H01L 23/482 - H01L 23/498 take precedence)

References

Limiting references

This place does not cover:

Arrangements for conducting electric current to or from the solid state body in operation: lead-in layers inseparably applied to the semiconductor body	H01L 23/482
Leads on insulating substrates	H01L 23/498

H01L 23/5222

{Capacitive arrangements or effects of, or between wiring layers (other capacitive arrangements H01L 23/642)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Other capacitive arrangements	H01L 23/642

H01L 23/5227

{Inductive arrangements or effects of, or between, wiring layers (other inductive arrangements H01L 23/645)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Other inductive arrangements	H01L 23/645

H01L 23/5228

{Resistive arrangements or effects of, or between, wiring layers (other resistive arrangements H01L 23/647)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Other resistive arrangements	H01L 23/647

H01L 23/528

Layout of the interconnection structure

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Algorithms, e.g. computer aided design of layouts of integrated circuits	G06F 30/00

H01L 23/53209

{based on metals, e.g. alloys, metal silicides (H01L 23/53285 takes precedence)}

References

Limiting references

This place does not cover:

Arrangements for conducting electric current within the device in operation from one component to another: containing superconducting materials	H01L 23/53285

H01L 23/53276

{containing carbon, e.g. fullerenes (superconducting fullerenes H10N 60/853)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Nanosized carbon materials per se	C01B 32/15
Superconducting fullerenes	H10N 60/853

H01L 23/535

including internal interconnections, e.g. cross-under constructions {(internal lead connections H01L 23/481)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Internal lead connections	H01L 23/481

H01L 23/538

the interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates ({H05K takes precedence; manufacture or treatment H01L 21/4846} ; mountings per se H01L 23/12; {materials H01L 23/49866})

References

Limiting references

This place does not cover:

Printed circuits; casings or constructional details of electric apparatus; manufacture of assemblages of electrical components	H05K

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment	H01L 21/4846
Mountings per se	H01L 23/12
Materials	H01L 23/49866

H01L 23/5383

{Multilayer substrates (H01L 23/5385 takes precedence; multilayer metallisation on monolayer substrates H01L 23/538)}

References

Limiting references

This place does not cover:

Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: assembly of a plurality of insulating substrates	H01L 23/5385

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multilayer metallisation on monolayer substrates	H01L 23/538

H01L 23/5384

{Conductive vias through the substrate with or without pins, e.g. buried coaxial conductors (H01L 23/5383, H01L 23/5385 take precedence; pins attached to insulating substrates H01L 23/49811)}

References

Limiting references

This place does not cover:

Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: multilayer substrates	H01L 23/5383
Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: assembly of a plurality of insulating substrates	H01L 23/5385

Informative references

Attention is drawn to the following places, which may be of interest for search:

Pins attached to insulating substrates	H01L 23/49811

H01L 23/5387

{Flexible insulating substrates (H01L 23/5388 takes precedence)}

References

Limiting references

This place does not cover:

Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: for flat cards, e.g. credit cards	H01L 23/5388

H01L 23/5388

{for flat cards, e.g. credit cards (cards per se G06K 19/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Cards per se	G06K 19/00

H01L 23/544

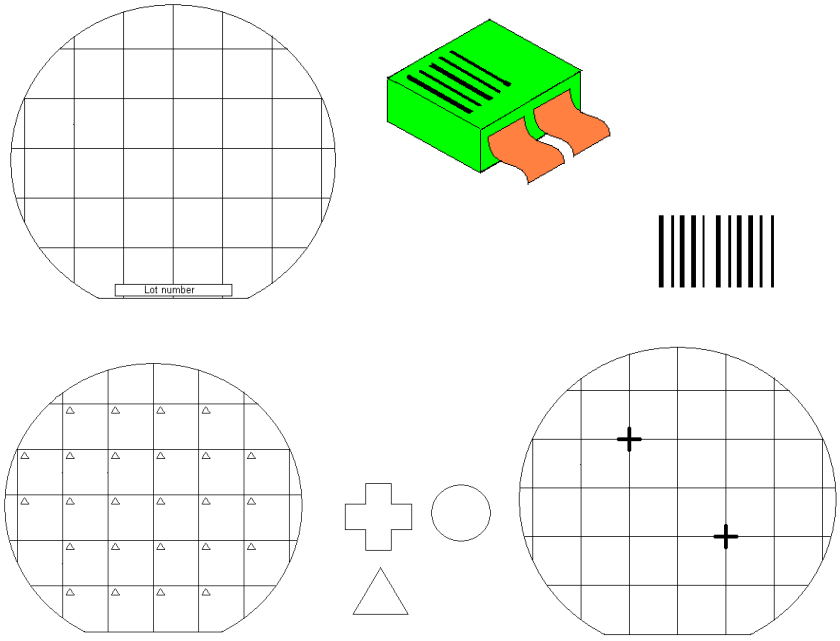
Marks applied to semiconductor devices {or parts}, e.g. registration marks, {alignment structures, wafer maps (test patterns for characterising or monitoring manufacturing processes H01L 22/00)}

Definition statement

This place covers:

Marks for identification purposes, including electrical structures used to generate identification information for electrical read out.

Typical views of marks of this type:



References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Marking devices, scribers	B25H 7/04
Marking methods	B41M 5/00
Marks used for overlay monitoring in photolithography	G03F 7/70633
Alignment marks used in photolithographic machines	G03F 9/7073

H01L 23/552

Protection against radiation, e.g. light {or electromagnetic waves}

Definition statement

This place covers:

Electromagnetic shielding arrangements; RF interference suppression.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electrostatic shielding in general	H05F 3/00
Screening of apparatuses or components of PCB	H05K 9/00

H01L 23/58

Structural electrical arrangements for semiconductor devices not otherwise provided for {, e.g. in combination with batteries (H01L 23/49593, H01L 23/49596 take precedence)}

References

Limiting references

This place does not cover:

Lead-frames: battery in combination with a lead-frame	H01L 23/49593
Lead-frames: oscillators in combination with a lead-frame	H01L 23/49596

H01L 23/585

{comprising conductive layers or plates or strips or rods or rings (H01L 23/60, H01L 23/62, H01L 23/64, H01L 23/66 take precedence)}

Definition statement

This place covers:

Active and passive measures to prevent or detect tampering; reverse engineering protection structures; seal rings, protection against delamination of layers during dicing

References

Limiting references

This place does not cover:

Protection against electrostatic charges or discharges	H01L 23/60
Protection against overvoltage	H01L 23/62
Impedance arrangements	H01L 23/64
High-frequency adaptations	H01L 23/66

Informative references

Attention is drawn to the following places, which may be of interest for search:

Secure housings for data carriers (memories)	G06F 21/86
Protective means for data carriers (memories)	G06K 19/073

H01L 23/60

Protection against electrostatic charges or discharges, e.g. Faraday shields

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Faraday shields in general	H05F 3/00
Protection against electrostatic discharge (ESD) provided in a semiconductor body	H10D 89/60

H01L 23/642

{Capacitive arrangements (H01L 23/49589, H01L 23/645, H01L 23/647, H01L 23/66 take precedence; capacitive effects between wiring layers on the semiconductor body H01L 23/5222)}

References

Limiting references

This place does not cover:

Lead-frames: capacitor integral with or on the lead-frame	H01L 23/49589
Impedance arrangements: inductive arrangements	H01L 23/645
Impedance arrangements: resistive arrangements	H01L 23/647
High-frequency adaptations	H01L 23/66

Informative references

Attention is drawn to the following places, which may be of interest for search:

Capacitive effects between wiring layers on the semiconductor body	H01L 23/5222

H01L 23/645

{Inductive arrangements (H01L 23/647, H01L 23/66 take precedence)}

References

Limiting references

This place does not cover:

Impedance arrangements: resistive arrangements	H01L 23/647
High-frequency adaptations	H01L 23/66

Informative references

Attention is drawn to the following places, which may be of interest for search:

Inductors formed within interconnection layers	H01L 23/5227

H01L 23/647

{Resistive arrangements (H01L 23/66, H01L 23/62 take precedence)}

References

Limiting references

This place does not cover:

Protection against overvoltage	H01L 23/62
High-frequency adaptations	H01L 23/66

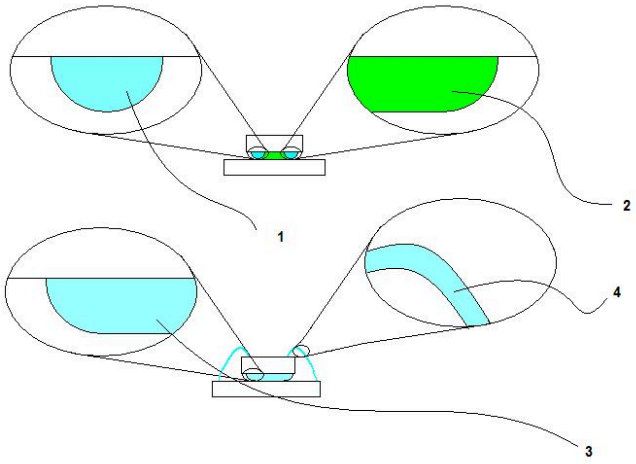
H01L 24/00

{Arrangements for connecting or disconnecting semiconductor or solid-state bodies; Methods or apparatus related thereto}

Definition statement

This place covers:

Examples of first level interconnects



1 = H01L 24/10 and subgroups,

2 = H01L 24/26 and subgroups,

3 = H01L 24/26 and subgroups,

4 = H01L 24/42 and subgroups

References

Limiting references

This place does not cover:

Manufacture or treatment of parts	H01L 21/48
Assemblies of semiconductor devices	H01L 21/50 - H01L 21/568

Applying interconnections to be used for carrying current between separate components within a device	H01L 21/768
Containers or seals	H01L 23/02 - H01L 23/10
Mountings	H01L 23/12 - H01L 23/15
Arrangements for cooling, heating, ventilating or temperature compensation	H01L 23/34 - H01L 23/4735
Arrangements for conducting electric current	H01L 23/48 - H01L 23/50 and H01L 23/52 - H01L 23/5389
Structural electrical arrangements	H01L 23/58 - H01L 23/66
Assemblies consisting of a plurality of individual semiconductor or other solid state devices	H01L 25/00 - H01L 25/18
Printed circuits	H05K 1/00 - H05K 1/189
Apparatus or manufacturing processes for printed circuits	H05K 3/00 - H05K 3/4685
Details peculiar to solid state devices using organic materials as the active part, or using a combination of organic materials with other materials as the active part	H10K 99/00
Details peculiar to thermoelectric devices comprising a junction of dissimilar materials	H10N 10/00
Details peculiar to thermoelectric devices without a junction of dissimilar materials or of thermomagnetic devices	H10N 15/00
Details peculiar to piezoelectric, electrostrictive, magnetostrictive devices in general	H10N 30/00
Details peculiar to devices using galvano-magnetic or similar magnetic effects	H10N 50/00
Details peculiar to devices using superconductivity	H10N 60/00
Details peculiar to solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier or of Ovshinsky-effect devices	H10N 70/00
Details peculiar to bulk negative resistance effect devices	H10N 80/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Details of semiconductor bodies or electrodes of semiconductor devices adapted for rectifying, amplifying, oscillating or switching, or capacitors or resistors with at least one potential-jump barrier or surface barrier	H10D 89/00
Details peculiar to semiconductor devices sensitive to infrared radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation	H10F 39/00
Details peculiar to semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission	H10H 20/00

Special rules of classification

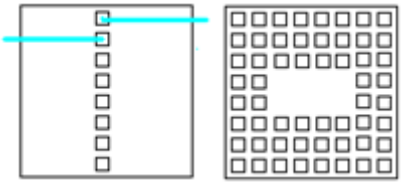
The use of Indexing Codes of the indexing schemes H01L 24/00 and subgroups, H01L 2224/00 and subgroups and H01L 2924/00 and subgroups is mandatory.

H01L 24/02

{Bonding areas (on insulating substrates, e.g. chip carriers, H01L 23/49816, H01L 23/49838, H01L 23/5389); Manufacturing methods related thereto}

Definition statement

This place covers:



References

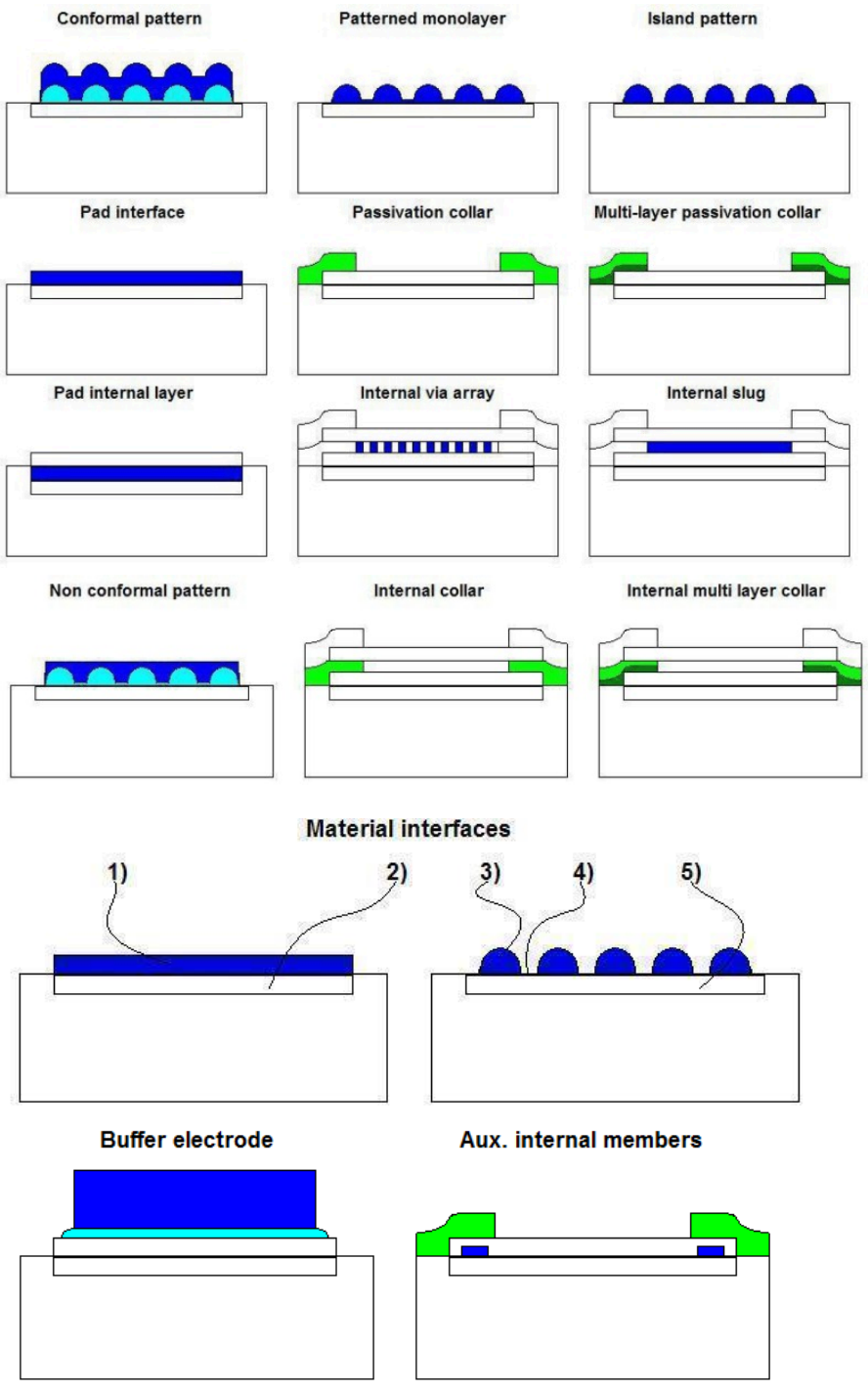
Informative references

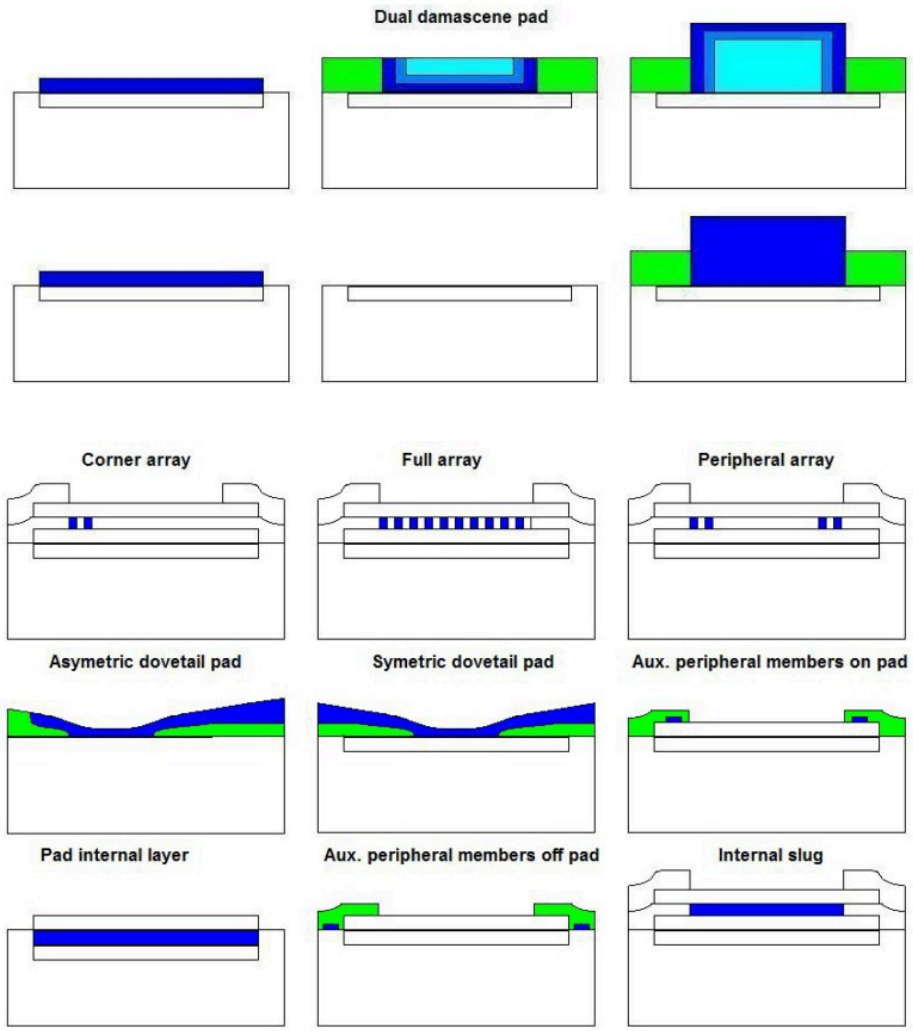
Attention is drawn to the following places, which may be of interest for search:

Bonding areas on insulating substrates, e.g. chip carriers	H01L 23/49816, H01L 23/49838, H01L 23/5389

Special rules of classification

The following figures show some key technologies relating to H01L 24/00





H01L 24/06

{of a plurality of bonding areas}

References

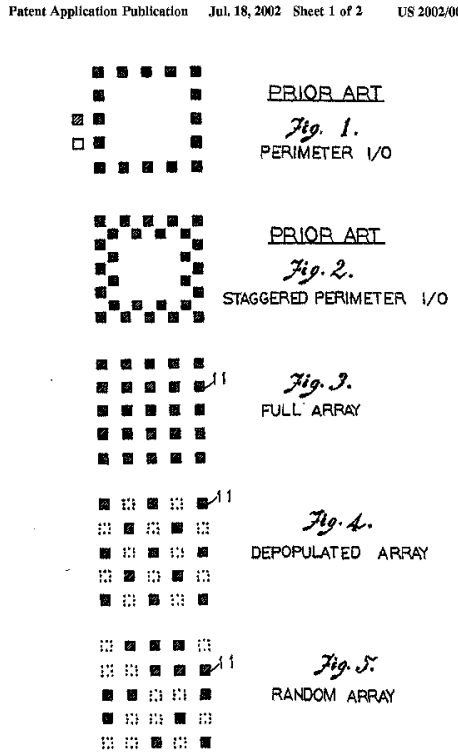
Informative references

Attention is drawn to the following places, which may be of interest for search:

Physical circuit design	G06F 30/39

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:



H01L 24/10

{Bump connectors (bumps on insulating substrates, e.g. chip carriers, H01L 23/49816); Manufacturing methods related thereto}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

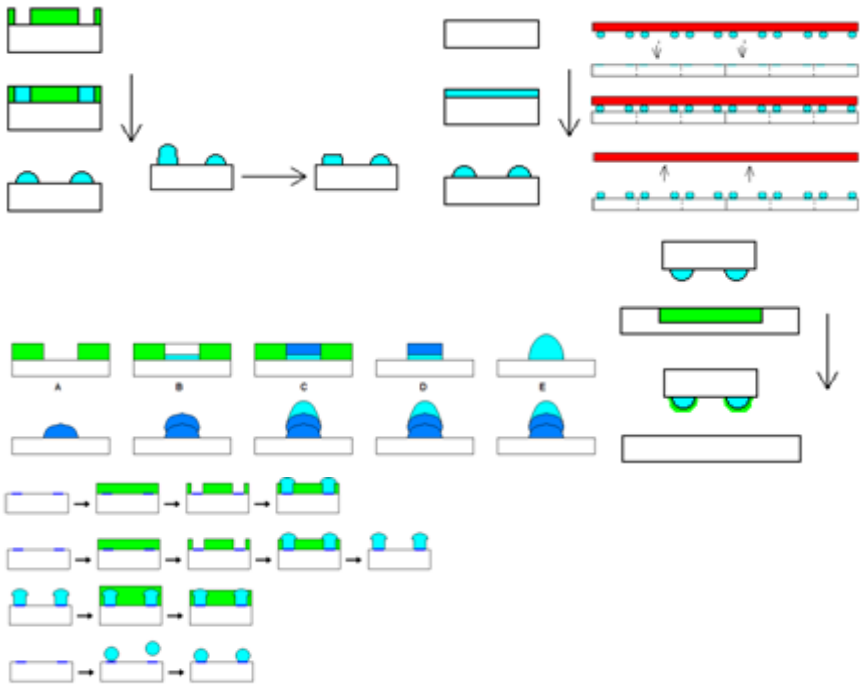
Bumps on insulating substrates, e.g. chip carriers	H01L 23/49816

H01L 24/11

{Manufacturing methods (for bumps on insulating substrates H01L 21/4853)}

Definition statement

This place covers:



References

Informative references

Attention is drawn to the following places, which may be of interest for search:

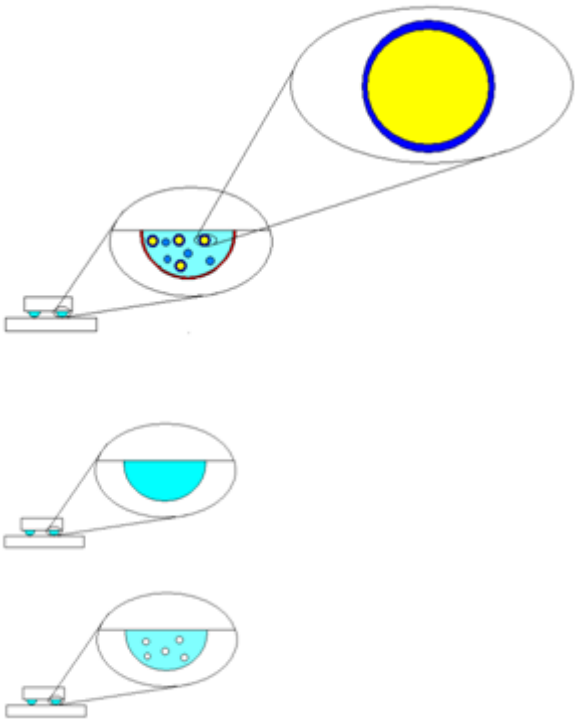
Manufacturing methods for bumps on insulating substrates	H01L 21/4853
Inks, e.g. metallic inks	C09D 11/00

H01L 24/12

{Structure, shape, material or disposition of the bump connectors prior to the connecting process}

Definition statement

This place covers:

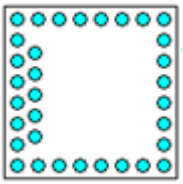


H01L 24/14

{of a plurality of bump connectors}

Definition statement

This place covers:



H01L 24/18

{High density interconnect [HDI] connectors; Manufacturing methods related thereto (interconnection structure between a plurality of semiconductor chips H01L 23/5389)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

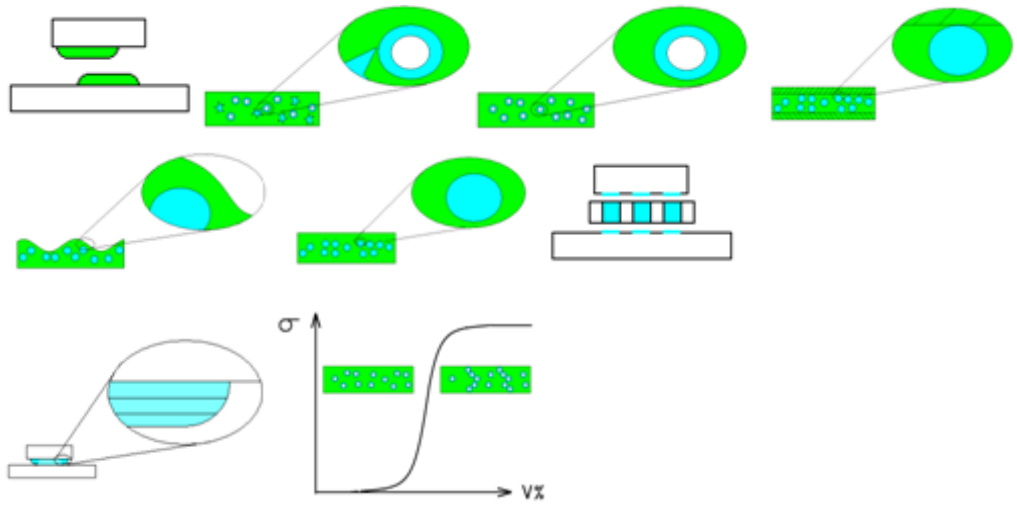
Interconnection structure between a plurality of semiconductor chips	H01L 23/5389

H01L 24/26

{Layer connectors, e.g. plate connectors, solder or adhesive layers; Manufacturing methods related thereto}

Definition statement

This place covers:



References

Informative references

Attention is drawn to the following places, which may be of interest for search:

metal powder in organic matrix	H01B 1/22

H01L 24/27

{Manufacturing methods}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Applying fluids in general	B05C 9/02

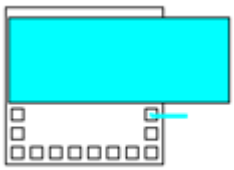
Applying adhesive films using preforms	B65H 37/02

H01L 24/34

{Strap connectors, e.g. copper straps for grounding power devices; Manufacturing methods related thereto}

Definition statement

This place covers:



H01L 24/50

{Tape automated bonding [TAB] connectors, i.e. film carriers; Manufacturing methods related thereto (thin flexible metallic tape with or without a film carrier H01L 23/49572, flexible insulating substrates H01L 23/4985, H01L 23/5387)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thin flexible metallic tape with or without a film carrier	H01L 23/49572
Flexible insulating substrates	H01L 23/4985, H01L 23/5387

H01L 24/71

{Means for bonding not being attached to, or not being formed on, the surface to be connected (holders for supporting the complete device in operation H01L 23/32)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

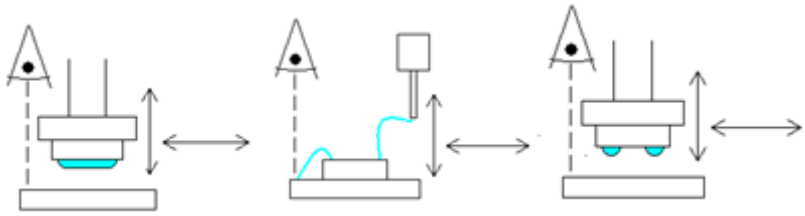
Holders for supporting the complete device in operation H01L 23/32	H01L 23/32

H01L 24/80

{Methods for connecting semiconductor or other solid state bodies using means for bonding being attached to, or being formed on, the surface to be connected}

Definition statement

This place covers:

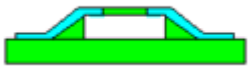


H01L 24/82

{by forming build-up interconnects at chip-level, e.g. for high density interconnects [HDI] (interconnection structure between a plurality of semiconductor chips H01L 23/5389)}

Definition statement

This place covers:



References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Interconnection structure between a plurality of semiconductor chips	H01L 23/5389

H01L 24/85

{using a wire connector (wire bonding in general B23K 20/004)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

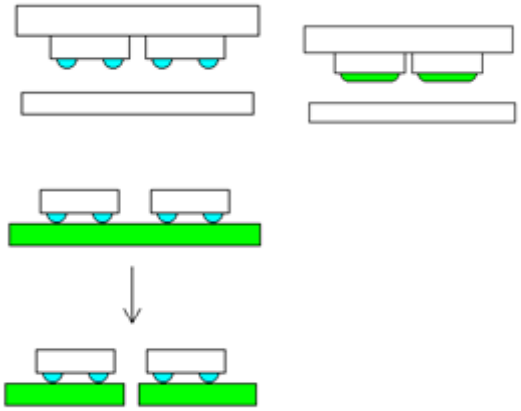
Wire bonding in general	B23K 20/004

H01L 24/93

{Batch processes}

Definition statement

This place covers:



H01L 24/96

{the devices being encapsulated in a common layer, e.g. neo-wafer or pseudo-wafer, said common layer being separable into individual assemblies after connecting}

Definition statement

This place covers:

H01L 25/00

Assemblies consisting of a plurality of semiconductor or other solid state devices (devices consisting of a plurality of solid-state components formed in or on a common substrate H10D 89/00; photovoltaic modules or arrays of photovoltaic cells H10F 19/00)

References

Limiting references

This place does not cover:

Panels or arrays of photo electrochemical cells	H01G 9/2068
Devices consisting of a plurality of solid state components formed in or on a common substrate	H10D 89/00
Photovoltaic modules or arrays of photovoltaic cells	H10F 19/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Assemblies of semiconductor devices on lead-frames	H01L 23/49575
Leads on insulating substrates (chip carriers)	H01L 23/498
Interconnection structures for a plurality of bare semiconductor chips provided on or in an insulating substrate	H01L 23/538
Arrangements for connecting or disconnecting semiconductor or solid-state bodies; methods related thereto	H01L 24/00
Couplings of light guides with optoelectronic elements	G02B 6/42
Static Stores	G11C
Generators using solar cells or photovoltaic modules	H02S
Details of complete circuit assemblies provided for in another subclass, e.g. details of television receivers, see the relevant subclass, e.g. H04N	H04N
Details of assemblies of electrical components in general	H05K
Tandem solar cells, meaning monolithically integrated solar cells with different wavelengths sensibilities deposited on one another by coating processes	H10F 10/142, H10F 10/161, H10F 10/172, H10F 10/19
Integrated photodetecting devices on a substrate	H10F 39/10
Light sensitive devices structurally associated with, e.g. formed in or on a common substrate with, one or more electric light sources, and electrically or optically coupled thereto (e.g. opto-couplers)	H10F 55/00
Organic light emitting devices [OLEDs]	H10K 50/00
Integration of organic light emitting devices (OLEDs), e.g. OLED displays	H10K 59/00

Special rules of classification

The classification of additional information is mandatory in this main group.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Assembly of a Device	The "assembly" of a device is the building up of the device from its component constructional units and includes the provision of fillings in containers.

H01L 25/03

all the devices being of a type provided for in a single subclass of subclasses H10B, H10F, H10H, H10K or H10N, e.g. assemblies of rectifier diodes

Definition statement

This place covers:

- "package in package" devices
- assemblies of rectifier diodes

H01L 25/042

{the devices being arranged next to each other (solar cells H10F 19/00)}

Definition statement

This place covers:

Arrays of photodetectors disposed next to one another on a common substrate.

References

Limiting references

This place does not cover:

Assemblies of thin film solar cells	H10F 19/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multicolour imagers having a stacked structure	H10F 39/1825
Multispectral infrared imagers, having a stacked structure	H10F 39/1847

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Disposed	means that photodetectors already manufactured are individually placed on the common substrate, as opposed to "integrated" which means the devices are all formed on or in said substrate during the same process

H01L 25/043

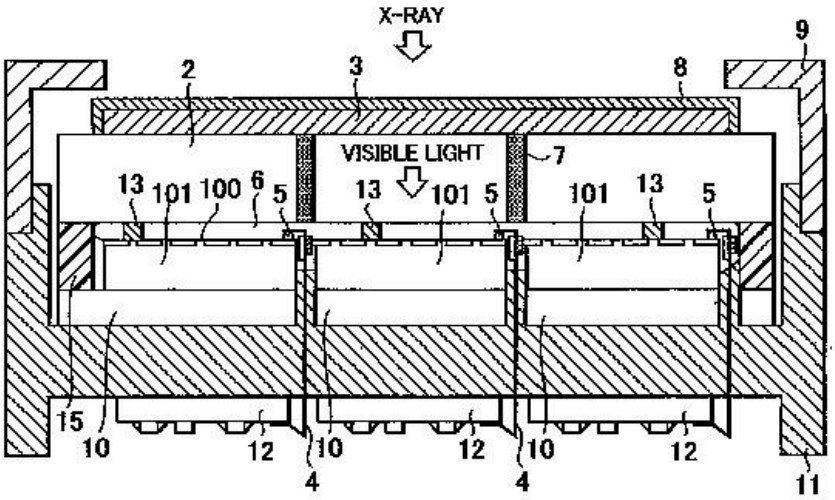
{Stacked arrangements of devices}

Definition statement

This place covers:

Photodetectors mechanically stacked on one another:

FIG. 8



EP 1 287 403 A2

H01L 25/075

the devices being of a type provided for in group H10H 20/00

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Light sources using semiconductor devices as light-generating elements, e.g. using light-emitting diodes [LED] or lasers	F21K 9/00

H01L 25/16

the devices being of types provided for in two or more different subclasses of H10B, H10D, H10F, H10H, H10K or H10N, e.g. forming hybrid circuits

Definition statement

This place covers:

Hybrid modules of active and passive components

References

Limiting references

This place does not cover:

Interconnections for hybrid circuits	H01L 23/5389

H01L 25/18

the devices being of the types provided for in two or more different main groups of the same subclass of H10B, H10D, H10F, H10H, H10K or H10N

Definition statement

This place covers:

Arrangement of memory and logic chips

Arrangement of diode and IGBT

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate and controlled by radiation	H10F 39/10

H01L 25/50

{Multistep manufacturing processes of assemblies consisting of devices, the devices being individual devices of subclass H10D or integrated devices of class H10 (H01L 21/50 takes precedence)}

Definition statement

This place covers:

Processes to fabricate devices formed of an assembly of a multiplicity of components on a host substrate.

References

Limiting references

This place does not cover:

Assembly of semiconductor devices using processes or apparatus not provided for in a single one of the subgroups H01L 21/18 - H01L 21/326	H01L 21/50

H01L 2221/68372

used to support a device or wafer when forming electrical connections thereto

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacturing methods of bonding areas for connecting semiconductor or solid-state bodies	H01L 24/03
Manufacturing methods of bump connectors for connecting semiconductor or solid-state bodies	H01L 24/11
Manufacturing methods of layer connectors for connecting semiconductor or solid-state bodies	H01L 24/27

H01L 2223/6644

Packaging aspects of high-frequency amplifiers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Amplifiers per se	H03F

H01L 2223/6661

for passive devices

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Passive two-terminal components without a potential-jump or surface barrier for integrated circuits	H10D 1/00

H01L 2223/6672

for integrated passive components, e.g. semiconductor device with passive components only

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Devices consisting of a plurality of semiconductor or other solid-state components comprising only passive thin-film or thick film elements formed on a common insulating substrate	H10D 84/201, H10D 86/80

H01L 2223/6677

for antenna, e.g. antenna included within housing of semiconductor device

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Antennas per se	H01Q

H01L 2224/03422

by dipping, e.g. in a solder bath

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Hot-dipping or immersion processes for applying the coating material in the molten state without affecting the shape	C23C 2/00

H01L 2224/03424

Immersion coating, e.g. in a solder bath

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Hot-dipping or immersion processes for applying the coating material in the molten state without affecting the shape	C23C 2/00

H01L 2224/036

by patterning a pre-deposited material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of semiconductor parts, e.g. containers, prior to assembly of the devices using processes not provided for in a single one of the subgroups H01L 21/18 - H01L 21/326	H01L 21/48

H01L 2224/0383

Reworking, e.g. shaping

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thermal post-treatment of the bonding area, e.g. reflowing	H01L 2224/03849

H01L 2224/05187

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Material with principal constituent being glasses, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05188

H01L 2224/05287

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05288

H01L 2224/05387

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05388

H01L 2224/05487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05488

H01L 2224/05687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05688

H01L 2224/05787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05788

H01L 2224/05887

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05888

H01L 2224/05987

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/05988

H01L 2224/0912

Layout

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Layout of bonding areas prior to the connecting process	H01L 2224/0612

H01L 2224/11422

by dipping, e.g. in a solder bath

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Hot-dipping or immersion processes for applying the coating material in the molten state without affecting the shape	C23C 2/00

H01L 2224/11424

Immersion coating, e.g. in a solder bath

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Hot-dipping or immersion processes for applying the coating material in the molten state without affecting the shape	C23C 2/00

H01L 2224/116

by patterning a pre-deposited material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of semiconductor parts, e.g. containers, prior to assembly of the devices using processes not provided for in a single one of the subgroups H01L 21/18 - H01L 21/326	H01L 21/48

H01L 2224/1183

Reworking, e.g. shaping

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thermal post-treatment of the bump connector, e.g. reflowing	H01L 2224/11849

H01L 2224/13187

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13188

H01L 2224/13287

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13288

H01L 2224/13387

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13388

H01L 2224/13487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13488

H01L 2224/13687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13688

H01L 2224/13787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13788

H01L 2224/13887

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13888

H01L 2224/13987

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/13988

H01L 2224/1712

Layout

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Layout of bump connectors prior to the connecting process	H01L 2224/1412

H01L 2224/27422

by dipping, e.g. in a solder bath

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Hot-dipping or immersion processes for applying the coating material in the molten state without affecting the shape	C23C 2/00

H01L 2224/27424

Immersion coating, e.g. in a solder bath

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Hot-dipping or immersion processes for applying the coating material in the molten state without affecting the shape	C23C 2/00

H01L 2224/276

by patterning a pre-deposited material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacture or treatment of semiconductor parts, e.g. containers, prior to assembly of the devices using processes not provided for in a single one of the subgroups H01L 21/18 - H01L 21/326	H01L 21/48

H01L 2224/2783

Reworking, e.g. shaping

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Thermal post-treatment of the layer connector, e.g. reflowing	H01L 2224/27849

H01L 2224/29021

the layer connector being disposed in a recess of the surface

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Layer connector being at least partially embedded in the surface	H01L 2224/29022

H01L 2224/29187

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29188

H01L 2224/29287

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29288

H01L 2224/29387

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29388

H01L 2224/29487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29488

H01L 2224/29687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29688

H01L 2224/29787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29788

H01L 2224/29887

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29888

H01L 2224/29987

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/29988

H01L 2224/3312

Layout

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Layout of layer connectors prior to the connecting process	H01L 2224/3012

H01L 2224/37187

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37188

H01L 2224/37287

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37288

H01L 2224/37387

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37388

H01L 2224/37487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37488

H01L 2224/37687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37688

H01L 2224/37787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37788

H01L 2224/37887

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37888

H01L 2224/37987

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/37988

H01L 2224/45187

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45188

H01L 2224/45287

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45288

H01L 2224/45387

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45388

H01L 2224/45487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45488

H01L 2224/45687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45688

H01L 2224/45787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45788

H01L 2224/45887

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45888

H01L 2224/45987

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/45988

H01L 2224/48687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/48688

H01L 2224/48787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/48788

H01L 2224/48887

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/48888

H01L 2224/80052

Detaching bonding areas, e.g. after testing

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Unsoldering; Removal of melted solder or other residues	B23K 1/018

H01L 2224/80237

using an electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2224/80379

Material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Material of the bonding area prior to the connecting process	H01L 2224/05099, H01L 2224/05599

H01L 2224/80487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics e.g. amorphous oxides, nitrides or fluorides	H01L 2224/80488

H01L 2224/80587

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/80588

H01L 2224/80687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/80688

H01L 2224/80787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/80788

H01L 2224/80901

Pressing a bonding area against another bonding area by means of a further bonding area or connector

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Detachable connecting means consisting of mechanical auxiliary parts connecting the device, e.g. pressure contacts using springs or clips	H01L 2224/72

H01L 2224/81052

Detaching bump connectors, e.g. after testing

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Unsoldering; Removal of melted solder or other residues	B23K 1/018

H01L 2224/81237

using an electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2224/81379

Material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Material of the bump connector prior to the connecting process	H01L 2224/13099, H01L 2224/13599

H01L 2224/81487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/81488

H01L 2224/81587

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/81588

H01L 2224/81687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/81688

H01L 2224/81787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/81788

H01L 2224/81901

Pressing the bump connector against the bonding areas by means of another connector

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Detachable connecting means consisting of mechanical auxiliary parts connecting the device, e.g. pressure contacts using springs or clips	H01L 2224/72

H01L 2224/82237

using electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2224/83052

Detaching layer connectors, e.g. after testing

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Unsoldering; Removal of melted solder or other residues	B23K 1/018

H01L 2224/83237

using an electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2224/83379

Material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Core member material of the layer connector prior to the connecting process	H01L 2224/29099
Coating material of the layer connector prior to the connecting process	H01L 2224/29599

H01L 2224/83487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/83488

H01L 2224/83587

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/83588

H01L 2224/83687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/83688

H01L 2224/83787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/83788

H01L 2224/84237

using an electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2224/84487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/84488

H01L 2224/84587

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/84588

H01L 2224/84687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/84688

H01L 2224/84787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/84788

H01L 2224/85237

using electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2224/85487

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/85488

H01L 2224/85587

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/85588

H01L 2224/85687

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/85688

H01L 2224/85787

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Glass ceramics, e.g. amorphous oxides, nitrides or fluorides	H01L 2224/85788

H01L 2224/86237

using electron beam

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Electron-beam welding or cutting	B23K 15/00

H01L 2225/06541

Conductive via connections through the device, e.g. vertical interconnects, through silicon via [TSV]

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Manufacturing of interconnections to be used for carrying current between separate components with a device formed through a semiconductor substrate	H01L 21/76898

H01L 2225/06593

Mounting aids permanently on device; arrangements for alignment

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Apparatus for supporting or gripping semiconductor using temporarily an auxiliary support	H01L 21/6835

H01L 2225/06596

Structural arrangements for testing

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Testing or measuring during manufacture or treatment	H01L 22/00
Testing electrical properties or locating electrical faults	G01R 31/00

H01L 2225/107

Indirect electrical connections, e.g. via an interposer, a flexible substrate, using TAB

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Printed circuits	H05K 1/00

H01L 2924/06

Polymers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Organic macromolecular compounds	C08
Adhesives; Non-mechanical aspects of adhesive processes in general	C09J

H01L 2924/16174

Ceramics, e.g. crystalline carbides, nitrides or oxides

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

The bump connector connecting between a semiconductor or solid-state body and an item not being a semiconductor or solid-state body, the item being metallic	H01L 2224/16175