H01L

SEMICONDUCTOR DEVICES; ELECTRIC SOLID STATE DEVICES NOT OTHERWISE PROVIDED FOR (use of semiconductor devices for measuring G01; resistors in general H01C; magnets, inductors, transformers H01F; capacitors in general H01G; electrolytic devices H01G 9/00; batteries, accumulators H01M; waveguides, resonators, or lines of the waveguide type H01P; line connectors, current collectors H01R; stimulated-emission devices H01S; electromechanical resonators H03H; loudspeakers, microphones, gramophone pick-ups or like acoustic electromechanical transducers H04R; electric light sources in general H05B; printed circuits, hybrid circuits, casings or constructional details of electrical apparatus, manufacture of assemblages of electrical components H05K; use of semiconductor devices in circuits having a particular application, see the subclass for the application)

Definition statement

This place covers:

in general
  • discrete and integrated semiconductor devices and
  • other electric solid state devices (as far as not provided for in another subclass) and
  • details thereof.

This includes the following kind of devices:
  • integrated circuit devices, e.g. CMOS integrated devices, DRAM, EPROM, CCD;
  • semiconductor devices (e.g. field-effect, bipolar) adapted for rectifying, amplifying, oscillating or switching, e.g. diodes, transistors, thyristors;
  • semiconductor devices sensitive to radiation, e.g. photo diodes, photo transistors, solar cells;
  • incoherent light emitting diodes, e.g. LED;
  • solid state devices using organic materials as the active part or using a combination of organic materials with other materials as the active part, e.g. organic LED or polymer LED;
  • electric solid state devices using thermoelectric, superconductive, piezo-electric, electrostrictive, magnetostrictive, galvano-magnetic or bulk negative resistance effects, e.g. thermo couples, Peltier elements, Josephson elements, piezo elements;
  • photo-resistors, magnetic field dependent resistors, field effect resistors;
  • capacitors with potential-jump barrier, resistors with potential-jump barrier or surface barrier;
  • thin-film or thick-film circuits;
  • processes and apparatus adapted for the manufacture or treatment of such devices, except where such processes relate to single step processes for which provision exists elsewhere.

Relationships with other classification places

Microstructural devices or systems are classified in subclass B81B, and the processes and apparatus specially adapted for the manufacture or treatment thereof are classified in subclass B81C. So, by way of example, microelectro-mechanical devices (MEMS), containing microelectronic and mechanical components, are classified in group B81B 7/02, and their manufacture, treatment or assembling in the relevant groups of B81C. Microstructural devices or systems working purely electrically or electronically, or related processes or apparatus for the manufacture or treatment thereof are however not covered by B81B or B81C and are classified in section H, for example in the groups of the current subclass H01L.

Microstructural devices or systems being of other than purely electrical or electronically type, and apparatus or processes for the manufacture or treatment thereof, which are normally classified in

1
the subclasses B81B and B81C, may be also classified in those groups of H01L providing for their structural or functional features, whenever such features are of interest per se.

Nanostructures, which are normally classified in subclass B82B, may be also classified in those groups of H01L providing for their structural or functional features, whenever such features are of interest per se.

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Category</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micromechanical Devices (MEMS)</td>
<td>B81B</td>
</tr>
<tr>
<td>Processes and apparatus specially adapted for the manufacture or</td>
<td>B81C</td>
</tr>
<tr>
<td>treatment of microstructural devices or systems</td>
<td></td>
</tr>
<tr>
<td>Measurement of Mechanical Vibrations or Ultrasonic, Sonic or Infrasonic</td>
<td>G01H</td>
</tr>
<tr>
<td>Waves</td>
<td></td>
</tr>
<tr>
<td>Measurement of Intensity, velocity, Spectral, Content, Polarization,</td>
<td>G01J</td>
</tr>
<tr>
<td>Phase or Pulse Characteristic of Infra-red, Visible or Ultra-Violet</td>
<td></td>
</tr>
<tr>
<td>Light</td>
<td></td>
</tr>
<tr>
<td>Measuring Electrical or Magnetic Variables</td>
<td>G01P</td>
</tr>
<tr>
<td>Radio Direction-Finding; Radio Navigation; Determining Distance or</td>
<td>G01S</td>
</tr>
<tr>
<td>Velocity by Use of Radio Waves; Locating or Presence-Detecting by Use</td>
<td></td>
</tr>
<tr>
<td>of the Reflection or Reradiation of Radio Waves; Analogous Arrangements</td>
<td></td>
</tr>
<tr>
<td>Using Other Waves</td>
<td></td>
</tr>
<tr>
<td>Measuring Nuclear or X-Radiation</td>
<td>G01T</td>
</tr>
<tr>
<td>Electro photography</td>
<td>G03G</td>
</tr>
<tr>
<td>Systems for Regulating Electrical or Magnetic Variables</td>
<td>G05F</td>
</tr>
<tr>
<td>Digital Computers</td>
<td>G06F</td>
</tr>
<tr>
<td>Static Stores</td>
<td>G11C</td>
</tr>
<tr>
<td>Conductive and Insulating Materials</td>
<td></td>
</tr>
<tr>
<td>Resistors in general</td>
<td>H01B</td>
</tr>
<tr>
<td>Magnets, inductors, transformers</td>
<td>H01C</td>
</tr>
<tr>
<td>Capacitors in general</td>
<td>H01G</td>
</tr>
<tr>
<td>Batteries, accumulators</td>
<td>H01M</td>
</tr>
<tr>
<td>Waveguides, resonators or lines of the waveguide type</td>
<td>H01P</td>
</tr>
<tr>
<td>Line connectors, current collectors</td>
<td>H01R</td>
</tr>
<tr>
<td>Stimulated emission devices (e.g. semiconductor laser)</td>
<td>H01S</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>H03F</td>
</tr>
<tr>
<td>Electromechanical resonators; impedance networks</td>
<td>H03H</td>
</tr>
<tr>
<td>Pictorial Communication, e.g. Television</td>
<td>H04N</td>
</tr>
<tr>
<td>Loudspeakers, microphones, gramophone pick-ups or like acoustic</td>
<td>H04R</td>
</tr>
<tr>
<td>electromechanical transducers</td>
<td></td>
</tr>
<tr>
<td>Electric light sources in general</td>
<td>H05B</td>
</tr>
<tr>
<td>Printed circuits, hybrid circuits, casings or constructional details of</td>
<td>H05K</td>
</tr>
<tr>
<td>electric apparatus, manufacture of assemblages of electrical components</td>
<td></td>
</tr>
</tbody>
</table>
**Application-oriented references**

Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

| Use of semiconductor devices for measuring | G01 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Containers merely intended for transport or storage of wafers except during manufacture or finishing devices thereon | B65D 85/30, B65D85/86 |
| Conveying systems for semiconductor wafers except during manufacture or treatment of semiconductor or electric solid state devices or components thereon | B65G 49/07 |
| Coating Material | C23C |
| Non-mechanical removal of metallic material from surface | C23F |
| Details of scanning-probe apparatus, in general | G01Q 10/00 - G01Q 90/00 |
| Electric discharge tubes or discharge lamps | H01J |
| Use of semiconductor devices in circuits having a particular application: see particular subclass for the application | |

**Special rules of classification**

In this subclass, Indexing Codes are mainly attributed with a view to allow retrieval of documents comprising a combination of technical characteristics, some of them being unimportant per se, and, hence, identified as additional information rather than invention information.

In this subclass, both the process and apparatus for the manufacture or treatment of a device and the device itself are classified, whenever both of these are described sufficiently to be of interest.

**Glossary of terms**

In this place, the following terms or expressions are used with the meaning indicated:

| Assembly of a Device | The "assembly" of a device is the building up of the device from its component constructional units and includes the provision of fillings in containers. |
| Complete Device | A "complete device" is a device in its fully assembled state which may or may not require further treatment, e.g. electro-forming, before it is ready for use but which does not require the addition of further structural units. |
| Component | A "component" is one electric circuit element of a plurality of elements formed in or on a common substrate. |
| Container | A "container" is an enclosure forming part of the complete device and is essentially a solid construction in which the body of the device is placed, or which is formed around the body without forming an intimate layer thereon. |
| Device | The term "device" refers to an electric circuit element |
### Electrodes

"Electrodes" are regions in or on the body of the device (other than the solid state body itself), which exert an influence on the solid state body electrically, whether or not an external electrical connection is made thereto. Electrodes are often referred to as "contacts" in the literature. An electrode may include several portions and the term includes metallic regions which exert influence on the solid state body through an insulating region, (e.g. capacitive coupling) and inductive coupling arrangements to the body. The dielectric region in a capacitive arrangement is regarded as part of the electrode. In arrangements including several portions only those portions which exert an influence on the solid state body by virtue of their shape, size or disposition or the material of which they are formed are considered to be part of the electrode. The other portions are considered to be "arrangements for conducting electric current to or from the solid state body" or "interconnections between solid state components formed in or on a common substrate", e.g. interconnections.

### Encapsulation

An "encapsulation" is an enclosure which consists of one or more layers formed on the body and in intimate contact therewith.

### Integrated Circuit

An "integrated circuit" is a device where all components, e.g. diodes, resistors, are built up on a common substrate and form the device including interconnections between the components.

### Integration Process

Processes for the manufacture of at least two different components where the process is especially adapted to their integration, e.g. to take advantage of the integration or to reduce their manufacturing cost. Example: in a CMOS process, the same ion implant dopes the p-MOS gate and the n-MOS source and drain. Consequently, a process for the manufacture of a component per se is not considered as an integration process, even though that component will be part of an integrated circuit.

### Interconnection

Refers to the arrangement of conductive and insulating regions aimed at electrically connecting the respective electrodes of at least two device units, e.g. two transistors.

### Parts

The term "parts" includes all structural units which are included in a complete "device".

### Solid State Body

The expression "solid state body" refers to the body of material within which, or at the surface of which, the physical effects characteristic of the device occur. In thermoelectric devices it includes all materials in the current path.

### Wafer

A "wafer" means a slice of semiconductor or crystalline substrate material, which can be modified by impurity diffusion (doping), ion implantation or epitaxy, and whose active surface can be processed into arrays of discrete devices or integrated circuits.

### Synonyms and Keywords

In patent documents, the following words/expressions are often used with the meaning indicated:

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>package</td>
<td>container, encapsulation</td>
</tr>
</tbody>
</table>
H01L 21/00

Processes or apparatus adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof (testing or measuring during manufacture or treatment, or reliability measurements H01L 22/00; multistep manufacturing processes for passive two-terminal components without a potential-jump or surface barrier for integrated circuits H01L 28/00; processes or apparatus peculiar to the manufacture or treatment of devices provided for in groups H01L 31/00 - H01L 51/00 or of parts thereof, see these groups; single-step processes covered by other subclasses, see the relevant subclasses, e.g. C23C, C30B; photomechanical production of textured or patterned surfaces, materials or originals therefor, apparatus specially adapted therefor, in general G03F)

Definition statement

This place covers:
Processes and apparatus that are specially adapted for the manufacturing of semiconductor or solid state devices belonging to the type:
- Integrated circuit devices, e.g. CMOS integrated devices, DRAM, EPROM, CCD;
- Semiconductor devices (e.g. field-effect, bipolar) adapted for rectifying, amplifying, oscillating or switching, e.g. diodes, transistors, thyristors;

This main group includes:
- Manufacture or treatment of the above semiconductor devices or of parts thereof
- Manufacture or treatment of solid state devices other than semiconductor devices, or of parts thereof
- Apparatus specially adapted for handling semiconductor or electric solid state devices during manufacture or treatment thereof; Apparatus specially adapted for handling wafers during manufacture or treatment of semiconductor or electric solid state devices or components
- Manufacture or treatment of devices consisting of a plurality of solid state components formed in or on a common substrate or of parts thereof; manufacture of integrated circuit devices or of parts thereof

References

Limiting references

This place does not cover:

| Processes or apparatus specially adapted for the manufacture or treatment of devices provided for in groups H01L 31/00 - H01L 51/00 or of parts thereof, see these groups | H01L 31/00 - H01L 51/00 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

<p>| Processes for applying liquids or other fluent materials | B05D 1/00 |
| Liquid cleaning (in general) | B08B 3/00 |
| Machines, Devices, or Processes for Grinding or Polishing | B24B |
| Containers, packaging elements or packages specially adapted for particular articles or materials | B65D 85/00 |
| Shaped ceramic Products | C04B 35/00 |</p>
<table>
<thead>
<tr>
<th>Description</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polishing compositions</td>
<td>C09G 1/00</td>
</tr>
<tr>
<td>Cleaning Compositions</td>
<td>C11D</td>
</tr>
<tr>
<td>Coating by vacuum evaporation, by sputtering or by ion implantation of the coating forming material</td>
<td>C23C 14/00</td>
</tr>
<tr>
<td>Chemical coating by decomposition of gaseous compounds, without leaving reaction products of surface material in the coating (CVD)</td>
<td>C23C 16/00</td>
</tr>
<tr>
<td>Chemical coating by decomposition of either liquid compounds or solutions of the coating forming compounds, without leaving reaction products of surface material in the coating</td>
<td>C23C 18/00</td>
</tr>
<tr>
<td>Etching metallic material by chemical means</td>
<td>C23F 1/00</td>
</tr>
<tr>
<td>Processes for the Electrolytic or Electrophoretic Production of Coatings</td>
<td>C25D</td>
</tr>
<tr>
<td>Single Crystal Growth; Epitaxy</td>
<td>C30B</td>
</tr>
<tr>
<td>Testing individual semiconductor devices</td>
<td>G01R 31/00</td>
</tr>
<tr>
<td>Preparation of originals for the photomechanical production of textured or patterned surfaces</td>
<td>G03F 1/00</td>
</tr>
<tr>
<td>Photolithographic, production of textured or patterned surfaces</td>
<td>G03F 7/00</td>
</tr>
<tr>
<td>Registration or positioning of originals, masks, frames, photographic sheets or textured or patterned surfaces</td>
<td>G03F 9/00</td>
</tr>
<tr>
<td>Discharge tubes with provision for introducing objects or material to be exposed to the discharge (plasma etching; ion implantation)</td>
<td>H01J 37/00</td>
</tr>
<tr>
<td>Apparatus or processes specially adapted for manufacturing or adjusting assemblages of electric components</td>
<td>H05K 13/00</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Single mono-steps for which a provision exists elsewhere in ECLA need not to be classified in H01L 21/00, except if they are specific to the fabrication of semiconductor devices as defined under H01L 21/00. E.g., apparatuses which are not specific to the fabrication of these devices, e.g. apparatuses for depositing layers, are classified in C23C or C30B.

Multi-aspect classification is used for subject matter characterized by several aspects, for example, a process and its particular use. Single steps forming part of a multi step process should also be classified when they present a special interest or particular features.

Direct pre-treatment or direct post-treatment of a specific step is classified under the specific step if no other place exists in H01L 21/00. Example: annealing after layer coating is classified together with the coating. Exception: cleaning, see H01L 21/02041.

In H01L 21/00, poly-silicon is generally considered as a conductive material for classification purposes, except for its deposition (H01L 21/02365) where it is considered as semiconducting.

Polishing or chemical-mechanical polishing are not distinguished for classification.

Machines and apparatuses for which a provision exists somewhere else in CPC are not classified in H01L 21/00. For example apparatus for deposition of materials are classified in C23C or C30B.

Machines and apparatuses for which no particular provision exists in CPC are classified in H01L 21/67 and subgroups. See also the notes under H01L 21/67.

Processes mainly consisting of features of the use of the elements of the apparatus and which are necessary to operate said apparatus (like for example rotating the turntable of a polisher, evacuating the chamber of a plasma apparatus etc...) need not to be classified in H01L 21/00.
Subject matter relating to processes and apparatus which are clearly suitable for manufacture or treatment of devices whose bodies comprise elements of the fourth group of the Periodic System (silicon, germanium), and where the material used is not explicitly specified, is classified in the subgroups relating to semiconductors of the fourth group of the Periodic System (silicon, germanium).

For multistep processes, a junction between two regions of the same material but in a different crystalline state, e.g. amorphous silicon or polysilicon emitters on single crystalline silicon, is not considered as a heterojunction.

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry Process</td>
<td>refers to processes wherein only gases or vapours are provided on the surface of a substrate, e.g. a wafer, irrespective of the physical state of the reaction products, gaseous, liquid or solid.</td>
</tr>
<tr>
<td>Wet Process</td>
<td>refers to processes wherein only liquids are provided at the surface of a wafer, including the condensation on the surface of a wafer of gaseous components.</td>
</tr>
<tr>
<td>Pre-, post-treatment</td>
<td>direct, for example in situ, treatment, preceding or following a main technological step, aimed at improving said main technological step or its result. Not considered as a technological step per se. Examples: - annealing or crystallisation after deposition of insulating layers, - cleaning before or after a technological step, - modifying an insulating layer just after its formation, e.g. implantation after deposition</td>
</tr>
<tr>
<td>After treatment</td>
<td>Subsequent main technological step. Examples: - patterning or polishing of a layer after deposition- modifying an insulating layer after a step which is not the formation of the insulating layer</td>
</tr>
</tbody>
</table>

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVD</td>
<td>Chemical vapour deposition</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma enhanced CVD</td>
</tr>
<tr>
<td>LPCVD</td>
<td>Low pressure CVD</td>
</tr>
<tr>
<td>PVD</td>
<td>Physical Vapour Deposition</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic layer deposition</td>
</tr>
<tr>
<td>ALE</td>
<td>Atomic layer epitaxy</td>
</tr>
<tr>
<td>CMP</td>
<td>Chemical mechanical polishing</td>
</tr>
<tr>
<td>ECMP</td>
<td>Electrochemical CMP</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on Insulator</td>
</tr>
<tr>
<td>BESOI</td>
<td>Bonded and Etched-Back Silicon-On-Insulator</td>
</tr>
<tr>
<td>SOS</td>
<td>Silicon on Sapphire</td>
</tr>
<tr>
<td>HSG</td>
<td>Hemispherical grain</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive ion etching</td>
</tr>
<tr>
<td>BSG</td>
<td>boron silicate glass</td>
</tr>
<tr>
<td>PSG</td>
<td>phosphorous silicate glass</td>
</tr>
<tr>
<td>BPSG</td>
<td>boron phosphorous silicate glass</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>USG</td>
<td>Undoped silicate glass</td>
</tr>
<tr>
<td>FSG</td>
<td>Fluorine silicate glass</td>
</tr>
<tr>
<td>PZT</td>
<td>Lead zirconate titanate</td>
</tr>
<tr>
<td>BST</td>
<td>Barium strontium titanate</td>
</tr>
<tr>
<td>HSQ</td>
<td>Hydrogen silsesquioxane</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular beam epitaxy</td>
</tr>
<tr>
<td>ELO</td>
<td>Epitaxial lateral overgrowth</td>
</tr>
<tr>
<td>MIS</td>
<td>Metal-insulator-semiconductor</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary MOS</td>
</tr>
<tr>
<td>DMOS</td>
<td>Double diffused MOS</td>
</tr>
<tr>
<td>VDMOS</td>
<td>Vertical DMOS</td>
</tr>
<tr>
<td>LDMOS</td>
<td>Lateral DMOS</td>
</tr>
<tr>
<td>IMPATT</td>
<td>Impact Ionization Avalanche Transit Time</td>
</tr>
<tr>
<td>TRAPATT</td>
<td>Trapped Plasma Avalanche Triggered Transistor</td>
</tr>
<tr>
<td>SiTh</td>
<td>Static induction thyristor</td>
</tr>
<tr>
<td>FCTh</td>
<td>Field controlled thyristor</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>HET</td>
<td>Hot electron transistor</td>
</tr>
<tr>
<td>SET</td>
<td>Single electron transistor</td>
</tr>
<tr>
<td>SIT</td>
<td>Static Induction Transistor</td>
</tr>
<tr>
<td>MBT</td>
<td>Metal base transistor</td>
</tr>
<tr>
<td>RHET</td>
<td>Resonant tunnelling hot electron transistor</td>
</tr>
<tr>
<td>RTT</td>
<td>Resonant tunnelling transistor</td>
</tr>
<tr>
<td>BBT</td>
<td>Bulk barrier transistor</td>
</tr>
<tr>
<td>PBT</td>
<td>Permeable Base Transistor</td>
</tr>
<tr>
<td>HFET</td>
<td>Heterostructure FET</td>
</tr>
<tr>
<td>HIGFET</td>
<td>Heterostructure Insulated Gate FET</td>
</tr>
<tr>
<td>SISFET</td>
<td>Semiconductor-insulator-semiconductor FET</td>
</tr>
<tr>
<td>HJFET</td>
<td>Hetero Junction FET</td>
</tr>
<tr>
<td>MISFET</td>
<td>Metal-insulator-semiconductor FET</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction FET</td>
</tr>
<tr>
<td>FinFET</td>
<td>FET with Fin-type channel</td>
</tr>
<tr>
<td>MuGFET</td>
<td>Multi Gate FET</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>PDBT</td>
<td>Planar doped barrier transistor</td>
</tr>
<tr>
<td>CHINT</td>
<td>Charge injection transistor</td>
</tr>
<tr>
<td>LDD</td>
<td>lightly doped drain</td>
</tr>
<tr>
<td>DDD</td>
<td>Double diffused drain</td>
</tr>
<tr>
<td>EPIC</td>
<td>Epitaxial Passivated Integrated Circuit</td>
</tr>
</tbody>
</table>
LOCOS | Local Oxidation of Silicon
---|---
SWAMI | Side Wall Masked Isolation
SILO | Sealed Isolation LOCOS
SIMOX | Separation by Implantation of Oxygen
FIPOS | Full Isolation by porous oxidized silicon
ELTRAN | Epitaxial Layer Transfer
SEG | Selective Epitaxial Growth
DRAM | Dynamic RAM
CCD | Charge Coupled Device

**H01L 21/02002**

**{Preparing wafers}**

**Definition statement**

*This place covers:*

Multi-step processes for the manufacture of semiconductor wafers for the fabrication of semiconductor devices as defined under H01L 21/00, prior to the fabrication of any device or part of device, i.e. between the sawing of ingots (covered by B28D) and the cleaning of the wafers (H01L 21/02041), e.g. grinding followed by lapping and polishing.

Covers the preparation of bulk semiconductor wafers (e.g. bulk silicon wafers).

**Relationships with other classification places**

See also H01L 21/8258, which has been used for classifying the fabrication of substrates containing parts of Group-IV and Group AIII-BV semiconductors.

See also C30B 33/00.

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Thermal smoothening</th>
<th>H01L 21/324</th>
</tr>
</thead>
<tbody>
<tr>
<td>The fabrication of inhomogeneous wafers, like SOI</td>
<td>H01L 21/76</td>
</tr>
<tr>
<td>Marking of wafers</td>
<td>H01L 23/544</td>
</tr>
<tr>
<td>The fabrication of wafers comprising portions of different materials</td>
<td>H01L 27/00</td>
</tr>
<tr>
<td>Forming flats</td>
<td>C30B 33/00</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Multiple classification on different aspects is made, provided the invention is sufficiently disclosed on these different aspects.

Wafers per se are classified in H01L 29/06
**H01L 21/02005**  
{Preparing bulk and homogeneous wafers}

**Definition statement**

*This place covers:*

Bulk, homogeneous wafers:
- Group IV, Si, Ge,
- Group III-V, GaAs, InP,

**H01L 21/0201**  
{Specific process step}

**Definition statement**

*This place covers:*

Multistep process for preparing wafers where the accent is put on a specific step.

**H01L 21/02013**  
{Grinding, lapping}

**Definition statement**

*This place covers:*

Multistep process for preparing wafers where the accent is put on the grinding or lapping, e.g. multiple grinding steps.

**H01L 21/02016**  
{Backside treatment}

**Definition statement**

*This place covers:*

Multistep process for preparing wafers where the accent is put on the backside treatment.

Includes backside treatment for recognition purposes

**H01L 21/02019**  
{Chemical etching}

**Definition statement**

*This place covers:*

Multistep process for preparing wafers where the accent is put on the chemical etching step or steps.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Chemical or electrical treatment, e.g. electrolytic etching | H01L 21/306 |
H01L 21/02021
{Edge treatment, chamfering}

**Definition statement**

This place covers:
Multistep process for preparing wafers where the accent is put on the edge treatment, e.g. chamfering.

**References**

*Limiting references*

This place does not cover:

<table>
<thead>
<tr>
<th>Does not cover the processing of edges of Smart Cut donor substrates, classified in reclaiming/reprocessing</th>
</tr>
</thead>
</table>

H01L 21/02024
{Mirror polishing}

**Definition statement**

This place covers:
Multistep process for preparing wafers where the accent is put on the mirror polishing.

**Special rules of classification**

In case a mechanical mirror polishing is completed by a chemical flattening step, e.g. a gaseous flattening step, the latter is classified independently.

H01L 21/02027
{Setting crystal orientation}

**Definition statement**

This place covers:
Multistep processes for preparing wafers having a specific orientation planes as useful plane, or a specific orientation plane in a plane parallel to the surface.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Single-crystal growth by pulling from a melt characterised by the seed, e.g. its crystallographic orientation</th>
</tr>
</thead>
</table>

C30B 15/36
H01L 21/0203

{Making porous regions on the surface}

Definition statement

This place covers: Making a surface of the wafer porous. Includes formation of internal porous regions.

References

Limiting references

This place does not cover:

| Localized formation (using e.g. masks) of porous regions | H01L 21/306, H01L 21/3063 |

H01L 21/02032

{by reclaiming or re-processing}

Definition statement

This place covers: Multistep processes for reclaiming or re-processing, a wafer containing more than a cleaning process. Also contains the re-processing of Smart-Cut donor substrates.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Specific cleaning for reclaiming or reprocessing | H01L 21/02079 |

H01L 21/02035

{Shaping}

Definition statement

This place covers: Processes adapted to change the shape of a wafer, either in the surface plane (e.g. square, rectangular wafers), or in cross section (bone cross section).

References

Limiting references

This place does not cover:

| The provision of flats, classified with the fabrication of the ingot | C30B |
**H01L 21/02041**

**{Cleaning}**

**Definition statement**

*This place covers:*

Cleaning of wafers before or during manufacturing;

Cleaning is the removal of entities which were always unwanted, like particles, impurities, stringers, fences etc. Also includes the removal of edge beads or unwanted coatings on edges or backside of the wafers etc., except photoresist edge beads and photoresist on backside.

Removal of entities which have had a use or a function (sidewalls, resists etc.) is not considered to be a cleaning.

Includes the removal of natural oxide, see also the section "Special rules for classification within this group" below.

Starts with the deep cleaning carried out before first fabrication step (Piranha-RCA) up to cleaning after singulation.

**Relationships with other classification places**

Rinsing and drying are seen as a post-treatment of a wet cleaning, classified together with wet cleaning in H01L 21/02052.

**References**

**Limiting references**

*This place does not cover:*

| Does not cover the transformation of an impurity or contaminant in something else remaining on the device, e.g. passivation, classified with passivation in general | H01L 21/28247 |
| Processes for the removal of only photoresists, classified in | H01L 21/31127 |
| Removal of excess metal after silicidation, classified in | H01L 21/3213 |
| Does not cover processes for the removal of photoresists edge beads after coating | G03F 7/168, G03F 7/2028 |

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Cleaning apparatus | H01L 21/67005 |
| Cleaning by methods involving the use of tools, brushes, or analogous members, the use or presence of liquid or steam, the use of air flow or gas flow; Cleaning by electrostatic means | B08B 1/00 - B08B 7/00 |
| Detergent compositions, e.g. cleaning solutions or liquids | C11D |

**Special rules of classification**

Multiaspect classification is used in H01L 21/02041 and subgroups.

Removal of only natural oxide is also classified in H01L 21/311 if the process is of special relevance for thick oxides.
Removal of impurities, e.g. side walls after RIE, together with the photoresist is classified in H01L 21/02041, and additionally in H01L 21/311, if the resist removal method is peculiar.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RCA</td>
<td>standard clean composed of SC-1 and SC-2 at least, with piranha and HF or DHF</td>
</tr>
<tr>
<td>SC-1</td>
<td>standard clean 1: NH4OH-H2O2</td>
</tr>
<tr>
<td>SC-2</td>
<td>standard clean 2: HCl, H₂O₂</td>
</tr>
<tr>
<td>DHF</td>
<td>diluted HF</td>
</tr>
<tr>
<td>Piranha</td>
<td>H₂SO₄-peroxide</td>
</tr>
</tbody>
</table>

H01L 21/02043

{Cleaning before device manufacture, i.e. Begin-Of-Line process}

Definition statement

This place covers:

Cleaning of the wafer before any manufacturing step for the device is carried out.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 21/28247</td>
<td>Does not cover the transformation of an impurity or contaminant in something else remaining on the device, e.g. passivation</td>
</tr>
<tr>
<td>H01L 21/31127</td>
<td>Processes for the removal of only photoresist</td>
</tr>
<tr>
<td>H01L 21/3213</td>
<td>Removal of excess metal after silicidation</td>
</tr>
<tr>
<td>G03F 7/168, G03F 7/2028</td>
<td>Does not cover processes for the removal of photoresist edge beads after coating</td>
</tr>
</tbody>
</table>

H01L 21/02046

{Dry cleaning only (H01L 21/02085 takes precedence)}

Definition statement

This place covers:

All cleaning steps are dry, or when the invention is focussed on a dry cleaning aspect, the cleaning also containing more classical wet steps, like RCA.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 21/02085</td>
<td>Cleaning of diamond</td>
</tr>
</tbody>
</table>
H01L 21/02052
{Wet cleaning only (H01L 21/02085 takes precedence)}

Definition statement
This place covers:
Wet cleaning.

References
Limiting references
This place does not cover:
| Cleaning of diamond | H01L 21/02085 |

Special rules of classification
Rinsing and drying are seen as a post-treatment of a wet cleaning, classified together with wet cleaning in H01L 21/02052.

H01L 21/02054
{combining dry and wet cleaning steps (H01L 21/02085 takes precedence)}

Definition statement
This place covers:
The sequence of combining wet and dry steps.

References
Limiting references
This place does not cover:
| Cleaning of diamond | H01L 21/02085 |

Special rules of classification
Rinsing and drying are seen as a post-treatment of a wet cleaning, classified together with wet cleaning in H01L 21/02052.

H01L 21/02057
{Cleaning during device manufacture}

Definition statement
This place covers:
Cleaning when at least a fabrication step for a device (for example, first oxidation) has been carried out.
**H01L 21/0206**
{during, before or after processing of insulating layers}

**Definition statement**

This place covers:
- Cleaning after etching gate sidewalls and etching of gate oxide.
- Cleaning after formation of a resist pattern

**H01L 21/02079**
{Cleaning for reclaiming}

**Definition statement**

This place covers:
Reclaiming of semiconductor wafers as well as donor semiconductor wafers, e.g. donors in Smart-Cut®

**References**

*Limiting references*

This place does not cover:
- Etching for reclaiming

**H01L 21/02082**
{product to be cleaned}

**Definition statement**

This place covers:
Special products to be cleaned, including particular materials as well as substrates comprising particular features, like vertical features, isolated sidewalls, etc.

**H01L 21/02087**
{Cleaning of wafer edges}

**Definition statement**

This place covers:
Removal of edge beads.

**References**

*Limiting references*

This place does not cover:
- Removal of photoresist edge beads
H01L 21/0209
{Cleaning of wafer backside}

Definition statement
This place covers:
Removal of impurities or unwanted materials on backside, including parasitic coatings.

References
Limiting references
This place does not cover:
Removal of photoresist edge beads

H01L 21/02096
{only mechanical cleaning}

Definition statement
This place covers:
The group covers inventions wherein the mechanical aspect is of particular importance. Does not exclude some enhancement by chemical means.

H01L 21/02098
{only involving lasers, e.g. laser ablation}

Definition statement
This place covers:
Covers processes wherein the laser action has a primary function, with or without chemical, mechanical or electrical assistance.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:
Cleaning using a laser per se

H01L 21/02101
{only involving supercritical fluids}

Definition statement
This place covers:
Covers processes wherein the supercritical fluid has a primary function, with or without chemical, mechanical or electrical assistance.
**H01L 21/02104**

{Forming layers (deposition in general C23C; crystal growth in general C30B)}

**Definition statement**

*This place covers:*

Processes for the formation of inorganic and organic layers on a substrate, except photoresist layers (see H01L 21/027), for the fabrication of semiconductor devices as defined under H01L 21/00.

In situ pre- and post-treatments of these processes.

Processes for the formation of a multiplicity of these layers.

**Relationships with other classification places**

Processes for coating materials in general: C23C

Processes for the electrolytic coating of materials in general: C25D

Processes for the single-crystal growth of materials in general: C30B

**References**

**Limiting references**

*This place does not cover:

| Processes for forming photoresist layers, covered in | H01L 21/027 |
| Processes for forming conductive layers, covered by | H01L 21/283, H01L 21/285, H01L 21/288, H01L 21/3205 |

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Groups and their subdivisions for general aspects of formation of layers. | C23C, C25D, C30B |
| Photoresist per se | G03F 7/00 |

**Special rules of classification**

- Multiple classification is possible for different aspects, provided the invention is sufficiently disclosed on these different aspects.
- Multistep processes for fabricating laminates of insulating and conductive layers, for example insulated gates or capacitors, are classified in the corresponding application, H01L 21/28 for the insulated gates, H01L 28/40 for the capacitors etc. and do not need to be systematically classified in H01L 21/02107. However a group symbol in H01L 21/02107 may be given in case the process for forming the insulating layer is considered of general interest.

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

| ALD | atomic layer deposition |
| ALE | atomic layer epitaxy |
| MBE | molecular beam epitaxy |
PECVD | plasma enhanced chemical vapour deposition  
---|---  
PVD | physical vapour deposition  
CVD | chemical vapour deposition

**H01L 21/02107**

**{Forming insulating materials on a substrate}**

**Definition statement**

*This place covers:*

Processes for the formation of inorganic and organic insulating layers on a substrate, except photoresist layers (see H01L 21/027), for the fabrication of semiconductor devices as defined under H01L 21/00.

In situ pre- and post-treatments of these processes.

Processes for the formation of a multiplicity of these layers.

Includes fabrication of insulating
- porous layers,
- organic layers, like polyimide, cyclobutenes etc.
- Spin On Glass layers,
- silicate layers,
- inorganic layers, like SiO\(_2\), Si\(_3\)N\(_4\), Al\(_2\)O\(_3\), high-k layers, perovskites etc.

**Relationships with other classification places**

Processes for coating materials in general, including insulating materials: C23C

Processes for the electrolytic coating of materials in general: C25D

Organic or polymer layer composition: see C08G

**References**

**Limiting references**

*This place does not cover:*

| Processes for forming photoresist layers | H01L 21/027 |

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Photoresist per se | G03F 7/00 |

**Special rules of classification**

Multiple classification is made for different aspects (type of layer, formation process, treatment of layer), provided the invention is sufficiently disclosed on this aspect.

The process must be adapted or specific to the fabrication of semiconductor devices as defined under H01L 21/00. The mere mentioning of an intended use in semiconductor fabrication does not require that the document being given a group symbol in H01L 21/02107.
If the deposition is specifically adapted to a specific application, with details as to this specific application, e.g. the fabrication of a MIS or MOS electrode or interconnections, the document should additionally be classified in this specific application, for example in H01L 21/28 for the MIS or MOS aspect.

**H01L 21/02112**

{characterised by the material of the layer}

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Layers comprising sub-layers, i.e. multi-layers, are additionally classified in</th>
<th>H01L 21/022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Porous layers are additionally classified in</td>
<td>H01L 21/02203</td>
</tr>
</tbody>
</table>

**H01L 21/02115**

{the material being carbon, e.g. alpha-C, diamond or hydrogen doped carbon}

**References**

**Limiting references**

*This place does not cover:*

| Carbon Nitride. | H01L 21/02118 |

**H01L 21/02118**

{carbon based polymeric organic or inorganic material, e.g. polyimides, poly cyclobutene or PVC (polymers per se C08G, photoresist per se G03F)}

**Definition statement**

*This place covers:*

Carbon Nitride.

Carbon based polymeric material

**H01L 21/02129**

{the material being boron or phosphorus doped silicon oxides, e.g. BPSG, BSG or PSG}

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Halogen doped silicon oxides, e.g. fluorine, containing BPSG, PSG, BSG | H01L 21/02131 |
Special rules of classification
Halogen containing materials, e.g. fluorine, containing BPSG, PSG, BSG, are additionally classified in H01L 21/02131

H01L 21/02164
{the material being a silicon oxide, e.g. SiO$_2$}

Definition statement
This place covers:
The formation of silicon oxide layers is classified in this group regardless of the precursor or of the process of formation.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>In case of explicit statements on doping, on rest-groups, or on material components, see</td>
<td>H01L 21/02126</td>
</tr>
<tr>
<td>Deposition of silicon oxide from organic precursors without further statements on film composition is classified here and in</td>
<td>H01L 21/02205</td>
</tr>
</tbody>
</table>

H01L 21/02167
{the material being a silicon carbide not containing oxygen, e.g. SiC, SiC:H or silicon carbonitrides (H01L 21/02126 and H01L 21/0214 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>The formation of material containing Si, O and C, with or without additional elements</td>
<td>H01L 21/02126</td>
</tr>
<tr>
<td>The formation of material containing Si, O and N, with or without additional elements</td>
<td>H01L 21/0214</td>
</tr>
</tbody>
</table>

H01L 21/0217
{the material being a silicon nitride not containing oxygen, e.g. SixNy or SixByNz (H01L 21/02126 and H01L 21/0214 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>The formation of material containing Si, N and C, with or without additional elements</td>
<td>H01L 21/02126</td>
</tr>
<tr>
<td>The formation of material containing Si, O and N, with or without additional elements</td>
<td>H01L 21/0214</td>
</tr>
</tbody>
</table>
H01L 21/02172
{the material containing at least one metal element, e.g. metal oxides, metal nitrides, metal oxynitrides or metal carbides (materials containing silicon H01L 21/02123; metal silicates H01L 21/02142)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Material</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Materials containing silicon</td>
<td>H01L 21/02123</td>
</tr>
<tr>
<td>Metal silicates</td>
<td>H01L 21/02142</td>
</tr>
</tbody>
</table>

H01L 21/02175
{characterised by the metal (H01L 21/02197 takes precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Material</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Materials having a perovskite structure, e.g. BaTiO$_3$</td>
<td>H01L 21/02197</td>
</tr>
</tbody>
</table>

H01L 21/02197
{the material having a perovskite structure, e.g. BaTiO$_3$}

Special rules of classification
Perovskites are not classified in H01L 21/02175 and subgroups thereof.

H01L 21/022
{the layer being a laminate, i.e. composed of sublayers, e.g. stacks of alternating high-k metal oxides (adhesion layers or buffer layers H01L 21/02304, H01L 21/02362)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adhesion or buffer layers</td>
<td>H01L 21/02304, H01L 21/02362</td>
</tr>
</tbody>
</table>
H01L 21/02214
{the compound comprising silicon and oxygen}

References
Limiting references
This place does not cover:

| Mixtures of silane and oxygen | H01L 21/02211 |

H01L 21/02216
{the compound being a molecule comprising at least one silicon-oxygen bond and the compound having hydrogen or an organic group attached to the silicon or oxygen, e.g. a siloxane}

Glossary of terms
In this place, the following terms or expressions are used with the meaning indicated:

| Alkoxysilane       | Siloxane     |

H01L 21/02219
{the compound comprising silicon and nitrogen}

References
Limiting references
This place does not cover:

| Mixtures of silane and oxygen | H01L 21/02211 |

H01L 21/02227
{formation by a process other than a deposition process}

Special rules of classification
Subject matter classified in the range H01L 21/0223 - H01L 21/02249 is additionally classified in H01L 21/02252, H01L 21/02255, and H01L 21/02258 depending on the type of reaction.

H01L 21/02252
{formation by plasma treatment, e.g. plasma oxidation of the substrate (after treatment of an insulating film by plasma H01L 21/3105 and subgroups)}

References
Limiting references
This place does not cover:

| After treatment of an insulating film by plasma | H01L 21/3105 |
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Formation of an insulating film by introduction of substances into an already existing insulating film is covered by</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 21/02318</td>
</tr>
</tbody>
</table>

**H01L 21/02255**

{formation by thermal treatment (H01L 21/02252 takes precedence; after treatment of an insulating film H01L 21/3105 and subgroups)}

**References**

**Limiting references**

This place does not cover:

| Formation of insulating layers by plasma treatment, e.g. plasma oxidation of the substrate | H01L 21/02252 |
| --- |
| After treatment of an insulating film by plasma | H01L 21/3105 |

**H01L 21/02263**

{deposition from the gas or vapour phase}

**Definition statement**

This place covers:

Deposition methods in which the gas or vapour is produced by physical means, e.g. ablation from targets or heating of source materials.

**H01L 21/02266**

{deposition by physical ablation of a target, e.g. sputtering, reactive sputtering, physical vapour deposition or pulsed laser deposition}

**Definition statement**

This place covers:

Deposition methods in which the gas or vapour is produced by physical means, i.e. by ablation from targets.

**H01L 21/02269**

{deposition by thermal evaporation (H01L 21/02293 takes precedence)}

**Definition statement**

This place covers:

- Deposition methods in which the gas or vapour is produced by heating of source materials.
- Molecular beam epitaxy
References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Formation of epitaxial insulating films by a deposition method also under | H01L 21/02293 |

H01L 21/02271
{deposition by decomposition or reaction of gaseous or vapour phase compounds, i.e. chemical vapour deposition (H01L 21/02266 takes precedence)}

References

Limiting references
This place does not cover:

| Deposition by physical ablation of a target, like sputtering, reactive sputtering, physical vapour deposition, pulsed laser deposition | H01L 21/02266 |

H01L 21/0228
{deposition by cyclic CVD, e.g. ALD, ALE, pulsed CVD}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Deposition by decomposition or reaction of gaseous or vapour phase compounds in the presence of a plasma (PECVD) | H01L 21/02274 |

Special rules of classification
Subject matter relating to cyclic plasma CVD is additionally classified in H01L 21/02274

H01L 21/02288
{printing, e.g. ink-jet printing (per se B41J)}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Printing in general | B41J |
H01L 21/02293
{formation of epitaxial layers by a deposition process (epitaxial growth per se C30B)}

References
Limiting references
This place does not cover:

| Formation of non-epitaxial layers by MBE | H01L 21/02269 |
| Atomic layer epitaxy [ALE]             | H01L 21/0228 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Epitaxial growth in general | C30B |

H01L 21/02296
{characterised by the treatment performed before or after the formation of the layer (H01L 21/02227 and subgroups take precedence)}

Definition statement
This place covers:
Treatments, carried out just before or just after the formation of an insulating layer, which do not participate in the formation of the layer itself, but which are directly linked to the layer formation.

References
Limiting references
This place does not cover:

| Processes participating to the formation of a layer, for example oxidation or nitridation of silicon to form an oxide or nitride layer | H01L 21/02227 |
| After treatments like - etching - cleaning - planarising | H01L 21/311, H01L 21/02041, H01L 21/31051 |

Special rules of classification
Pre- or post treatments of general nature (pre-, post-cleaning, pre-, post conditioning etc.) without details or routine annealing steps, i.e. thermal treatment without further features as to a special atmosphere, presence of a plasma, thermally induced chemical reactions, change of phase or crystal structure, need not to be given this group symbol.
H01L 21/02299
{pre-treatment}
Definition statement
This place covers:
• Treatments to improve adhesion or change the surface termination

References
Limiting references
This place does not cover:

| Treatments by etching          | H01L 21/306, H01L 21/311 |

H01L 21/02301
{in-situ cleaning}

References
Limiting references
This place does not cover:

| Ex situ cleaning, covered by   | H01L 21/02041 |

H01L 21/02318
{post-treatment}

Definition statement
This place covers:
The definition should read "post-treatment" instead of after-treatment.
Only covers processes that are part of the layer formation.

References
Limiting references
This place does not cover:

| After- treatments performed after completion of the insulating layer | H01L 21/3105 |

Special rules of classification
Functionalization just after formation should be classified here.
In case the process would also be of interest as an after treatment (H01L 21/3105), both group symbols should be given.
H01L 21/02321
{introduction of substances into an already existing insulating layer (H01L 21/0227 and subgroups take precedence)}

Definition statement
This place covers:
Processes for introducing substances into the formed insulating layer e.g. introduction of phosphorus into silicon oxide, or introduction of nitrogen into silicon nitride to change stoichiometry.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| For the method of introduction of the dopant | H01L 21/0237, H01L 21/02343, H01L 21/02345 |

Special rules of classification
Introduction of substances into the formed insulating layer is classified both here and in H01L 21/3115

H01L 21/02326
{into a nitride layer, e.g. changing SiN to SiON}

Definition statement
This place covers:
Oxidation of silicon nitride to form silicon oxynitride.

H01L 21/02332
{into an oxide layer, e.g. changing SiO to SiON}

Definition statement
This place covers:
Nitridation of silicon oxide to form silicon oxynitride.

H01L 21/02334
{in-situ cleaning after layer formation, e.g. removing process residues}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Subject matter relating to cleaning processes for semiconductor device fabrication | H01L 21/02041 |
| Cleaning in general | B08B |
| Cleaning compositions in general | C30D |
H01L 21/02365

{Forming inorganic semiconducting materials on a substrate (for light-sensitive devices H01L 31/00)}

Definition statement

This place covers:
Processes for the formation of inorganic semiconductors on a substrate.
Processes for forming doped inorganic semiconductors.
In situ pre-and post-treatments of inorganic semiconductor materials.
Processes for the formation of multiple layers of inorganic semiconductors, comprising heterostructures.
The formed semiconductor layer may be crystalline (mono-, poly-, microcrystalline) or amorphous.

Relationships with other classification places

Attention is drawn to the groups C23C, C25D, C30B and their subdivisions for general aspects of these techniques.

References

Limiting references

This place does not cover:

Nanosized carbon materials, e.g. fullerenes, carbon nanotubes C01B 32/15
Processes for forming layers only characterized by the purely chemical aspects of the used precursors C23C, C30B

Informative references

Attention is drawn to the following places, which may be of interest for search:

Formation of inorganic semiconductors for light H01L 31/00
Processes specially adapted for the manufacture or treatment of organic semiconductor or solid state devices or of parts thereof H01L 51/0001
Fullerenes used in semiconductor or solid state devices H01L 51/0046

Special rules of classification

• Multi-aspect classification is possible in
• substrates
• intermediate layers,
• deposited layers,
• formation type,

provided the invention is sufficiently disclosed on these different aspects.
• Processes characterized by the chemical aspects of the used precursors are not classified under H01L 21/02365, but are given an Indexing Code.
• Processes for forming semiconductor layers specific to devices as defined under H01L 31/00 or H01L 33/00 may be classified, provided the invention is sufficiently disclosed on the aspect
of forming the semiconductor layers, and the material may be used for devices as defined in
H01L 21/00.

• A material is classified in the corresponding group when an emphasis has been put on said
material, for example with an example.
• Long lists of materials do not require a classification for each material.
• In case the composition of a material may be covered by two or more groups, the document should
be classified in each concerned group. For example, CdSSe should be classified in sulphide of II-
VI and selenide of II-VI semiconductors.

Fullerenes and carbon nanotubes are considered to be organic materials.

H01L 21/02606
{Nanotubes (carbon nanotubes H01L 51/0048)}

References

Limiting references
This place does not cover:

Carbon nanotubes used in semiconductor or solid state devices

H01L 21/02658
{Pretreatments (cleaning in general H01L 21/02041)}

References

Limiting references
This place does not cover:

Ex situ cleaning

H01L 21/02664
{Aftertreatments (planarisation in general H01L 21/304)}

References

Limiting references
This place does not cover:

After-treatments for improving the planarity of the layers, e.g. thermal
smoothening of layers

H01L 21/02697
{Forming conducting materials on a substrate}

Special rules of classification
This group is not used for classification; subject matter relating to the formation of conductive
material on a semiconductor substrate is classified in H01L 21/283 - H01L 21/288, H01L 21/3205 and
H01L 21/768.
Making masks on semiconductor bodies for further photolithographic processing not provided for in group H01L 21/18 or H01L 21/34 {{(photographic masks or originals per se G03F 1/00; registration or positioning of photographic masks or originals G03F 9/00; photographic cameras G03B; control of position G05D 3/00)}}

Definition statement

This place covers:

Formation of masks to be used for etching or patterning, formed out of a layer formed or deposited on the wafer. Includes inorganic masks (metallic or insulating materials) as well as organic masks.

Relationships with other classification places

Composition of photosensitive polymers, see G03F 7/00.

Photographic masks of the stencil tape or originals per se: G03F 1/00

Registration or positioning of photographic masks or originals: G03F 9/00

Photographic cameras G03B

Control of position G05D 3/00

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Category</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>masks for selective growth</td>
<td>H01L 21/02639</td>
</tr>
<tr>
<td>masks for implantation</td>
<td>H01L 21/266</td>
</tr>
<tr>
<td>masks for forming insulating layers</td>
<td>H01L 21/322</td>
</tr>
<tr>
<td>Formation and use of stencil masks</td>
<td>G03F 1/00</td>
</tr>
<tr>
<td>Masks per se, e.g. free standing mask, stencil mask</td>
<td>G03F 1/16, G03F 7/12</td>
</tr>
<tr>
<td>Formation of photoresist masks per se</td>
<td>G03F 7/00</td>
</tr>
<tr>
<td>Formation of masks for non patterning purposes:</td>
<td></td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Category</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photographic cameras</td>
<td>G03B</td>
</tr>
<tr>
<td>Photographic masks or originals per se</td>
<td>G03F 1/00</td>
</tr>
<tr>
<td>Registration or positioning of photographic masks or originals</td>
<td>G03F 9/00</td>
</tr>
<tr>
<td>Control of position</td>
<td>G05D 3/00</td>
</tr>
</tbody>
</table>

Special rules of classification

In main group H01L 21/00 and subgroup thereof, a mask is defined as a layer, which is coated directly onto the surface of the wafer.
A free standing mask (stencil mask) laid on the wafer is not considered as a mask in the sense of H01L 21/00.

Masks are classified in H01L 21/00 only under the condition that its treatment or structure has been specially adapted to the fabrication of a device covered by H01L 21/00. Examples are:

• masks used for more than one technological step during device fabrication,
• masks whose structure, formation or treatment are adapted to the nature of the layers or materials used in the fabrication of semiconductor device, or to the device itself

**H01L 21/0271**

{comprising organic layers}

**Definition statement**

*This place covers:*

Covers polymeric masks, including photo-sensitive masks (photoresist) as well as non photo-sensitive masks, e.g., wax, polyimide etc.

**H01L 21/0273**

{characterised by the treatment of photoresist layers}

**Definition statement**

*This place covers:*

Treatment of photoresist layers peculiar to fabrication of electronic devices.

**H01L 21/0273** covers the treatment of photoresist which is not peculiar to the type of resist (UV, e-beam, ion beam resist), for example:

• method of reflowing the resist,
• method of hardening the resist

**References**

*Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

| Photoresists and processing of photoresists in general | G03F 7/00 |

**Special rules of classification**

• If the treatment is peculiar to the resist type (light, e-beam or ion-beam resist), then it is classified in the corresponding subgroup. If not, remains in H01L 21/0273.
• Chemical amplification is considered to be peculiar to the resist type.
• fabricating masks by irradiating a resist with different types of radiation, e.g. photons and electrons, the document is classified in H01L 21/0273.
**H01L 21/0276**
{using an anti-reflective coating (anti-reflective coating for lithography in general G03F 7/09)}

**Definition statement**
This place covers:
Anti-reflective coatings specially adapted for devices as defined under H01L 21/00.
Covers organic as well as inorganic anti-reflective coatings

**References**

*Informative references*
Attention is drawn to the following places, which may be of interest for search:

| Antireflective coatings for lithography in general | G03F 7/09 |

**H01L 21/0277**
{Electrolithographic processes}

**Definition statement**
This place covers:
Multilayer structures and special structures adapted to evacuate charges, e.g. multilayer resists with a conductive layer.

**Special rules of classification**
Multilayer resists for electrolithography should additionally be classified in G03F 7/00.

**H01L 21/0278**
{Röntgenlithographic or X-ray lithographic processes}

**Definition statement**
This place covers:
Includes multilayer structures.

**Special rules of classification**
Multilayer resists for Röntgenlithography should additionally be classified in G03F 7/00.

**H01L 21/033**
comprising inorganic layers

**Definition statement**
This place covers:
Processes for forming masks comprising inorganic layers.
Special rules of classification

This group H01L 21/033 acts as a head group for inorganic masks for patterning layers. Multiple classification with H01L 21/31144 (masks for etching insulating layers), H01L 21/32139 (masks for etching conductive layers and polysilicon layers) and H01L 21/308 (masks for etching semiconductors) is possible.

H01L 21/033

{for lift-off processes}

Definition statement

This place covers:

Processes for forming masks to be used for lifting off another layer (for example having a multilayer structure or special profile) irrespective of their fabrication process

Example:

References

Limiting references

This place does not cover:

Lifting off for obtaining the mask

H01L 21/0337

H01L 21/0334

{characterised by their size, orientation, disposition, behaviour, shape, in horizontal or vertical plane}

References

Limiting references

This place does not cover:

Masks having an orientation or shape adapted to the requirements of an orientation dependent etching

H01L 21/0334
H01L 21/0335
{characterised by their behaviour during the process, e.g. soluble masks, redeposited masks}

Definition statement
This place covers:
Mask having a shape being directly affected by and during the patterning process, e.g. erosion or redeposition, such that the shape of the mask changes during the patterning process.

H01L 21/0337
{characterised by the process involved to create the mask, e.g. lift-off masks, sidewalls, or to modify the mask, e.g. pre-treatment, post-treatment}

Definition statement
This place covers:
Processes for forming masks involving special processes, like lift-off, or sidewall formation, e.g. deposition on a step followed by anisotropic etching, or to modify the mask, e.g. oxidation of an Aluminium layer, hardening, before etching step.

H01L 21/0338
{Process specially adapted to improve the resolution of the mask}

Definition statement
This place covers:
Process specially adapted to provide a mask below the lithographic resolution limit.

Special rules of classification
Sidewall masks may also be classified in H01L 21/0337. As a sidewall spacer has inherently a sub lithographic size, it does not require an automatic group symbol here.

H01L 21/04
the devices having at least one potential-jump barrier or surface barrier, e.g. PN junction, depletion layer, carrier concentration layer {(multistep processes specially adapted for the manufacture of said devices H01L 29/66007, H01L 29/401; details of semiconductor bodies H01L 29/02)}

Definition statement
This place covers:
The group range from H01L 21/04 - H01L 21/326 covers processes for fabrication of semiconductor devices on substrates belonging to the semiconductors of
- group IV: Si, Ge,
- group IV: carbon, diamond,
- group III-V: GaAs, GaN, InP etc.
- group IV-IV: Silicon Carbide,
- inorganic semiconductors other than the above mentioned materials, e.g. II-VI semiconductors,
- bonding or joining semiconductor bodies
• diffusion, and alloying of impurities in these semiconductor materials
• bombardment of these semiconductor materials with radiation,
• Manufacture of electrodes on these semiconductor materials,
• special treatments of these semiconductor materials, like
  thermal treatments, e.g. gettering
  electroforming
  mechanical treatments of these semiconductor materials
  hydrogenation of these materials
treatments of insulating layers formed on these materials, including planarisation, etching,
deposition conductive or resistive layers on these semiconductor materials
treatment of these conductive layers, like planarisation, oxidation, etching, doping,
treatment of the insulating or conductive layers formed thereon,
planarisation of these semiconductor materials, or of the insulating and conductive layers formed thereon

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formation of insulating layers on semiconductor wafers and the direct</td>
<td>H01L 21/02107</td>
</tr>
<tr>
<td>post-treatment of this formation</td>
<td></td>
</tr>
<tr>
<td>Formation of SOI</td>
<td>H01L 21/7624</td>
</tr>
</tbody>
</table>

Special rules of classification

The presence of a potential jump barrier need not to be specified. Inventions intended to be used in the fabrication of devices having a potential barrier may be classified under H01L 21/04.

H01L 21/0405

{the devices having semiconductor bodies comprising semiconducting carbon, e.g. diamond, diamond-like carbon (multistep processes for the manufacture of said devices H01L 29/66015)}

Definition statement

This place covers:
Passivation of semiconducting carbon, e.g. diamond

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fullerenes, e.g. C60, C70</td>
<td>H01L 51/0046</td>
</tr>
<tr>
<td>Carbon nanotubes</td>
<td>H01L 51/0048</td>
</tr>
</tbody>
</table>
Special rules of classification

Processes for fabricating devices having bodies of diamond not covered by H01L 21/041 - H01L 21/0425 are classified in H01L 21/18 - H01L 21/326 and are also mandatorily classified in H01L 29/1602 as invention information or additional information whenever appropriate.

H01L 21/0445

{the devices having semiconductor bodies comprising crystalline silicon carbide (multistep processes for the manufacture of said devices H01L 29/66053)}

References

Limiting references

This place does not cover:

| Preparation of SiC wafers            | H01L 21/2002 |
| Etching, polishing of semiconducting SiC | H01L 21/304 - H01L 21/3065 |

Special rules of classification

Processes for fabricating devices having bodies comprising crystalline silicon carbide not covered by H01L 21/045 - H01L 21/048 are classified in H01L 21/18 - H01L 21/326 and are also mandatorily classified in H01L 29/1608 as invention information or additional information whenever appropriate.

H01L 21/046

{using ion implantation}

Definition statement

This place covers:

Processes where ion implantation of boron and subsequent annealing does produce a p-doped region in a silicon carbide.

Special rules of classification

Processes where ion implantation of boron and subsequent annealing does not produce a p-doped region are classified elsewhere, e.g. H01L 21/0445.

H01L 21/164

{Oxidation and subsequent heat treatment of the foundation plate (H01L 21/165 takes precedence)}

References

Limiting references

This place does not cover:

| Reduction of the copper oxide or treatment of the oxide layer | H01L 21/165 |
**H01L 21/18**

The devices having semiconductor bodies comprising elements of Group IV of the Periodic System or $\text{A}_{	ext{III}}\text{B}_5$ compounds with or without impurities, e.g. doping materials {([H01L 21/041] - [H01L 21/0425], [H01L 21/045] - [H01L 21/048] take precedence)}

**Definition statement**

This place covers:
Processes and apparatus which, by using the appropriate technology, are clearly suitable for manufacture or treatment of devices whose bodies comprise elements of the fourth group of the Periodic System or $\text{A}_{	ext{III}}\text{B}_5$ compounds, even if the material used is not explicitly specified.

**References**

**Limiting references**

This place does not cover:

| Making n- or p-doped regions for devices having semiconductor bodies of diamond; Changing their shape; Making electrodes | H01L 21/041 - H01L 21/0425 |
| Making n- or p-doped regions for devices having semiconductor bodies comprising crystalline silicon carbide; Changing their shape; Making electrodes; Passivating silicon carbide surfaces | H01L 21/045 - H01L 21/048 |

**H01L 21/185**

{Joining of semiconductor bodies for junction formation}

**Definition statement**

This place covers:
Joining through a metal layer or eutectic layer.

**References**

**Limiting references**

This place does not cover:

| Joining/bonding of semiconductor bodies through an oxide layer | H01L 21/762 |

**H01L 21/187**

{by direct bonding}

**Definition statement**

This place covers:
Direct bonding of semiconductor bodies without intermediate layer.
H01L 21/20
Deposition of semiconductor materials on a substrate, e.g. epitaxial growth {solid phase epitaxy}

Special rules of classification
Groups H01L 21/20 - H01L 21/2085 are no longer used for classification of documents, see H01L 21/02365 and subgroups.

H01L 21/22
Diffusion of impurity materials, e.g. doping materials, electrode materials, into or out of a semiconductor body, or between semiconductor regions; {Interactions between two or more impurities; Redistribution of impurities}

Definition statement
This place covers:
Plasma doping.

Special rules of classification
Plasma doping is considered as doping from a gas phase, as is the case in Plasma Immersion Ion Implantation. Nevertheless, plasma doping can have ion implantation aspects like the type of ions. These aspects should be classified in ion implantation, H01L 21/265. But a group symbol e.g. H01L 21/2236 or an index code e.g. H01L 21/2236 should always be allocated to track the fact it uses a plasma.

H01L 21/223
using diffusion into or out of a solid from or into a gaseous phase
{(H01L 21/221 - H01L 21/222 take precedence; diffusion through an applied layer H01L 21/225)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Diffusion of killers</th>
<th>H01L 21/221</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lithium-drift</td>
<td>H01L 21/222</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Diffusion through an applied layer | H01L 21/225 |
H01L 21/225
using diffusion into or out of a solid from or into a solid phase, e.g. a doped oxide layer {((H01L 21/221 - H01L 21/222 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Diffusion of killers</th>
<th>H01L 21/221</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lithium-drift</td>
<td>H01L 21/222</td>
</tr>
</tbody>
</table>

H01L 21/224
{from or through or into an applied layer, e.g. photoresist, nitrides}

Special rules of classification
In the range H01L 21/224 - H01L 21/2257 the main compositional part of the applied layer just before the diffusion step has to be considered for classification

H01L 21/228
using diffusion into or out of a solid from or into a liquid phase, e.g. alloy diffusion processes {((H01L 21/221 - H01L 21/222 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Diffusion of killers</th>
<th>H01L 21/221</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lithium-drift</td>
<td>H01L 21/222</td>
</tr>
</tbody>
</table>

H01L 21/24
Alloying of impurity materials, e.g. doping materials, electrode materials, with a semiconductor body {((H01L 21/182 takes precedence)}

References
Limiting references
This place does not cover:

| Intermixing, interdiffusion or disordering of AIII-BV heterostructures | H01L 21/182 |
**H01L 21/26**  
Bombardment with radiation \{(H01L 21/3105 takes precedence)\}

References

**Limiting references**

*This place does not cover:*

| Bombardment with radiation as post-treatment of an insulating layer | H01L 21/3105 |

**H01L 21/263**  
with high-energy radiation \(H01L 21/261\) takes precedence)

References

**Limiting references**

*This place does not cover:*

| High energy radiation creating a nuclear transmutation | H01L 21/261 |

**Special rules of classification**

There is no exact border defining high energy. It is meant to cover alpha, beta, gamma, Röntgen... rays. The sub group H01L 21/263 is incorrectly placed as a subgroup.

**H01L 21/265**

producing ion implantation (ion beam tubes for localised treatment H01J 37/30)

References

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Thermal treatment for modifying the properties of semiconductor bodies per se | H01L 21/324 |
| Ion beam tubes for localised treatment | H01J 37/30 |

**H01L 21/266**

using masks \{(H01L 21/26586 takes precedence)\}

References

**Limiting references**

*This place does not cover:*

| Crystal planes or main crystal surface and ion beam present an angle | H01L 21/26586 |
H01L 21/28

Manufacture of electrodes on semiconductor bodies using processes or apparatus not provided for in H01L 21/20 - H01L 21/268; {etching for patterning the electrodes H01L 21/311 and H01L 21/3213}

Definition statement

This place covers:
Includes processes for forming
• conductor-semiconductor,
• conductor-insulator-semiconductor, or
• conductor-insulator-conductor-insulator-semiconductor structures.

Multistep processes for manufacturing electrodes on semiconductor bodies characterized by
• a sequence of single steps, possibly including steps like deposition conductive material, alloying, silicidation,
• the structure or the shape of the electrode,

References

Limiting references

This place does not cover:
Mono-step processes: single diffusion of dopants, alloying of electrode materials, implantation of dopants

| Mono-step processes: single diffusion of dopants, alloying of electrode materials, implantation of dopants | H01L 21/22, H01L 21/24, H01L 21/265 |
| Multi-step processes for forming capacitor electrodes | H01L 28/60 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Etching for patterning electrodes | H01L 21/311 and H01L 21/3213 |

Special rules of classification

Formation of electrodes only involving an etching of conductive materials, including silicide on polysilicon: H01L 21/3213 and subgroups

Information peculiar to single-step processes should also be classified in the corresponding group, e.g.
• H01L 21/311 or H01L 21/3213 for etching,
• H01L 21/027, H01L 21/033, H01L 21/31144 or H01L 21/32139 for masking,
• H01L 21/3105 or H01L 21/321 for planarising

H01L 21/28008

{Making conductor-insulator-semiconductor electrodes}

Definition statement

This place covers:
Processes for the fabrication of conductor-insulator-semiconductor structure, e.g. wherein the conductor is part of the interconnect (gate level interconnect).
References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Monosteps for forming insulators or conductors for which the application to gate electrodes is mentioned without further details.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>H01L 21/02104</strong>, <strong>H01L 21/283</strong></td>
</tr>
</tbody>
</table>

**H01L 21/28017**

{the insulator being formed after the semiconductor body, the semiconductor being silicon}

Definition statement

This place covers:

Deposition of the insulators, using epitaxy

Deposition of the conductor and the insulator within the same process chamber.

**H01L 21/28026**

{characterised by the conductor (**H01L 21/28176** takes precedence)}

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Annealing, after the formation of the definitive gate conductor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>H01L 21/28176</strong></td>
</tr>
</tbody>
</table>

Special rules of classification

When the final conductor comprises a superconductor, subject matter is not classified according to **H01L 21/28035** - **H01L 21/28097**, but instead it is classified in **H01L 21/28026**.

**H01L 21/28035**

{the final conductor layer next to the insulator being silicon, e.g. polysilicon, with or without impurities (**H01L 21/28105** takes precedence)}

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>the final conductor next to the insulator having a lateral composition or doping variation, or being formed laterally by more than one deposition step</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>H01L 21/28105</strong></td>
</tr>
</tbody>
</table>

Special rules of classification

A very thin, e.g. silicon, adhesion or seed layer is not considered as the one next to the insulator
H01L 21/28052
{the conductor comprising a silicide layer formed by the silicidation reaction of silicon with a metal layer (formed by metal ion implantation H01L 21/28044)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Silicide formed by metal ion implantation | H01L 21/28044 |

Special rules of classification
To assess the coverage of groups H01L 21/28052 and H01L 21/28061, barrier layers, e.g. TaSiN, are not considered

H01L 21/28061
{the conductor comprising a metal or metallic silicide formed by deposition, e.g. sputter deposition, i.e. without a silicidation reaction (H01L 21/28052 takes precedence)}

References
Limiting references
This place does not cover:

| Conductors comprising a silicide layer formed by the silicidation reaction of silicon with a metal layer | H01L 21/28052 |

Special rules of classification
To assess the coverage of groups H01L 21/28052 and H01L 21/28061, barrier layers, e.g. TaSiN, are not considered

H01L 21/28114
{characterised by the sectional shape, e.g. T, inverted-T}

Special rules of classification
Documents are also classified in groups H01L 21/28035 - H01L 21/28105 when the composition is also relevant
H01L 21/28123

{Lithography-related aspects, e.g. sub-lithography lengths; Isolation-related aspects, e.g. to solve problems arising at the crossing with the side of the device isolation; Planarisation aspects}

References

Limiting references

This place does not cover:

| Fabrication of lithographic masks for electrodes | H01L 21/027, H01L 21/033 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Lift-off aspects involving multilayer masks | H01L 21/0272 or H01L 21/0331 |

H01L 21/28158

{Making the insulator}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Forming insulating materials on a substrate | H01L 21/02107 |

Special rules of classification

In case the formation of the insulator would be of general interest, a group symbol should be given in H01L 21/02107.

H01L 21/28185

{with a treatment, e.g. annealing, after the formation of the gate insulator and before the formation of the definitive gate conductor}

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| RTN | Rapid Thermal Nitridation |
| RPN | Rapid Plasma Nitridation |
H01L 21/28211
{in a gaseous ambient using an oxygen or a water vapour, e.g. RTO, possibly through a layer (H01L 21/28194 and H01L 21/28202 take precedence)}

References

Limiting references

This place does not cover:

| Evaporation, ALD, CVD, sputtering, laser deposition | H01L 21/28194 |
| Nitride deposition, growth, oxynitridation, NH\textsubscript{3} nitridation, N\textsubscript{2}O oxidation, thermal nitridation, RTN, plasma nitridation, RPN | H01L 21/28202 |

Special rules of classification

Thin oxidation layers used as a barrier layer or as a buffer layer, e.g. before the formation of a high-k insulator, are classified here only if important per se.

H01L 21/28229
{by deposition of a layer, e.g. metal, metal compound or polysilicon, followed by transformation thereof into an insulating layer}

Special rules of classification

In case the transformation would be of general interest it should be classified in

• H01L 21/32105 or H01L 21/3211,
• H01L 21/02107.

H01L 21/283
Deposition of conductive or insulating materials for electrodes {conducting electric current}

Definition statement

This place covers:

H01L 21/283 - H01L 21/2885 cover the deposition of conductive layers directly in contact with the semiconductor for forming electrodes.

References

Limiting references

This place does not cover:

| Formation of electrodes of capacitors, resistors, inductors | H01L 28/00 |

Special rules of classification

Application to contacts must be mentioned with details. Moreover, details of deposition processes of conductive layers covered by H01L 21/3205 are additionally classified in this group and subgroups thereof. If a document discloses information relevant for any of the groups H01L 21/768 - H01L 21/76898, one or more of these groups should also be assigned.
**H01L 21/285**

from a gas or vapour, e.g. condensation

**Definition statement**

*This place covers:*

Methods for depositing conductive layers using gases or vapours of metals or metal-containing precursors.

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition of polysilicon in contact with a semiconductor</td>
<td>H01L 21/02365</td>
</tr>
<tr>
<td>Formation of electrodes of capacitors, resistors, inductors</td>
<td>H01L 21/28</td>
</tr>
</tbody>
</table>

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chemical coating by decomposition of gaseous compounds, without leaving reaction products of surface material in the coating, i.e. chemical vapour deposition (CVD) processes</td>
<td>C23C 16/00</td>
</tr>
</tbody>
</table>

**Special rules of classification**

The deposition process (PVD, CVD, ALD etc.) must be specially adapted for forming contacts or interconnects within semiconductor devices and must be disclosed in detail, i.e. include details on deposition parameters, precursor materials, particular apparatus details etc.

If a document discloses information relevant for any of the groups H01L 21/768 - H01L 21/76898, one or more of these groups should also be assigned.

**H01L 21/28525**

{the conductive layers comprising semiconducting material (H01L 21/28518, H01L 21/28537 take precedence)}

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductive layers comprising silicides</td>
<td>H01L 21/28518</td>
</tr>
<tr>
<td>Deposition of Schottky electrodes</td>
<td>H01L 21/28537</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Deposition of polysilicon on silicon classified there only if application to contacts is mentioned. Otherwise H01L 21/02365
H01L 21/28531

{Making of side-wall contacts}

Special rules of classification
Deposition of polysilicon on silicon classified there only if application to contacts is mentioned. Otherwise H01L 21/02365

H01L 21/288

from a liquid, e.g. electrolytic deposition

Definition statement
This place covers:
The deposition of conductive layers directly in contact with semiconductors for forming electrodes using liquid deposition techniques, e.g. electroless plating.

References

Limiting references
This place does not cover:

Formation of electrodes of capacitors, resistors, inductors H01L 21/28

Informative references
Attention is drawn to the following places, which may be of interest for search:

Chemical coating by decomposition of either liquid compounds or solutions of the coating forming compounds, without leaving reaction products of surface material in the coating C23C 18/00

Special rules of classification
The deposition process must be specially adapted for forming contacts or interconnects within semiconductor devices and must be disclosed in detail, i.e. include details on deposition parameters, precursor materials, particular apparatus details etc.

If a document discloses information relevant for any of the groups H01L 21/768 - H01L 21/76898, one or more of these groups should also be assigned.

H01L 21/30

Treatment of semiconductor bodies using processes or apparatus not provided for in groups H01L 21/20 - H01L 21/26 (manufacture of electrodes thereon H01L 21/28)

Definition statement
This place covers:
• mechanical treatments, like grinding, sand blasting etc.
• hydrogenation of these semiconductors
• chemical treatments, like etching,
• formation of insulating layers and after treatment of these layers, like planarisation, etching, formation of conductive layers on these insulating layers and after treatment of these conductive layers and their doping.

References

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>the treatment of II-VI compounds</td>
<td>H01L 21/02365</td>
</tr>
<tr>
<td>the treatment of insulating layers</td>
<td>H01L 21/31</td>
</tr>
<tr>
<td>the treatment of metallic</td>
<td>H01L 21/3205</td>
</tr>
</tbody>
</table>

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacture of electrodes thereon</td>
<td>H01L 21/28</td>
</tr>
</tbody>
</table>

**H01L 21/304**

Mechanical treatment, e.g. grinding, polishing, cutting {\((H01L 21/30625\ takes precedence)\)}

**Definition statement**

*This place covers:*

Mechanical treatment of semiconductor wafers or semiconductor layers, except the mechanical treatment of insulating or conductive layers on semiconductor wafers.

**Relationships with other classification places**

Mechanical treatment in general:

• grinding, polishing \[B24B\],
• abrasive blasting \[B24C\]

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polishing of semiconductor wafers</td>
<td>H01L 21/0201</td>
</tr>
<tr>
<td>Polishing of epitaxial layers on semiconductor wafers</td>
<td>H01L 21/30625</td>
</tr>
<tr>
<td>Mechanical treatment of insulating layers on wafers</td>
<td>H01L 21/3205</td>
</tr>
<tr>
<td>Conductive layers on wafers</td>
<td>H01L 21/321</td>
</tr>
<tr>
<td>Single step mechanical operations, like sawing, polishing, breaking etc. classified in the corresponding group in section [B]</td>
<td>[B24B, B24C]</td>
</tr>
</tbody>
</table>

**Special rules of classification**

The mere use of a machine is classified with the machine only.
Process for the mechanical treatment, enhanced by chemical treatment, is classified in chemical treatment, but may be given a group symbol in mechanical treatment if the mechanical treatment itself is of importance for the invention.

Purely mechanical polishing is considered as chemical-mechanical polishing, and is classified accordingly.

**H01L 21/3043**

*{Making grooves, e.g. cutting}*

**Definition statement**

*This place covers:*

Making grooves, which may result in cutting

**References**

*Limiting references*

*This place does not cover:*

- Singulation of wafers into dies

**H01L 21/306**

*Chemical or electrical treatment, e.g. electrolytic etching (to form insulating layers H01L 21/31)*

**Definition statement**

*This place covers:*

- Chemical or electrical treatment of group IV or III-V semiconductors.
- Formation of porous semiconductors,
- Functionalisation of semiconductor surfaces

**References**

*Limiting references*

*This place does not cover:*

- Chemical or electrical treatment to form insulating layers

**H01L 21/30608**

*{Anisotropic liquid etching (H01L 21/3063 takes precedence)}*

**Definition statement**

*This place covers:*

Anisotropic liquid etching, i.e. "crystal orientation dependant" etching, using basic (pH>7) compositions. The etch composition is often composed of KOH, amines, azines, quaternary ammonium compounds
References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Electrolytic etching</th>
<th>H01L 21/3063</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anisotropic etching for tartarising surfaces</td>
<td>H01L 31/18</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Etching for fabrication of MEMs.</th>
<th>B81C 1/00539</th>
</tr>
</thead>
</table>

H01L 21/30621

{Vapour phase etching}

Definition statement

This place covers:

Reactive Ion Etching [RIE] of III-V

H01L 21/30625

{With simultaneous mechanical treatment, e.g. mechanico-chemical polishing}

Definition statement

This place covers:

Processes for polishing semiconductors not being part of the sequence for preparing wafers from an ingot (H01L 21/02013 or H01L 21/02024).

Covers polishing or CMP of semiconductor layers deposited on a substrate, like epitaxial layers.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Polishing or CMP of bulk wafers, wherein the polishing is part of the sequence for preparing wafers from an ingot</th>
<th>H01L 21/02013, H01L 21/02024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polishing or CMP of insulating layers</td>
<td>H01L 21/31053</td>
</tr>
<tr>
<td>Polishing or CMP of conductive layers</td>
<td>H01L 21/3212</td>
</tr>
</tbody>
</table>

Special rules of classification

Chemical-mechanical polishing also includes purely mechanical polishing.
H01L 21/3063
Electrolytic etching

References
Limiting references
This place does not cover:

formation of porous materials by electrolysis

Informative references
Attention is drawn to the following places, which may be of interest for search:

Electrolytic etching in general

H01L 21/3065
Plasma etching; Reactive-ion etching

Definition statement
This place covers:

• sputter etching,
• particle (electron, ion, photon) beam enhanced etching
• light assisted etching,
• plasma etching
• dry etching, i.e. using an etching gas without plasma

References
Limiting references
This place does not cover:

Reactive ion etching of III-V materials

Informative references
Attention is drawn to the following places, which may be of interest for search:

Laser etching without reactive atmosphere per se

H01L 21/308
using masks (H01L 21/3063, H01L 21/3065 take precedence)

Definition statement
This place covers:

• Masks used for patterning semiconductors of group IV or III-V, including masks used for plasma etching/patterning, excepted masks for electrolytic etching.
• The fabrication of masks to be used for etching or patterning semiconductors (non-monocrystalline semiconductors being excluded).
References

Limiting references

This place does not cover:

Formation of masks for non patterning purposes, which are classified with the step in question: - masks for implantation - masks for forming insulating layers, - masks for selective growth, - masks for patterning semiconductors belonging to groups other than group IV and group III-V.

Electrolytic etching

Formation and use of stencil masks

Free standing masks, e.g. stencil masks

Formation of photoresist masks per se, except if the formation of the photoresist mask is specific to the device to be fabricated or semiconductor substrate

Informative references

Attention is drawn to the following places, which may be of interest for search:

General masks for patterning in the fabrication of semiconductor device

Masks for patterning insulating layers

Masks for patterning conductors, including polycrystalline or amorphous silicon

Special rules of classification

A mask in **H01L 21/00** is formed of a layer coated directly onto the surface of the wafer.

A free standing mask (stencil mask) laid on the wafer is not considered as a mask in the sense of **H01L 21/00**.

Masks are classified in **H01L 21/308** only under the condition that its treatment or structure has been specially adapted to the fabrication of a device covered by **H01L 21/00**. Examples are:

- masks used for more than one technological step during device fabrication,
- masks whose structure, formation or treatment are adapted to the nature of the layers or materials used in the fabrication of semiconductor device, or to the device itself

The takes precedence rule (stemming from IPC) pointing to **H01L 21/3065** is not valid for CPC: masks for etching by plasma or reactive ion etching are given a group symbol here.

Masks for electrolytic etching are classified with the electrochemical etching in **H01L 21/3063**.

Using stencil masks for ion implantation is classified in **H01L 21/266**.

**H01L 21/3085**

{characterised by their behaviour during the process, e.g. soluble masks, redeposited masks}

Definition statement

*This place covers:*

Masks having a specific behaviour during etching process. e.g. erodible mask, shrinking mask etc.
References

Limiting references

This place does not cover:

| Processes wherein the etching is interrupted to modify the mask (sequential etching), e.g. etching, followed by modifying the mask, followed by re-etching, with possible cycling of the above steps | H01L 21/30604, H01L 21/30625, H01L 21/3063, H01L 21/3065 |

H01L 21/3086

{characterised by the process involved to create the mask, e.g. lift-off masks, sidewalls, or to modify the mask, e.g. pre-treatment, post-treatment}

Definition statement

This place covers:

Covers pre-treatment for the formation of a mask, post treatment of the mask before etching, treatments to modify the mask before use, e.g. hardening, formation of sidewalls, multiple sidewalls etc.

References

Limiting references

This place does not cover:

| Modification of the mask during etching | H01L 21/3085 |
| Removal of the mask after use | H01L 21/31144 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Photoresist for lift | H01L 21/0272 |
| Inorganic masks for lift-off | H01L 21/0331 |

H01L 21/3088

{Process specially adapted to improve the resolution of the mask}

Definition statement

This place covers:

Process specially adapted to go below resolution limit of lithography.
**H01L 21/31**

to form insulating layers thereon, e.g. for masking or by using photolithographic techniques (layers forming electrodes H01L 21/28; encapsulating layers H01L 21/56); After treatment of these layers

**Definition statement**

This place covers:


To be used in any process, formation of interconnects, isolation oxides etc. when the invention is focussed on the insulator.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Insulating layers forming part of electrodes | H01L 21/28 |
| Encapsulating layers | H01L 21/56 |

**H01L 21/3105**

After-treatment

**Definition statement**

This place covers:

Covers special treatments of insulating layers, wherein the special treatment is not a post-treatment as defined under H01L 21/00, i.e. the classical annealing of the insulating layer to improve its characteristics, but is for example planarisation, patterning, functionalization after etching.

**References**

*Limiting references*

This place does not cover:

Classical annealing after formation of the insulator, classified together with the formation | H01L 21/02318 |

**Special rules of classification**

Functionalization just after formation should be classified with the formation.

In case the process would also be of interest as a post treatment, both classes should be given.
**H01L 21/31051**

{Planarisation of the insulating layers (H01L 21/31058 takes precedence)}

**Definition statement**

*This place covers:*

- Planarisation of insulating layers.
- Atomic scale planarisation (smoothening) of the insulating layers.
- Reflow of insulating layers.

**References**

*Limiting references*

*This place does not cover:*

| After treatment, e.g. planarisation, of organic layers | H01L 21/31058 |

**H01L 21/31053**

{involving a dielectric removal step}

**Definition statement**

*This place covers:*

Planarisation involving a removal step not being a chemical etch step: this is the group for polishing and chemical-mechanical polishing (CMP) of insulating materials.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Polishing slurries | C09G, C09K |

**H01L 21/31055**

{the removal being a chemical etching step, e.g. dry etching (etching per se H01L 21/311)}

**Definition statement**

*This place covers:*

Planarisation by non selective etching, e.g. by a blanket etching reducing the protrusions.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Etching per se | H01L 21/311 |
H01L 21/31056
{the removal being a selective chemical etching step, e.g. selective dry etching through a mask}

Definition statement
This place covers:
Processes where protrusions are selectively etched through a mask.

H01L 21/31105
{Etching inorganic layers}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Etching glass | C03C 15/00 |

H01L 21/31111
{by chemical means}

Definition statement
This place covers:
Etching by wet process, or by processes wherein gaseous reactants are condensed on the surface.

Special rules of classification
Gaseous etch with HF is classified in H01L 21/31116

H01L 21/31116
{by dry-etching}

Definition statement
This place covers:
• Plasma etching
• Ion beam etching

H01L 21/31127
{Etching organic layers}

Definition statement
This place covers:
Removal of organic layers or polymers, including photoresists peculiar to semiconductor wafers or devices.
References

Limiting references

This place does not cover:

| The removal of silicon-containing compounds having an organic nature. | H01L 21/31105 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Removal of photoresist not peculiar to semiconductor wafers | G03F 7/42 |

Special rules of classification

Removal of photoresist being not peculiar to semiconductors is classified in G03F 7/42.

Peculiar to semiconductor devices means that particular precautions are taken to avoid influence of the removal of the photoresist on the semiconductor wafer or device.

H01L 21/31133

{by chemical means}

Definition statement

This place covers:

Etching by wet process, or by processes wherein gaseous reactants are condensed on the surface.

H01L 21/31144

{using masks}

Definition statement

This place covers:

Etching involving a specially adapted mask

Special rules of classification

In case the mask would be of general interest, it should also be classified in H01L 21/033.

H01L 21/3115

Doping the insulating layers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| See also after treatment of insulating layers | H01L 21/3105 |
| Doping with the purpose to alter resistivity or increase conductivity | H01L 21/76888 |

Special rules of classification

Implantation or diffusion into insulating layers is also classified under H01L 21/02318 and subgroups.
H01L 21/312
Organic layers, e.g. photoresist (H01L 21/3105, H01L 21/32 take precedence; {photoresists per se G03C})

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Photoresists per se | G03C |

Special rules of classification
H01L 21/312 - H01L 21/3128 are no longer used for classification of new documents, see H01L 21/02112.

H01L 21/314
Inorganic layers (H01L 21/3105, H01L 21/32 take precedence)

Special rules of classification
H01L 21/314 - H01L 21/3185 are no longer used for classification of new documents. See H01L 21/02112.

H01L 21/3205
Deposition of non-insulating-, e.g. conductive- or resistive-, layers on insulating layers; After-treatment of these layers (manufacture of electrodes H01L 21/28)

Definition statement
This place covers:
Deposition of conductive layers exclusively on insulating layers, when the process of deposition is relevant.

References
Limiting references
This place does not cover:

| Deposition of conductive layers on semiconductor | H01L 21/283 - H01L 21/288 |

Special rules of classification
When the technique of deposition is particular (CVD, PVD or electroplating), also classify in H01L 21/283, H01L 21/285 or H01L 21/288. When an interconnection is concerned, see also H01L 21/768 and subgroups.
H01L 21/321

After treatment

Definition statement

This place covers:
Treatment of formed conductive layers. Includes:
- etching by chemical or physical means,
- planarisation, including chemical-mechanical polishing,
- oxidation, nitridation, or surface treatment,
- doping.

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups.

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. After treatment of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32105

{Oxidation of silicon-containing layers}

Definition statement

This place covers:
Oxidation of non-monocrystalline silicon, e.g. polycrystalline, microcrystalline or amorphous silicon.

References

Limiting references

This place does not cover:

| Oxidation of monocrystalline silicon | H01L 21/02236 |

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Oxidation of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/3211

{Nitridation of silicon-containing layers}

Definition statement

This place covers:
Nitridation of non-monocrystalline silicon, e.g. polycrystalline, microcrystalline or amorphous silicon.
References

Limiting references

This place does not cover:

| Nitridation of monocrystalline silicon | H01L 21/02247 |

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Nitridation of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32115

{Planarisation}

Definition statement

This place covers:

Planarisation of conductive or resistive layers.

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Planarisation of these layers is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/3212

{by chemical mechanical polishing [CMP]}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| CMP slurries | C09G |

H01L 21/3213

Physical or chemical etching of the layers, e.g. to produce a patterned layer from a pre-deposited extensive layer

Definition statement

This place covers:

Physical or chemical etching of conductive or resistive layers.

Etching of polysilicon layers

Etching of amorphous silicon layers
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Machines or apparatus for liquid etching                     | H01L 21/67 |
| Machines for plasma etching                                 | H01J 37/00 |

Special rules of classification

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Etching of layers of these materials is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32131
{by physical means only}

Definition statement

This place covers:
Etching processes, where no chemical reaction is involved, e.g.
sputtering, ion milling, laser ablation, pure ion beam etching.

Special rules of classification

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/32132
{of silicon-containing layers}

Definition statement

This place covers:
Silicides and silicon alloys.

H01L 21/32133
{by chemical means only}

Definition statement

This place covers:
Use of Plasmas, e.g. RIE, and chemically assisted particle (ion or electron, photon) beam etching

Special rules of classification

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.
H01L 21/32134
{by liquid etching only}

Definition statement
This place covers:
Etching with supercritical fluids

H01L 21/32136
{using plasmas}

Definition statement
This place covers:
Etching assisted by electrons, ions and laser beams.

H01L 21/32137
{of silicon-containing layers}

Definition statement
This place covers:
Polysilicon, amorphous, silicides, multilayers containing silicon

H01L 21/32138
{pre- or post-treatments, e.g. anti-corrosion processes}

Definition statement
This place covers:
Pre-treatments before etching, including removal of natural oxide.
Anti-corrosion post-treatments.

References
Limiting references
This place does not cover:
Post-treatment after etching, e.g. RIE

Special rules of classification
In case the pre-treatment is a removal of natural oxide and is of general interest, a group symbol in H01L 21/02041 should be given.

In case the post treatment is a passivation by oxidation or nitridation this step should be classified independently.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.
H01L 21/32139

{using masks}

**Definition statement**

*This place covers:*

Etching involving a mask specifically adapted to the etching operation.

**References**

**Limiting references**

*This place does not cover:*

| Classical photoresist masks, except if submitted to a special treatment, for example hardening, fluorination, etc. | G03F 7/00 |

**Special rules of classification**

In case the mask would be of general interest, it should also be classified in H01L 21/033.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/3215

**Doping the layers**

**Special rules of classification**

Polysilicon, amorphous silicon and silicides are considered as conductive materials for these groups. Doping of these layers is thus classified here.

For classifying in the group range H01L 21/321 - H01L 21/3215, the explicit presence of an insulating layer below the conductive or resistive layers is not mandatory.

H01L 21/322

**to modify their internal properties, e.g. to produce internal imperfections**

**Definition statement**

*This place covers:*

- Treatments aimed at modifying the intrinsic properties of the crystals not otherwise provided for in H01L 21/00, like crystallographic defect rate.
- Formation of defects for intrinsic or extrinsic gettering

**References**

**Limiting references**

*This place does not cover:*

| Modification of conductivity type | H01L 21/3242 |
H01L 21/3221
{of silicon bodies, e.g. for gettering}

**Definition statement**

*This place covers:*
Extrinsic gettering

**Special rules of classification**

Gettering using both extrinsic and intrinsic gettering techniques is classified in both H01L 21/3221 and H01L 21/3225.

H01L 21/3225

{Thermally inducing defects using oxygen present in the silicon body for intrinsic gettering (H01L 21/3226 takes precedence)}

**Definition statement**

*This place covers:*
Intrinsic gettering

**References**

*Limiting references*

*This place does not cover:*

| Treatment of semiconductor bodies to modify their internal properties of silicon on insulator | H01L 21/3226 |

**Special rules of classification**

Gettering using both extrinsic and intrinsic gettering techniques is classified in both H01L 21/3221 and H01L 21/3225.

H01L 21/34

the devices having semiconductor bodies not provided for in groups {H01L 21/0405, H01L 21/0445}, H01L 21/06, H01L 21/16 and H01L 21/18 with or without impurities, e.g. doping materials

**Definition statement**

*This place covers:*

Processes for fabricating devices having semiconductor bodies not belonging to group IV, IV-IV, III-V materials, or to Se, Te, CuO.

Processes for fabricating devices having semiconductor bodies based on II-VI materials.


References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inorganic semiconducting materials used for light detecting devices, e.g.</td>
<td>H01L 31/0264,</td>
</tr>
<tr>
<td>I-III-VI materials, like CuInSe</td>
<td>H01L 31/0322</td>
</tr>
<tr>
<td>Processes peculiar to the fabrication of light sensitive devices</td>
<td>H01L 31/18</td>
</tr>
<tr>
<td>Processes peculiar to the fabrication of inorganic light emitting devices</td>
<td>H01L 33/00</td>
</tr>
</tbody>
</table>

Special rules of classification

As already evident from the limiting reference in the main group title of H01L 21/00, only fabrication processes relating to devices covered by main groups H01L 21/00 - H01L 29/00 should be classified under H01L 21/34.

- A single mention of an application in manufacturing devices covered by main groups H01L 21/00 - H01L 29/00, e.g. a junction FET, is sufficient to give a group symbol.
- At the other hand processes wherein the type of fabricated device is not mentioned at all will be considered to refer to devices not belonging to those covered by H01L 21/00 - H01L 29/00, and will consequently be classified together with the most probable application, e.g. H01L 31/00 for II-VI for light-sensitive devices.

H01L 21/38

Diffusion of impurity materials, e.g. doping materials, electrode materials, into or out of a semiconductor body, or between semiconductor regions

Definition statement

This place covers:

Doping of II-VI materials.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor bodies composed of II-VI compounds for light sensitive devices</td>
<td>H01L 31/0296</td>
</tr>
</tbody>
</table>

H01L 21/42

Bombardment with radiation

Definition statement

This place covers:

Radiation covers corpuscular as well as electromagnetic radiation

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bombardment with radiation for deposition purposes</td>
<td>H01L 21/02104</td>
</tr>
</tbody>
</table>
Bombardment with radiation for etching purposes

H01L 21/425

producing ion implantation (ion beam tubes for localized treatment H01J 37/30)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Ion beam tubes for localized treatment H01J 37/30

H01L 21/426

using masks

Definition statement

This place covers:

Processes for implantation wherein the invention is focused on the mask aspect, e.g. mask having a specific topography.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Masks in general H01L 21/027 and H01L 21/033

H01L 21/44

Manufacture of electrodes on semiconductor bodies using processes or apparatus not provided for in groups H01L 21/38 - H01L 21/428

Definition statement

This place covers:

Electrodes on semiconductor materials as defined under H01L 21/34.

Covers the direct deposition of conductive materials on the semiconductor and on an insulating layer overlying the semiconductor (e.g. Tunnel contact).

The group H01L 21/44 includes specific treatments of the semiconductor before formation of the contact (e.g. degenerescence by bombardment etc.).

References

Limiting references

This place does not cover:

semiconductor materials of group IV or III-V H01L 21/18
**H01L 21/441**

Deposition of conductive or insulating materials for electrodes

**Definition statement**

*This place covers:*

Insulating materials, only if the contact is a tunnelling contact.

**H01L 21/445**

from a liquid, e.g. electrolytic deposition

**Definition statement**

*This place covers:*

- Electrolytic deposition
- Electroless deposition

**H01L 21/447**

involving the application of pressure, e.g. thermo-compression bonding

**Special rules of classification**

Classification is made in this group only if specific to the semiconductor material, or adapted to the type of device.

**H01L 21/449**

involving the application of mechanical vibrations, e.g. ultrasonic vibrations

**Special rules of classification**

Classification is made in this group only if specific to the semiconductor material, or adapted to the type of device.

**H01L 21/46**

Treatment of semiconductor bodies using processes or apparatus not provided for in groups H01L 21/428 (manufacture of electrodes thereon H01L 21/44)

**Definition statement**

*This place covers:*

The treatment of semiconductor bodies including

- mechanical treatments, like grinding, sand blasting etc.
- chemical treatments, like etching,
- after-treatments of these semiconductors, like formation of insulating layers, planarisation or etching of these insulating layers, formation of conductive layers on these insulating layers and after treatment of these conductive layers and their doping.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Manufacture of electrodes thereon | H01L 21/44 |

H01L 21/465

Chemical or electrical treatment, e.g. electrolytic etching (to form insulating layers H01L 21/469)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Chemical or electrical treatment to form insulating layers thereon | H01L 21/469 |

H01L 21/467

using masks

References

Limiting references

This place does not cover:

| Masks used for patterning group IV and group III-V semiconductors | H01L 21/308 |

H01L 21/469

to form insulating layers thereon, e.g. for masking or by using photolithographic techniques (layers forming electrodes H01L 21/44; encapsulating layers H01L 21/56); After-treatment of these layers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Layers forming electrodes | H01L 21/44 |
| Encapsulating layers | H01L 21/56 |
**H01L 21/47**

Organic layers, e.g. photoresist (H01L 21/475, H01L 21/4757 take precedence)

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Task</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forming insulating layers using masks</td>
<td>H01L 21/475</td>
</tr>
<tr>
<td>After-treatment</td>
<td>H01L 21/4757</td>
</tr>
</tbody>
</table>

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Task</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formation of photoresist masks</td>
<td>H01L 21/027, G03F 7/00</td>
</tr>
</tbody>
</table>

**H01L 21/4763**

Deposition of non-insulating, e.g. conductive -, resistive -, layers on insulating layers; After-treatment of these layers (manufacture of electrodes H01L 21/28, (H01L 21/44))

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Task</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacture of electrodes</td>
<td>H01L 21/28</td>
</tr>
</tbody>
</table>

**H01L 21/48**

Manufacture or treatment of parts, e.g. containers, prior to assembly of the devices, using processes not provided for in a single one of the subgroups H01L 21/06 - H01L 21/326 (apparatus therefor H01L 21/67005; insulative sealing of leads in bases H01L 21/50); containers, encapsulations, fillings, mountings per se H01L 23/00; (marking of parts H01L 23/544))

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Task</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arrangements for connecting or disconnecting semiconductor or other solid state bodies, or methods related thereto, other than those</td>
<td>H01L 24/00</td>
</tr>
</tbody>
</table>

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Task</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insulating sealing of leads in bases</td>
<td>H01L 21/50</td>
</tr>
<tr>
<td>Apparatus therefor</td>
<td>H01L 21/67</td>
</tr>
</tbody>
</table>
Special rules of classification

In this group, the expression "treatment" also covers the removal of leads from parts

**H01L 21/50**

Assembly of semiconductor devices using processes or apparatus not provided for in a single one of the subgroups H01L 21/06 - H01L 21/326, {e.g. sealing of a cap to a base of a container}

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Arrangements for connecting or disconnecting semiconductor or other solid state bodies, or methods related thereto, other than those</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 24/00</td>
</tr>
</tbody>
</table>

**H01L 21/67**

Apparatus specially adapted for handling semiconductor or electric solid state devices during manufacture or treatment thereof; Apparatus specially adapted for handling wafers during manufacture or treatment of semiconductor or electric solid state devices or components {; Apparatus not specifically provided for elsewhere (processes per se H01L 21/30, H01L 21/46, H01L 23/00; simple temporary support means, e.g. using adhesives, electric or magnetic means H01L 21/68, H01L 21/302; apparatus for manufacturing arrangements for connecting or disconnecting semiconductor or solid-state bodies and for methods related thereto H01L 24/74;)}

Definition statement

This place covers:

the apparatus of the title and also the use of those apparatus

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Welding apparatus</th>
</tr>
</thead>
<tbody>
<tr>
<td>B23K 20/00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Polishing apparatus</th>
</tr>
</thead>
<tbody>
<tr>
<td>B24B 1/00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Apparatus for cutting semiconductor ingot</th>
</tr>
</thead>
<tbody>
<tr>
<td>B28D 5/00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Coating apparatus</th>
</tr>
</thead>
<tbody>
<tr>
<td>C23C 14/00, C23C 16/00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Electroplating apparatus</th>
</tr>
</thead>
<tbody>
<tr>
<td>C25D 7/12</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Optical measuring apparatus</th>
</tr>
</thead>
<tbody>
<tr>
<td>G01N 21/00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Testing apparatus</th>
</tr>
</thead>
<tbody>
<tr>
<td>G01R 31/00</td>
</tr>
</tbody>
</table>
Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Cleaning in general</th>
<th>B08B 1/00, B08B 3/00, B08B 5/00, B08B 6/00, B08B 7/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutting in general</td>
<td>B23K 26/00</td>
</tr>
<tr>
<td>Robots in general</td>
<td>B25J 9/00</td>
</tr>
<tr>
<td>Conveying in general</td>
<td>B65G 49/00</td>
</tr>
<tr>
<td>Electrostatic holders in general</td>
<td>H02N 13/00</td>
</tr>
</tbody>
</table>

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| Substrate | a substrate suitable for semiconductor or electric solid state devices or semiconductor or electric solid state components, e.g. a wafer |

H01L 21/67017

{Apparatus for fluid treatment (H01L 21/67126, H01L 21/6715 take precedence)}

Definition statement

This place covers:

- Fluid delivery or exhaust systems (like plumbing, heat exchanger, valves systems, flow regulations means, pumping means) in direct connection with semiconductor manufacture or handling systems.
- Atmosphere control systems in relation with semiconductor industry

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Apparatus for sealing, encapsulating, glassing, decapsulating</th>
<th>H01L 21/67126</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apparatus for applying a liquid, a resin, an ink</td>
<td>H01L 21/6715</td>
</tr>
<tr>
<td>Details relating to the exhausts (e.g. pumps, filters, scrubber) of coating apparatus</td>
<td>C23C 16/4412</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Containers with atmosphere control | H01L 21/67389 |

72
H01L 21/67028
{for cleaning followed by drying, rinsing, stripping, blasting or the like}

Definition statement
This place covers:
- Apparatus dealing with at least two processing steps taking place successively (like cleaning, drying, rinsing, stripping or blasting) are classified in this group.
- Systems for only dry cleaning.

H01L 21/67092
{Apparatus for mechanical treatment (or grinding or cutting, see the relevant groups in subclasses B24B or B28D)}

Definition statement
This place covers:
- apparatus for dividing wafers into a plurality of parts (dicing),
- apparatus for exerting a pressure on a substrate (like apparatus for bonding two wafers together),
- apparatus for separating two bonded wafers.

References
Limiting references
This place does not cover:

| Cutting apparatus per se                      | B23K 26/00 |
| Polishing apparatus                          | B24B 1/00  |
| Apparatus for cutting semiconductor ingot    | B28D 5/00  |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Division of the substrate into plural individual devices | H01L 21/78 |

H01L 21/67103
{mainly by conduction}

Definition statement
This place covers:
- Apparatus where the substrate is in direct contact with the heating element
- Heating elements with specific thermal properties (like thermal conductivity), e.g. materials of the heating element.
H01L 21/67109
{mainly by convection}

Definition statement

This place covers:
- Apparatus where the substrate is not in direct contact with the heating element
- Thermal apparatus with cooling means, e.g. for temperature regulation

H01L 21/67115
{mainly by radiation}

Definition statement

This place covers:
Thermal apparatus comprising lamps, Infra-Red light irradiation means or Ultra-Violet light irradiation means

H01L 21/67126
{Apparatus for sealing, encapsulating, glassing, decapsulating or the like (processes H01L 23/02, H01L 23/28)}

Definition statement

This place covers:
- Sealing arrangements (like O-ring) for a process chamber, a holding or transporting device
- Slit valves or gates for closing the opening of a chamber

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Containers; Seals for semiconductor devices</th>
<th><strong>H01L 23/02</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Encapsulations, e.g. encapsulating layers, coatings for protection</td>
<td><strong>H01L 23/28</strong></td>
</tr>
</tbody>
</table>

H01L 21/67132

{Apparatus for placing on an insulating substrate, e.g. tape}

Definition statement

This place covers:
- All apparatus dealing with tapes (tape removal apparatus, tape placing apparatus)
- Apparatus for removing dies from an adhesive tape (on which a severed wafer is placed).
H01L 21/67144
{Apparatus for mounting on conductive members, e.g. leadframes or conductors on insulating substrates}

Definition statement
This place covers:
Pick and Place apparatus (picking a die from a wafer and placing it on a different location).

H01L 21/6715
{Apparatus for applying a liquid, a resin, an ink or the like (H01L 21/67126 takes precedence)}

References
Limiting references
This place does not cover:

Apparatus for sealing, encapsulating, glassing, decapsulating

H01L 21/67126

H01L 21/67213
{comprising at least one ion or electron beam chamber (coating by ion implantation C23C; ion or electron beam tubes H01J 37/00)}

References
Limiting references
This place does not cover:

Coating by ion implantation

C23C

Informative references
Attention is drawn to the following places, which may be of interest for search:

Ion or electron beam tubes

H01J 37/00

H01L 21/67219
{comprising at least one polishing chamber (polishing apparatuses B24B)}

References
Limiting references
This place does not cover:

Polishing apparatuses per se

B24B
H01L 21/67225
{comprising at least one lithography chamber (lithographic apparatuses
G03F 7/00)}

References

Limiting references
This place does not cover:

| Lithographic apparatuses per se | G03F 7/00 |

H01L 21/6723
{comprising at least one plating chamber (electroless plating apparatuses
C23C, electroplating apparatuses C25D)}

References

Limiting references
This place does not cover:

| Electroless plating apparatuses | C23C |
| Electroplating apparatuses     | C25D |

H01L 21/67242
{Apparatus for monitoring, sorting or marking (testing or measuring during
manufacture H01L 22/00, marks per se H01L 23/544; testing individual
semiconductor devices G01R 31/26)}

References

Limiting references
This place does not cover:

| Electrical testing individual semiconductor devices | G01R 31/26 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Testing or measuring | H01L 22/00 |
| Marks per se        | H01L 23/544 |
H01L 21/67276

{Production flow monitoring, e.g. for increasing throughput (program-control systems per se G05B 19/00, e.g. total factory control G05B 19/418)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Program-control systems per se | G05B 19/00 |
| Total factory control          | G05B 19/418 |

H01L 21/673

using specially adapted carriers {or holders; Fixing the workpieces on such carriers or holders (holders for supporting a complete device in operation H01L 23/32)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Holders for supporting a complete device in operation | H01L 23/32 |

H01L 21/67333

{Trays for chips (magazine for components H05K 13/0084)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Magazine for components | H05K 13/0084 |

H01L 21/6734

{specially adapted for supporting large square shaped substrates (containers and packaging elements for glass sheets B65D 85/48, transporting of glass products during their manufacture C03B 35/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Containers and packaging elements for glass sheets | B65D 85/48 |
| Transporting of glass products during their manufacture | C03B 35/00 |
H01L 21/67363
{specially adapted for containing substrates other than wafers (H01L 21/67356, H01L 21/67359 take precedence)}

References
Limiting references
This place does not cover:
- Closed carriers specially adapted for containing chips, dies or ICs
- Closed carriers specially adapted for containing masks, reticles or pellicles

H01L 21/67366
{characterised by materials, roughness, coatings or the like (materials relating to an injection moulding process B29C 45/00; chemical composition of materials C08L 51/00)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:
- Materials relating to an injection moulding process
- Chemical composition of macromolecular compounds

H01L 21/67706
{Mechanical details, e.g. roller, belt (H01L 21/67709 takes precedence)}

References
Limiting references
This place does not cover:
- Conveying using magnetic elements

H01L 21/67721
{the substrates to be conveyed not being semiconductor wafers or large planar substrates, e.g. chips, lead frames (H01L 21/6773 takes precedence)}

References
Limiting references
This place does not cover:
- Conveying cassettes, containers or carriers
H01L 21/67742
{Mechanical parts of transfer devices (robots in general in B25J)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Robots in general | B25J |

H01L 21/67763
{the wafers being stored in a carrier, involving loading and unloading (H01L 21/6779 takes precedence)}

References
Limiting references
This place does not cover:

| The workpieces being stored in a carrier, involving loading and unloading | H01L 21/6779 |

H01L 21/67766
{Mechanical parts of transfer devices (robots in general in B25J)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Robots in general | B25J |

H01L 21/67784
{using air tracks}

Definition statement
This place covers:
Apparatus for moving substrates on a liquid track

H01L 21/67796
{with angular orientation of workpieces (H01L 21/67787 and H01L 21/67793 take precedence)}

References
Limiting references
This place does not cover:

| Conveying with angular orientation of the workpieces | H01L 21/67787 |
Conveying with orientating and positioning by means of a vibratory bowl or track

H01L 21/67793

H01L 21/68
for positioning, orientation or alignment (for conveying H01L 21/677)

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

Conveying
H01L 21/677

H01L 21/682
{Mask-wafer alignment (in general G03F 7/70, G03F 9/70)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

Alignment in general
G03F 7/70, G03F 9/70

H01L 21/683
for supporting or gripping (for conveying H01L 21/677, for positioning, orientation or alignment H01L 21/68)

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

Conveying
H01L 21/677

Positioning, orientation or alignment
H01L 21/68

H01L 21/6835
{using temporarily an auxiliary support}

References

Limiting references
This place does not cover:

Temporary protection of the devices or parts of the devices during manufacture
B81C 2201/05
H01L 21/6836
{Wafer tapes, e.g. grinding or dicing support tapes (adhesive tapes in general C09J 7/20)}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Adhesive tapes in general | C09J 7/20 |

H01L 21/687

using mechanical means, e.g. chucks, clamps or pinches {(using electrostatic chucks H01L 21/6831)}

References

Limiting references
This place does not cover:

| Using electrostatic chucks | H01L 21/6831 |

H01L 21/70

Manufacture or treatment of devices consisting of a plurality of solid state components formed in or on a common substrate or of parts thereof; Manufacture of integrated circuit devices or of parts thereof {{multistep manufacturing processes of assemblies consisting of a plurality of individual semiconductor or other solid state devices H01L 25/00; } manufacture of assemblies consisting of preformed electrical components H05K 3/00, H05K 13/00}

Definition statement
This place covers:

- Process for the integration of a plurality of solid state devices in or on a common substrate.
- Processes for making isolation regions between components (e.g. LOCOS, STI etc.)
- Processes for fabricating SOI substrates.
- Processes for making interconnections between the solid state devices, on the surface of the substrate, or buried in the substrate, including specific treatments of these interconnections.
- Processes for cutting wafers to singulate the devices, dicing.
- Processes to fabricate devices consisting of a plurality of solid state components or integrated circuits of the bipolar, Field-Effect type and memories.
- Process for the assembly on a common substrate of two or more components.

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Manufacture of assemblies consisting of preformed electrical components | H05K 3/00, H05K 13/00 |
H01L 21/71

Manufacture of specific parts of devices defined in group H01L 21/70
((H01L 21/0405, H01L 21/0445), H01L 21/28, H01L 21/44, H01L 21/48 take precedence)

Definition statement

This place covers:

• Multistep processes for the fabrication of buried regions, also used as buried connections between zones,
• Multistep processes for the fabrication of zones providing electrical isolation between adjacent components,
• Multistep processes for the fabrication of SOI wafers, for which the fabrication of devices has not started yet,
• Multistep processes for the fabrication of interconnections between devices,
• Multistep processes for the fabrication of integrated circuits, bipolar technology, field-effect technology, CMOS, memories, IC based on combinations of these technologies,
• Multistep processes for dicing wafers into individual devices.

References

Limiting references

This place does not cover:

| Processing of parts of devices based on carbon or diamond | H01L 21/0405 |
| Processing of parts of devices based on crystalline Silicon Carbide | H01L 21/0445 |
| Multistep processes for the manufacture of electrodes | H01L 21/28 or H01L 21/44 |
| Manufacture or treatment of parts prior to assembly of the devices, like leads, heat-sinks, etc. | H01L 21/48 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Wire-like connections | H01L 24/00 |

H01L 21/74

Making of {localized} buried regions, e.g. buried collector layers, internal connections {substrate contacts}

Definition statement

This place covers:

Multistep processes for the fabrication of buried regions, like buried collector layers, buried connections between zones, substrate contacts, as part of a component, e.g. formation of buried silicides.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Technique</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusing impurities</td>
<td>H01L 21/22</td>
</tr>
<tr>
<td>Implanting impurities</td>
<td>H01L 21/265</td>
</tr>
</tbody>
</table>

H01L 21/743

{Making of internal connections, substrate contacts}

Definition statement

This place covers:

Fabrication of buried metallic or near metallic regions, like buried silicides, buried eutectic conductors.

H01L 21/76

Making of isolation regions between components

Definition statement

This place covers:

• Fabrication of zones aimed at providing electrical isolation between adjacent components, i.e. dielectric regions (LOCOS, trench, shallow trench), air gaps, p-n junction or field effect.
• Fabrication of SOI wafers, for which the fabrication of devices has not started yet.

Special rules of classification

For subject matter classified in the range H01L 21/76 - H01L 21/765, when the isolation combines several techniques, both techniques are given a group symbol.

When the combination of several techniques involves the fabrication of SOI, a group symbol within the range H01L 21/76264 - H01L 21/76291 is given.

Single steps, like etching a trench, when they present a general interest or are specifically disclosed, should be given a group symbol in the corresponding single step covered by H01L 21/02 and subgroups.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>horizontal</td>
<td>in the plane of the wafer</td>
</tr>
<tr>
<td>vertical</td>
<td>in a direction perpendicular to the plane of the wafer</td>
</tr>
</tbody>
</table>

H01L 21/762

Dielectric regions {, e.g. EPIC dielectric isolation, LOCOS; Trench refilling techniques, SOI technology, use of channel stoppers}

Definition statement

This place covers:

Covers the formation of dielectric regions by
• Oxidation of the substrate, or
• Deposition of a dielectric, for example in a trench.
• Formation of dielectric regions buried in the substrate, SOI

H01L 21/7624
{using trench refilling with dielectric materials (trench filling with polycrystalline silicon H01L 21/763; together with vertical isolation, e.g. trench refilling in a SOI substrate H01L 21/7624})

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Trench filling with vertical isolation, e.g. trench refilling in a SOI substrate | H01L 21/76264 |
| Trench filling with polycrystalline silicon | H01L 21/763 |

H01L 21/7624
{using semiconductor on insulator [SOI] technology (H01L 21/76297 takes precedence; manufacture of integrated circuits on insulating substrates H01L 21/84; silicon on sapphire [SOS] technology H01L 21/86})

Definition statement

This place covers:
The groups H01L 21/7624 - H01L 21/76291 cover the fabrication of a buried isolation region

References

Limiting references

This place does not cover:

| Dielectric isolation using EPIC techniques, i.e. epitaxial passivated integrated circuit | H01L 21/76297 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Manufacture of integrated circuits on insulating substrates | H01L 21/84 |
| Silicon on sapphire (SOS) technology | H01L 21/86 |
H01L 21/768

Applying interconnections to be used for carrying current between separate components within a device {comprising conductors and dielectrics}

Definition statement

This place covers:

Multi-steps processes for manufacturing interconnections on the surface of a device or through the wafer.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Fabrication of contacts</th>
<th>H01L 21/28</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal interconnections</td>
<td>H01L 21/743</td>
</tr>
<tr>
<td>Fabrication of fuses and anti-fuses</td>
<td>H01L 23/525</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Cleaning</th>
<th>H01L 21/02041</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formation of insulating layers</td>
<td>H01L 21/02107</td>
</tr>
<tr>
<td>Formation or use of masks</td>
<td>H01L 21/027, H01L 21/033, H01L 21/31144, H01L 21/32139</td>
</tr>
<tr>
<td>Planarising insulating or conductive layers</td>
<td>H01L 21/3105, H01L 21/321</td>
</tr>
<tr>
<td>Etching of insulating or conductive layers</td>
<td>H01L 21/311, H01L 21/3213</td>
</tr>
</tbody>
</table>

Special rules of classification

Information peculiar to single-step processes should also be classified in the corresponding sub group of H01L 21/02 (see informative references below).

Processes for fabricating fuses and anti-fuses are classified with the fuses and anti-fuses in H01L 23/525.

H01L 21/76804

{by forming tapered via holes}

Definition statement

This place covers:

Methods specially adapted for forming via or contact holes having a wider top or bottom region, e.g. "cup-shaped" vias
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Etching insulating layers per se  H01L 21/311

H01L 21/76805

{the opening being a via or contact hole penetrating the underlying conductor}

Definition statement

This place covers:

Methods of forming via or contact holes including a step of etching the conductor at the bottom of the hole so as to form e.g. a gouging feature;

methods of forming contact holes having a portion reaching into conductive regions (e.g. source and drain) of the semiconductor substrate

H01L 21/76808

{involving intermediate temporary filling with material}

Definition statement

This place covers:

Methods of dual damascene processing involving intermediate temporary filling of the opening first formed in the process with material, e.g. planarisation to facilitate lithography of the second opening

Examples:

• After formation of the via, the via is filled with a resin film 12 to provide for planarisation:

![Figure 2B](image)

• The dual damascene structure of a lower metal level 200 is filled with a sacrificial material 140 (see the figure below), then another metal level 202 having dual damascene structures 232 is fabricated. Finally, the sacrificial layer 140 is removed and all metal levels are metalized simultaneously:
This place does not cover:

Conventional trench-first dual damascene methods in which the photoresist for forming the via hole fills the trench

**References**

**Limiting references**

*This place does not cover:*

Conventional trench-first dual damascene methods in which the photoresist for forming the via hole fills the trench

**H01L 21/7681**

{involving one or more buried masks}

**Definition statement**

*This place covers:*

Methods of dual damascene processing involving one or more buried masks, i.e. one or more pre-patterned mask or etch stop layers are fabricated prior to deposition of the trench-level dielectric.

Examples:

- The etch stop 114 is pre-patterned and buried under ILD 118 (see the figure below):
**Definition statement**

This place covers:

Methods of dual damascene processing involving multiple stacked pre-patterned masks on the trench-level dielectric, i.e. mask stacks pre-defining the trench and via patterns before the actual etching process.

Examples:

Layers 135, 140, 150 are hardmask layers, layer 180 is a photoresist for patterning layer 150. The dual damascene structure is transferred into the ILD 130 with the help of the stack of pre-patterned hardmasks 135, 140, 150.
**H01L 21/76813**

{involving a partial via etch}

**Definition statement**

*This place covers:*

All dual damascene processes in which in an early stage a via is formed partially through the dielectric stack. The via etch is completed later in the process, e.g. during the etching step for forming the trench.

**Examples:**

First, the via is partially etched into the dielectric stack. In a later step, the via etch is completed together with the trench etch.

**Special rules of classification**

Dual damascene processing also involving a stack of pre-patterned hard mask layers, the group symbol H01L 21/76811 is also assigned.

If the partial via process also includes a step of intermediate filling the partial via with a planarising material, the document needs to be classified in H01L 21/76808, too.

**H01L 21/76814**

{post-treatment or after-treatment, e.g. cleaning or removal of oxides on underlying conductors}

**Definition statement**

*This place covers:*

Particular method steps designed for improving the result of a process of forming an interconnect opening in a dielectric, e.g. removal of oxides from the surface of a conductor at the bottom of a via hole, removal of etching residues, or treatments restoring the dielectric at the sidewalls.
Examples:

After formation of the opening 10, the photoresist mask and etch residues are removed using a reducing plasma. During this treatment an undesired coating layer 14 forms on the sidewalls of opening 10. Layer 14 is eventually removed by the directional beam of charged oxidizing particles having its main axis 20 parallel to the sidewalls of opening 10:

Note that in this case the sidewall layer 14 is an undesired by-product of a plasma treatment process. The document should therefore not be classified in H01L 21/76831.

After forming an opening in a low-k dielectric, a degassing treatment and a plasma treatment are carried out in order to remove methyl groups from the dielectric and an oxide from the underlying conductor 22A:
References

Limiting references

This place does not cover:

| After-treatment steps leading to the formation of modified sidewall layers | H01L 21/76831 |

Special rules of classification

If the method of after-treatment comprises aspects which are classified in any one of the subgroups H01L 21/76822+ (see below), the corresponding group should also be given. If the after-treatment leads to the formation of a sidewall layer in the opening comprising modified dielectric material, the group H01L 21/76831 should also be assigned (note, however, that if the sidewall insulation is formed by a conventional deposition step, H01L 21/76831 is the only relevant group).

H01L 21/76814 is essentially a multistep group, i.e. the after treatment step is only one of several steps to be carried out in order to form an interconnection. If a document exclusively relates to cleaning of openings in dielectrics (in a single-step fashion), the main group symbol is H01L 21/02063.

H01L 21/76816

{Aspects relating to the layout of the pattern or to the size of vias or trenches (layout of the interconnections per se H01L 23/528; CAD of ICs G06F 17/50)}

Definition statement

This place covers:

The geometrical "aspects" to be classified in this group are mainly methodological aspects, e.g. step sequences leading to a reduction of the pitch between via holes, step sequences for incorporating a plurality of vias of different depth, methods of forming vias having a particular cross-sectional shape.

Examples:

Layer 230 is introduced into the structure to enable the simultaneous formation of a deep and a not-so-deep via. Although the formation of the vias themselves contains no special features at all, there is an aspect related "to the size of the vias":

[Diagram of layer 230 introduction]
Method for decreasing the pitch between adjacent contact holes by using a sequence of steps involving among other things a sacrificial pattern (13 in the figure below) and a conformal hardmask layer (14’) to create an array of vias having a pitch below what is possible by standard lithography:

Fig. 4

References

Limiting references

This place does not cover:

Geometrical aspects relating to "tapered" vias, i.e. vias having a wider part somewhere

H01L 21/76804

H01L 21/76817

{using printing or stamping techniques}

Definition statement

This place covers:

Imprinting or stamping techniques for forming openings in dielectrics.

Methods using a stamp either to pattern a mask, e.g. a resist mask, for forming the opening or to imprint the opening directly into a dielectric
Example:

![Diagram of interconnection structure](image)

**H01L 21/76819**

{Smoothing of the dielectric (planarisation of insulating materials per se
H01L 21/31051)}

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Planarisation of insulating materials per se | H01L 21/31051 |

**H01L 21/76822**

{Modification of the material of dielectric layers, e.g. grading, after-treatment to improve the stability of the layers, to increase their density etc.}

**Definition statement**

This place covers:

All aspects related to forming or after-treatment steps which lead to a modification of the material of a dielectric layer within an interconnection structure.

Manufacture of "graded" dielectric layers having a varying composition throughout its thickness, no matter if said grading is achieved by a modified deposition process or an after-treatment.

Examples:

Graded dielectric layer: density and permittivity characteristics vary uniformly from a top portion to a bottom portion of the layer. The variation is achieved through varying deposition parameters such as
flow rate of constituent process gases or deposition chamber pressure, or through a post deposition treatment, such as plasma treatment or curing:

The surface of the PSG layer 704 is made hydrophilic by a "scrubbing treatment" 710:

**Special rules of classification**

It is not important whether the various treatment steps are conducted on a "main" interlevel or intralevel dielectric or on a "thin functional dielectric layer" as defined in H01L 21/76829 and subgroups.

If the treatment involves a patterned layer including an opening, the group H01L 21/76814 should also be given.

**H01L 21/76823**

{transforming an insulating layer into a conductive layer}

**Definition statement**

*This place covers:*

Processes designed for rendering a dielectric layer of an interconnect stack conductive

Examples:
A diamond etch-stop layer (66 in the figure below) is rendered conductive by implanting Ti followed by thermal treatment.

Special rules of classification
A document classified in this group is additionally classified in H01L 21/76822 and subgroups thereof, whenever appropriate, the method of conversion involves a plasma treatment, or an ion implantation.

H01L 21/76825
{by exposing the layer to particle radiation, e.g. ion implantation, irradiation with UV light or electrons etc. (plasma treatment H01L 21/76826)}

Definition statement
This place covers:
After-treatment or post-treatment process of dielectric layers of the interconnect stack involving particle radiation, e.g. removal of moisture etc. by UV or e-beam radiation, processes for modifying the dielectric constant of the layer, introduction of dopants into the dielectric by particle irradiation.

Examples:
A layer of silane is deposited onto a polymer dielectric layer 16. This layer is then exposed to UV light to initiate polymerization of the silane molecules to form an adhesion promoter layer 18 (or an etch stop or hard mask layer), and to react the adhesion promoter layer with low dielectric constant polymer layer 16:
The upper surface of the porous MSQ film 105 is treated by electron beam irradiation or by UV irradiation to reinforce the upper portion in the film 105:

**References**

**Limiting references**

_This place does not cover:_

| Removal of porogens for manufacturing porous dielectrics | H01L 21/7682 |
| Plasma treatment | H01L 21/76826 |

**Special rules of classification**

If the treatment is performed to form or modify a "thin functional" dielectric layer, e.g. an etch stop, one of the groups H01L 21/76829 is additionally assigned.

Curing of a dielectric precursor material is generally not considered an "after-treatment" but characterizes the formation of the dielectric layer per se, covered by H01L 21/02348.

**H01L 21/76826**

*(by contacting the layer with gases, liquids or plasmas)*

**Definition statement**

_This place covers:_

Processes involving contacting a dielectric of an interconnect stack with gases, liquids or plasmas in order to modify the internal structure and/or properties of the dielectric, e.g. nitridation, removal of organic groups from the layer, introduction of dopants into the dielectric using gases, liquids or plasmas.

Examples:
a low-k dielectric is treated in a supercritical fluid after deposition, after via etching, to improve mechanical strength or repair plasma damage:

Plasma treatment 130 is carried out in order to decrease the C- or F- concentration in an upper layer 120a of the ILD 120:

Plasma treatment is carried out in order to modify the sidewalls of a damascene opening 218:
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Supercritical fluid treatment after a via hole formation</th>
<th>H01L 21/76814</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plasma treatment is carried out to form a modified sidewall layer in an opening</td>
<td>H01L 21/76831</td>
</tr>
</tbody>
</table>

Special rules of classification

If the plasma treatment is carried out to form a modified sidewall layer in an opening, the group symbol H01L 21/76831 must also be assigned.

H01L 21/76828

{thermal treatment}

Definition statement

This place covers:

Thermal treatment for modifying the internal structure and/or properties of the dielectric of an interconnect stack, e.g. removal of moisture.

Example:

After completion of the deposition, the low-k dielectric layer 206 is subjected to a heat treatment in a nitrogen-free atmosphere to promote the out-gassing of the volatile materials 220 and especially of nitrogen and nitrogen compounds:

US2004121265

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Plasma annealing | H01L 21/76826 |

Special rules of classification

If the heat treatment is carried out in reactive atmospheres, i.e. inevitably involves modification of the dielectric material by e.g. introducing a further chemical element into the layer, e.g. plasma annealing, the group symbol H01L 21/76826 is additionally assigned.
**H01L 21/76829**

{characterised by the formation of thin functional dielectric layers, e.g. dielectric etch-stop, barrier, capping or liner layers}

**Definition statement**

*This place covers:*

All aspects related to the formation and the geometry of so-called "thin functional dielectric layers", e.g. etch-stop films or dielectric barrier or liner layers.

**Examples:**

Fabrication of an oxygen-doped low-k SiC etch-stop layer 230:

![Diagram](image1)

Nitride liner 130 imparts tensile stress in the underlying semiconductor to improve carrier mobility:

![Diagram](image2)

Silicon oxide layer 224 is formed on top of a low-k dielectric. Layer 224 serves as a sacrificial cap layer:

![Diagram](image3)
Special rules of classification

If a document dealing with a thin functional dielectric layer also contains after-treatment aspects as defined in H01L 21/76822+, one (or more) of the latter groups should also be assigned to this document.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

"Thin" layer as used herein means thin compared with the "main" interlevel or intralevel dielectric. In cases of doubt as to whether the layer is "thin" in the above sense, the criterion "functional layer" takes precedence, i.e. documents relating to layers, which may not exactly be "thin" in the above sense but serve some particular purpose except from merely isolating conductors, should also be classified here.

H01L 21/76831

{in via holes or trenches, e.g. non-conductive sidewall liners}

Definition statement

This place covers:

Sidewall layers that are formed by direct deposition

Sidewall liners obtained by treatment of the sidewalls of the opening.

Examples:

Sidewalls of a porous dielectric are plasma-treated in order to form a carbon sealing layer 24 on via sidewalls 22:

Non-metallic layer 15, e.g. silicon carbide or boron carbide is deposited in a dual damascene opening and etched back to form sidewall spacers 19:
Special rules of classification

If the treatment has characteristics relating to any of the groups H01L 21/7682+, one (or more) of the latter groups should also be assigned.

H01L 21/7683

{Multiple layers}

Definition statement

This place covers:

Stacks of two or more thin "functional" dielectric layers, e.g. multiple etch stop layers, multiple trench liners.

Examples:

Composite adhesion/etch-stop multilayer (SiC layer 104 and SiOC layer 106) is formed; layer 104 is for improving adhesion between layers 100 and 106:

![FIG. 2](image)

Multiple dielectric capping layers 616/622 and 620/624 are formed by gas cluster ion beam "infusion":

![Image](image)

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

"multiple"  two or more layers in direct contact with each other.
H01L 21/76834

{formation of thin insulating films on the sidewalls or on top of conductors (H01L 21/76831 takes precedence)}

Definition statement

This place covers:

Insulating film covering some part of the conductor regardless of whether the conductor is “free-standing” or an inlaid conductor.

Example:

Dielectric film 107 covers the top and part of the sidewalls of inlaid conductors 105:

Temporary sacrificial encapsulation layer (206 in fig. 5, 306 in fig. 6) is formed in a dual damascene opening and covering an exposed underlying conductor in order to form a protective layer for subsequent cleaning steps:

FIG. 5

FIG. 6
References

Limiting references

This place does not cover:

| Dielectric sidewall liners in openings | H01L 21/76831 |

H01L 21/76835

{Combinations of two or more different dielectric layers having a low dielectric constant (H01L 21/76832 takes precedence)}

Definition statement

This place covers:

Dielectric layer stacks in which e.g. the via-level dielectric and the trench-level dielectric comprise different low-k materials or in which e.g. the structure contains a low-k etch-stop or adhesion layer separating two dielectrics of which at least one must be a low-k dielectric.

Examples:

Trench-level dielectric (spin-on low-k dielectric 24) and via-level dielectric (CVD SiOC layer 10) are different low-k materials:

![Diagram](US2005130407)

Via-level and trench-level dielectrics (204 and 212) are made of the same low-k material, but the etch-stop layer 206 is made of a different low-k material:

![Diagram](US2005263876)
Posts (40) are made of a non-porous low-k dielectric whereas the material filling the spaces between the posts is a porous low-k dielectric:

References

Limiting references

This place does not cover:

Middle etch-stop layer being a multilayer system

H01L 21/76832

H01L 21/76837

{Filling up the space between adjacent conductive structures; Gap-filling properties of dielectrics}

Definition statement

This place covers:

Special measures for improving the gap-filling properties of a dielectric, wherein said "gap" is formed between conductive structures. The term "gap" is also intended to include vertical gaps.

Example:

a first dielectric (213) is deposited over conductive structures 207 and etched back (the figure above shows the layer 213 after etch-back) so as to partially fill the gap and reduce its aspect ratio, a second dielectric (217) fills the remaining gap.
H01L 21/76838
{characterised by the formation and the after-treatment of the conductors (etching for patterning the conductors H01L 21/3213)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| When the interconnect is also used as the conductor part of a conductor-insulator-semiconductor electrode (gate level interconnections) | H01L 21/28026 |
| Etching for patterning conductors | H01L 21/3213 |

Special rules of classification

Information peculiar to single-step processes should also be classified in the corresponding group, e.g.

- H01L 21/02041 for cleaning
- H01L 21/02697, H01L 212/283 - H01L 21/288 and H01L 21/3105 for the formation of conductive layers,
- H01L 21/3213 for etching,
- H01L 21/027, H01L 21/033, H01L 21/3213 for masking,
- H01L 21/321 for planarising, etc.

H01L 21/76843
{formed in openings in a dielectric}

Definition statement

This place covers:

Thin conductive film being formed in an opening in a dielectric, e.g. barrier, adhesion, nucleation, seed or liner layers.

Example:

a barrier layer comprising e.g. Ru, Ir etc. or one of their (conducting) oxides is deposited in a trench or a dual damascene opening:
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Thin films serving as seed layer for electroplating | H01L 21/76873 |

Special rules of classification

All documents dealing with the formation of thin conductive films in openings should be classified in this group or one of its subgroups even if the fact that the thin film is formed in an opening is not an important aspect of the disclosure under consideration.

If the deposition method of the thin functional layer is disclosed in some detail (PVD, CVD, ALD, plating etc.), the corresponding groups H01L 21/28512 - H01L 21/2885 should also be assigned.

H01L 21/76844

{Bottomless liners}

Definition statement

This place covers:

At least one of the conductive thin films in the opening does not cover the bottom of the opening in its entirety, i.e. even when the thin film is removed from only a part of the bottom of the openings.

Examples:

a set of conductive barrier layers is deposited over the sidewalls of a porous dielectric and subsequently removed from the via floor by sputtering:

![FIG. 27](US6528409)

Barrier layers covering only part of the sidewalls:

![FIG. 4C](US2006246699)
Multiple liner layers (30, 31, 33, 35) are deposited in a via of which only the outermost layers (30, 31) are removed from the via bottom:

**FIG. 1i**

**H01L 21/76846**

{Layer combinations}

**Definition statement**

*This place covers:*

Layer combinations, i.e. arrangements of more than one layer, in the openings, e.g. combinations of particular materials other than the "standard" barrier combinations Ti/TiN, TaN/Ta or W/WN.

Superlattices comprising a multitude of layers comprising "standard" materials (Ti/TiN, TaN/Ta or W/ WN), e.g. a TaN/Ta/TaN/Ta... superlattice.

Graded layers, e.g. a stack of infinitely thin multiple layers with varying composition.

Conductive thin film having a graded composition

Layer combinations formed on top of an inlaid conductor

In these cases the thin film is still considered as being formed "in an opening of a dielectric", see the further explanation and example (i) under point 1.4 below).

Examples:

43 is a TaN layer, 44 is a TaN layer having a graded content of N, 45 is an alpha-Ta layer:
TaN/W/TaN/W/... nanolaminates, fabricated by ALD:

TaN/Ta/TaN/Ta stack:

Different barrier materials on the sidewalls and on the bottom of the via hole (α-phase Ta layer 24 is provided on the via bottom, while the sidewalls are covered with a β-phase Ta layer 29):

**H01L 21/76847**

{the layer being positioned within the main fill metal}

**Definition statement**

This place covers:

Conductive thin film formed within the "main" conductor filling the opening or where the opening is filled by a sequence of thin films. It is important, however, that said thin film does not comprise the same material as the main fill material.

Examples:
Barrier layer 54s, 54d separates two layers of fill metal:

Trench filled by alternating layers 322, 324, comprising e.g. Co and Ni:

References

Limiting references

This place does not cover:

Multistep plating forming a sequence of thin Cu films

H01L 21/76847 (continued)
Cap layer 30 (CoWP layer) comprises multiple layers having periodic variations in the concentration of chemical elements:

Electromigration barrier formed by depositing a metal layer 11, diffusing the metal into the underlying conductor and removing the remainder of layer 11:

**Definition statement**

This place covers:

Thin functional conductive films covering interconnects not formed in an opening of a dielectric, e.g. on subtractive metal lines, e.g. a Ti/TiN adhesion/barrier stack on Al wiring.

Example:
Formation of a TiN layer (141) on an Al conductor (110). The method of fabrication avoids the formation of an unintentional Ti layer (140):
Examples:

**H01L 21/76853**

{characterized by particular after-treatment steps}

**Definition statement**

*This place covers:*

Conductive thin film treated in some way after it has been deposited. The resulting film must still be a conductive film.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Methods of formation of barrier layers other than PVD, CVD or deposition from a liquids</th>
<th>H01L 21/76867</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modifying permanently or temporarily the pattern or the conductivity of conductive members, e.g. formation of alloys, reduction of contact resistances</td>
<td>H01L 21/76886</td>
</tr>
</tbody>
</table>
H01L 21/76855

{After-treatment introducing at least one additional element into the layer}

Definition statement

This place covers:

All methods introducing a new chemical element into the thin film, e.g. the reaction of the layer with the semiconductor substrate to form a silicide.

Example:

A titanium layer (black circles in the figure below) is deposited on the sidewalls of a dielectric layer, the Ti layer reacts with the oxygen (cross-hatched circles) contained in the dielectric during a later thermal step:

![Diagram of a titanium layer reacting with oxygen](US2006214305)

H01L 21/76856

{by treatment in plasmas or gaseous environments, e.g. nitriding a refractory metal liner}

Definition statement

This place covers:

Contacting the thin film with a gas or a plasma so as to modify the composition of the layer, e.g. plasma nitriding.

Examples:

Refractive metal cap layer 303 is plasma nitrided to form a refractive metal nitride layer 305:

![Diagram showing a refractive metal cap layer](US6844258)
Ru barrier layer 650b and a seed layer 666 are deposited in a trench, the seed layer is partially oxidized by exposing it to an oxidizing ambient. The oxide layer 667 serves as a protective layer and is dissolved when contacted with a plating bath:

![Diagram of Ru barrier layer and seed layer](image)

**H01L 21/76858**

**(by diffusing alloying elements)**

**Definition statement**

*This place covers:*

Introducing alloying elements, i.e. metallic elements, by diffusion into or reaction with pre-fabricated conductive thin film into.

**Examples:**

A barrier layer, an adhesion layer (Ti), a seed layer and a Cu fill are formed in a dual damascene opening; after planarisation, a thermal treatment is carried out to react the adhesion layer with the Cu thereby forming an interface layer having a graded Cu content:
Conductive thin film 608 (Ca film) is formed over an inlaid Cu line (601) and heat treatment is performed to diffuse Cu from the line into the Ca layer thereby forming a CuCa capping layer (606). The unreacted material of layer 608 is subsequently removed:

References

Limiting references

This place does not cover:

Layers itself being fabricated by the diffusion of alloying elements

Special rules of classification

Diffusion is a bi-directional process, i.e. there can be cases where it cannot be unambiguously determined whether the final layer is the result of diffusing elements into the layer (which would constitute an example for the present class) or if the final film is the result of diffusing elements out of an original thin film, e.g. into the bulk conductor (this would pertain to H01L 21/76867, see the examples given there). In such cases both classes H01L 21/76858 and H01L 21/76867 should be assigned.

H01L 21/76859

{by ion implantation}

Definition statement

This place covers:
Implantation methods, i.e. methods allowing for precise control of the energy of the implanted ions as well as of the implantation depth.

Examples:
Sn ions are implanted into barrier layer (440) in order to render the barrier amorphous and to introduce dopants having favourable electromigration properties:

the surface of a CoWP capping layer (34) is nitrided by N2 ion implantation:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Implantation in semiconductors</th>
<th>H01L 21/265</th>
</tr>
</thead>
<tbody>
<tr>
<td>implantation in insulating layers</td>
<td>H01L 21/3105 or H01L 21/3115</td>
</tr>
</tbody>
</table>

H01L 21/76861

{Post-treatment or after-treatment not introducing additional chemical elements into the layer}

Definition statement

This place covers:
Methods for removing contaminants, e.g. oxides, from thin functional conductive films.
Methods for transforming their grain structure.

Example:
Oxides and other contaminants of a Cu seed layer (144) are removed by a wet-chemical treatment:

H01L 21/76862

{Bombardment with particles, e.g. treatment in noble gas plasmas; UV irradiation}

Definition statement

This place covers:

Contacting the film with plasmas or particles, e.g. high energy photons, while not introducing a new element into the film, e.g. treatment by UV irradiation for the removal of oxides.

Examples:

Barrier layer (Ti/TiN layer 118) is plasma treated to roughen the surface of the layer in the region 120. As a result, the number of nucleation sites is increased which slows down the growth of W layer 124:

Barrier layer (52) is subjected to a two-step redistribution process, i.e. overhanging portions (60) are removed and redistributed to reinforce sidewall regions (32, 34) where the PVD barrier is not
thick enough. In a first step, this redistribution is achieved by bombardment with Ar and Ta ions with simultaneous deposition of Ta, in the second step, only Ar is used for material redistribution:

**Figure 2D**

**H01L 21/76864**

**{Thermal treatment}**

**Definition statement**

*This place covers:*

Thermal treatment of thin functional films not introducing additional elements into the film, e.g. plasma annealing

**Examples:**

a Cu seed layer (228) is locally heat treated in order to induce grain growth in the seed layer:

**FIG. 2a**

a Ru barrier/seed layer (108) is annealed after deposition to remove oxides or other contaminants prior to plating:
References

Limiting references

This place does not cover:

| Film stacks, e.g. Ti/TiN and W, TaN/Ta and Cu, subjected to annealing after filling the contact hole | H01L 21/76877 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Seed layers treated by an annealing step | H01L 21/76873 |

Special rules of classification

"Plasma annealing" should be classified here and in H01L 21/76862.

Note that for assigning this group symbol it is important that it is the thin film per se which is subjected to the thermal treatment. Thermal treatment of the main conductor is classified in H01L 21/76838 or, if the main conductor is formed in an opening in a dielectric, in H01L 21/76883.

Thermal treatments for driving an alloying element into the thin metal film are not classified here but in H01L 21/76858.

H01L 21/76865

{Selective removal of parts of the layer (H01L 21/76844 takes precedence)}

Definition statement

This place covers:

Removal of overhanging or "necking" portions of conductive thin films at the upper regions of via holes, or all cases where sputter etching and sputter deposition are carried out simultaneously.

Examples:

Seed layer (10) is removed so as to provide a base layer for selective filling of the dual damascene trench;
Overhanging portions of a barrier layer 308 and/or a Cu seed layer (310) are removed and redistributed by gas cluster ion beam (GCIB) processing:

Capping layer (106) on an underlying conductor (105) is partially etched off by sputtering; the sputtered material of barrier (106) is redistributed on the via sidewalls to form a bottomless first barrier:

References

Limiting references
This place does not cover:

Forming a bottomless barrier

Informative references
Attention is drawn to the following places, which may be of interest for search:

Selective removal of a seed layer for electroplating
H01L 21/76867

{characterized by methods of formation other than PVD, CVD or deposition from a liquids (PVD H01L 21/2855; CVD H01L 21/28556; deposition from liquids H01L 21/288)}

**Definition statement**

*This place covers:*

Formation of a functional conductive thin film, e.g. barrier, liner, adhesion or seed layers, by diffusing alloying elements such that they segregate at the surfaces of a conductor.

Diffusion of material from an initial thin film into a surface portion of the conductor, optionally followed by the removal of said initial thin film.

**Examples:**

A layer stack comprising a first barrier layer (6) and a metal layer (Hf, Zr, or Ti) suitable for forming an intermetallic compound with Cu is deposited in a dual damascene trench. A heat treatment forms layer (10b) comprising a compound of Cu and Hf, Zr, or Ti, while at the same time another compound layer (10a) is formed within the main conductor by diffusion of Hf, Zr, or Ti:

Barrier layer sections 6a, 6b are formed by diffusing material of the barrier layer 510 into the porous dielectric 2:

![Diagram](image)
Al from Al layer 22 is diffused into inlaid Cu in order to form a CuAl electromigration barrier 12; the remaining unreacted Al layer is removed:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Method</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVD</td>
<td>H01L 21/2855</td>
</tr>
<tr>
<td>CVD</td>
<td>H01L 21/28556</td>
</tr>
<tr>
<td>Deposition from liquids</td>
<td>H01L 21/288</td>
</tr>
</tbody>
</table>

H01L 21/76868

{Forming or treating discontinuous thin films, e.g. repair, enhancement or reinforcement of discontinuous thin films}

Definition statement

This place covers:

Methods specially adapted for either forming a discontinuous thin functional conductive film or for treating a discontinuous film so as to make it continuous, e.g. repair of seed layers.

Example:

Ti layer 126 is formed only incompletely on the sidewalls of contact hole 124; the TiSix layer 132 repairs the discontinuities in layer 126:
H01L 21/7687
{Thin films associated with contacts of capacitors}

**Definition statement**

*This place covers:*

Thin conductive films formed in conjunction with the manufacture of contacts for capacitors

**Example:**
Formation of the barrier layer (13e):

![Diagram of barrier layer formation](image)

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Capacitor electrodes themselves | H01L 28/60 |

**Special rules of classification**

This group is intended to sort of "filter out" all documents related to capacitor contacts providing a solution to the very specific problems encountered during the manufacture of capacitors. The groups H01L 21/76843, H01L 21/7685, H01L 21/76853, H01L 21/76867 should also be given, provided "interesting" aspects which might also be of importance in the context of more conventional barriers are disclosed.

H01L 21/76871

{Layers specifically deposited to enhance or enable the nucleation of further layers, i.e. seed layers}

**Definition statement**

*This place covers:*

Formation of seed, wetting, nucleation or catalyst layers.

**Special rules of classification**

Whenever any one of the structural aspects covered by H01L 21/76843 or H01L 21/7685 applies the corresponding group symbol should be given in addition to the seed layer groups with the only
exception that "layer combinations", i.e. structures containing stacks of seed layers, are not classified in H01L 21/76846.

Whenever any one of the after-treatment or manufacturing aspects covered by H01L 21/76853, H01L 21/76867 or H01L 21/76868 applies the corresponding group should also be given.

Documents related to seed layers are classified in the head group H01L 21/76871 only if it is not clear which deposition method is envisaged or if the corresponding seed layer is suitable for all three of the deposition methods listed below.

H01L 21/76874

{for electroless plating}

Definition statement

This place covers:
Seed layers specifically adapted for facilitating the deposition of conductive films by electroless plating

Examples:
Formation of a Pd catalyst layer for electroless CoWP deposition on top of an inlaid Cu interconnect:

![Diagram of the electroless plating process](EP1496542)
Formation of a Pd catalyst layer for electroless Cu plating (The Pd seed is formed by plasma-immersion ion implantation into a TaN barrier layer):

**FIG. 3B**

Electroless Cu Plating

**FIG. 3C**

Copper

US2006040065

**H01L 21/76879**

{by selective deposition of conductive material in the vias, e.g. selective C.V.D. on semiconductor material, plating (plating on semiconductors in general H01L 21/288)}

**Definition statement**

*This place covers:*

Methods for selectively filling of vias or trenches in a dielectric layer with a conductive material, e.g. bottom up fill of a damascene opening not leading to a metal overburden on the field regions surrounding the opening.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Plating on semiconductors in general | H01L 21/288 |

**Special rules of classification**

If the deposition method is disclosed in some detail and includes one or more of PVD, CVD, ALD or liquid deposition, the corresponding group symbol H01L 21/2855, H01L 21/28556, H01L 21/28562, H01L 21/288 or H01L 21/2885 should also be assigned.
H01L 21/7688
{by deposition over sacrificial masking layer, e.g. lift-off (lift-off per se H01L 21/0272)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Lift-off of resists</th>
<th>H01L 21/0272</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lift-off of other layers</td>
<td>H01L 21/0331</td>
</tr>
</tbody>
</table>

H01L 21/76883
{Post-treatment or after-treatment of the conductive material}

Definition statement
This place covers:
After-treatment for improving or modifying the result of the process of filling an opening in a dielectric layer, e.g. a via hole or a damascene trench, with conductive material. Thermal treatments before or after polishing, e.g. to induce grain growth, removal of metal residues, plasma cleaning

References
Limiting references
This place does not cover:

| Plasma treatment specifically adapted for forming a thin layer on the surface of the conductor | H01L 21/76849, H01L 21/76886 |
| Reflowing the conductor or applying pressure so as to better fill the opening | H01L 21/76882 |
| Oxidation or otherwise rendering (parts of) the conductor non-conductive | H01L 21/76888 |

Special rules of classification
The after-treatment is part of a multi-step process for forming a conductor in an opening in a dielectric. Cleaning of conductors per se is classified in H01L 21/02068 - H01L 21/02074.

H01L 21/76885
{By forming conductive members before deposition of protective insulating material, e.g. pillars, studs}

Definition statement
This place covers:
Conductors formed by through-mask plating
References

Limiting references

This place does not cover:

Formation of pillars, studs, bumps etc. for connecting the semiconductor substrate to other substrates

H01L 24/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Doping

H01L 21/265, H01L 21/38

H01L 21/76886

{Modifying permanently or temporarily the pattern or the conductivity of conductive members, e.g. formation of alloys, reduction of contact resistances}

Definition statement

This place covers:

Methods in which the properties of an otherwise completed conductive member of an interconnect, i.e. the main conductor, are modified, e.g. by introducing dopants into the conductor, alloying the main conductor with another metal

References

Limiting references

This place does not cover:

Smoothing; Planarisation

H01L 21/7684

Modification of thin functional conductive films such as barrier, adhesion, liner or seed layers

H01L 21/7685 -
H01L 21/7686

Processes for fabricating fuses and anti-fuses are classified with the fuses and anti-fuses in

H01L 23/525

H01L 21/76897

{Formation of self-aligned vias or contact plugs, i.e. involving a lithographically uncritical step (self-aligned silicidation on field effect transistors H01L 29/665)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Self aligned silicidation on field effect transistors

H01L 29/66583
**H01L 21/76898**

{formed through a semiconductor substrate}

**Definition statement**

*This place covers:*

Establishing a conductive path extending through the substrate from the top surface to the bottom surface, e.g. through-silicon vias

Example

---

**FIG. 1A**

**FIG. 1B**

**FIG. 1C**

**FIG. 1D**

**FIG. 1E**

**FIG. 1F**

**FIG. 1G**
H01L 21/77
Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in, or on, a common substrate (electrically programmable read-only memories or multistep manufacturing processes therefor H01L 27/115)

Definition statement
This place covers:
In the group range H01L 21/77 - H01L 21/86 are classified processes for integration a plurality of solid state components formed in or on a common substrate, with

- H01L 21/77 and H01L 2021/775 covering the manufacturing of devices consisting of a plurality of solid state components formed or assembles ON a common substrate, e.g. integrated circuits formed of a plurality of chips on a host substrate, and
- H01L 21/82 - H01L 21/86 covering the manufacturing of devices consisting of a plurality of solid state components formed IN a common substrate, e.g. integrated circuits formed of a single chip, and
- H01L 21/78 - H01L 21/786 being reserved to processes for the division of a substrate into a plurality of individual devices.

References

Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multistep methods for manufacturing random access memories [RAM] structures</td>
<td>H01L 27/10844</td>
</tr>
<tr>
<td>Integration processes for the manufacture of devices of the type classified in H01L 27/14 - H01L 27/32</td>
<td>H01L 27/14 - H01L 27/32</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Devices comprising components using organic materials as active part</td>
<td>H01L 21/28</td>
</tr>
<tr>
<td>Devices sensitive to light</td>
<td>H01L 27/14</td>
</tr>
<tr>
<td>Devices adapted to emit light</td>
<td>H01L 27/15</td>
</tr>
<tr>
<td>Devices comprising thermo-electric components</td>
<td>H01L 27/16</td>
</tr>
<tr>
<td>Devices comprising superconductive components</td>
<td>H01L 27/18</td>
</tr>
<tr>
<td>Devices comprising piezo-electric, electro-strictive or magneto-strictive components</td>
<td>H01L 27/20</td>
</tr>
<tr>
<td>Devices comprising magneto-galvanic devices, e.g. Hall effect devices, MRAM</td>
<td>H01L 27/22</td>
</tr>
<tr>
<td>Devices comprising components for rectifying, amplifying or switching without a potential-jump barrier or surface barrier</td>
<td>H01L 27/24</td>
</tr>
<tr>
<td>Devices including bulk negative resistance effects, like Gunn devices</td>
<td>H01L 27/26</td>
</tr>
<tr>
<td>Components specially adapted for sensing light, electromagnetic or corpuscular radiation, or specially adapted for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation</td>
<td>H01L 27/30</td>
</tr>
</tbody>
</table>
Devices with components specially adapted for light emission

**Special rules of classification**

Integration processes for the manufacture of devices of the type classified in H01L 27/14 - H01L 27/32 are not classified in this group and its sub-groups. Instead, as they are peculiar to said devices, they are classified together with the devices.

Multistep processes for manufacturing memory structures in general using field effect technology are covered by H01L 27/1052;

Multistep processes for manufacturing dynamic random access memory structures are covered by H01L 27/10844;

Multistep processes for manufacturing static random access memory structures are covered by H01L 27/11;

Multistep processes for manufacturing read-only memory structures are covered by H01L 27/112;

Multistep processes for manufacturing electrically programmable read-only memory structures are covered by H01L 27/115.

**H01L 2021/775**

{comprising a plurality of TFTs on a non-semiconducting substrate, e.g. driving circuits for AMLCDs}

**Definition statement**

*This place covers:*

Multistep processes for the fabrication of devices comprising a plurality of TFT on an insulating substrate, e.g. for driving LCD displays.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Recrystallization of amorphous or polycrystalline semiconductor layers | H01L 21/02667 |
| LCD displays per se | G02F 1/1362 |

**Special rules of classification**

If a single step among the multistep sequence appears to be particular it should be given a group symbol in the corresponding single step group.

**H01L 21/78**

with subsequent division of the substrate into plural individual devices (cutting to change the surface-physical characteristics or shape of semiconductor bodies H01L 21/304)

**Definition statement**

*This place covers:*

Multistep processes for singulating devices.
References

Limiting references
This place does not cover:

| Devices sensitive to light          | H01L 31/00 |
| Light emitting devices              | H01L 33/00 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Single mechanical steps like cutting semiconductors | H01L 21/304 |
| Laser dicing                                           | B23K 26/00 |
| Single mechanical steps of grinding, lapping and polishing in general | B24B |
| Fine working of crystals, e.g. semiconductors         | B28D 5/00 |

H01L 21/7806
{involving the separation of the active layers from a substrate}

Definition statement
This place covers:
Separation of layers comprising active devices from the substrate, e.g. splitting after Epitaxial Lift-Off

Glossary of terms
In this place, the following terms or expressions are used with the meaning indicated:

| ELO | Epitaxial Lift-Off |

H01L 21/786
the substrate being other than a semiconductor body, e.g. insulating body

Definition statement
This place covers:
Division of the substrate into individual components where the process is peculiar to the insulating body or substrate.

H01L 21/82

to produce devices, e.g. integrated circuits, each consisting of a plurality of components

Definition statement
This place covers:
Multistep processes of integration of devices consisting of a plurality of solid state components formed in a common substrate, i.e. integrated circuits formed of a single chip.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Integrated circuits                          | H01L 27/00 |

Special rules of classification

Within the group range H01L 21/82 - H01L 21/86, a particular aspect linked to the fabrication of several components must appear. When the multistep processes do not show specific aspects linked to the fabrication of several components, e.g. when the integrated circuit is only constituted of a multiplicity of an identical device without further specification, then the process may only be classified with the multistep process for fabrication of this device, e.g. in H01L 29/00. Thus, the mere mention of the fabrication of an integrated circuit, when the fabrication of a device is disclosed, does not require a group symbol in H01L 21/82.

When the fabrication process is specified or peculiar to an electric circuit, only a group symbol in H01L 27/00 is given.

Combination of field effect devices and passive devices is classified in H01L 27/00.

H01L 21/8221

{Three dimensional integrated circuits stacked in different levels}

Definition statement

This place covers:

Three dimensional integrated circuits in a common substrate

References

Limiting references

This place does not cover:

| The fabrication of three-dimensional integrated devices by assembling different devices or substrates | H01L 25/00 |

H01L 21/823487

{with a particular manufacturing method of vertical transistor structures, i.e. with channel vertical to the substrate surface (with a current flow parallel to the substrate surface H01L 21/823431)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| With a current flow parallel to the substrate surface | H01L 21/823431 |
H01L 21/823885
{with a particular manufacturing method of vertical transistor structures, i.e.
with channel vertical to the substrate surface (with a current flow parallel to the
substrate surface H01L 21/823821)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| With a current flow parallel to the substrate surface | H01L 21/823821 |

H01L 21/8239
Memory structures

Definition statement
This place covers:
This group is no longer used for classification of new documents. Subject matter relating to memory
structures is covered by H01L 27/1052.

References
Limiting references
This place does not cover:

| Static random access memory structures | H01L 27/11 |

H01L 22/00
{Testing or measuring during manufacture or treatment; Reliability
measurements, i.e. testing of parts without further processing to modify the
parts as such; Structural arrangements therefor}

Definition statement
This place covers:
Application of testing and/or measuring procedures during the manufacturing processes of devices as
defined under H01L 21/00, with the aim to
- detect defects, repair defects, sort defective devices / wafers
- control the semiconductor device fabrication process,
- with or without corrective action on the process,

which are specific to semiconductor device fabrication, e.g. end point determination.

Covers the measuring of a single parameter or variable

Relationships with other classification places
Processes which are not specific to semiconductor device fabrication or processes, where the
semiconductor devices are included in a larger system, are typically not classified in H01L 22/00, but
are classified in the relevant place for the processes or testing in general, e.g. G01N or G01R.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Method</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detecting parts, counting parts, handling parts</td>
<td>H01L 21/87</td>
</tr>
<tr>
<td>Marks on wafers, test patterns on wafers</td>
<td>H01L 23/544</td>
</tr>
<tr>
<td>Means for detecting end-point in lapping or polishing machines</td>
<td>B24B 37/013</td>
</tr>
<tr>
<td>Analysing materials by determining their chemical or physical properties</td>
<td>G01N</td>
</tr>
<tr>
<td>Optical characterization of semiconductors</td>
<td>G01N 21/9501</td>
</tr>
<tr>
<td>Measuring electrical or magnetic variables</td>
<td>G01R</td>
</tr>
<tr>
<td>Multiple probes for testing, e.g. probe cards</td>
<td>G01R 1/073</td>
</tr>
<tr>
<td>Testing of individual devices, including on wafers, after manufacture</td>
<td>G01R 31/26</td>
</tr>
<tr>
<td>Testing of integrated circuits, including on wafers, after manufacture</td>
<td>G01R 31/28</td>
</tr>
<tr>
<td>Contactless testing of integrated circuits</td>
<td>G01R 31/302</td>
</tr>
<tr>
<td>Testing and controlling photoresist and lithographic patterns</td>
<td>G03F 7/70633</td>
</tr>
<tr>
<td>Multiple probes for testing, e.g. probe cards</td>
<td>G05B 19/418</td>
</tr>
<tr>
<td>Inspection of images, flaw detection</td>
<td>G06T 7/0002</td>
</tr>
<tr>
<td>Testing storing means, like memories, including repair</td>
<td>Q11C 29/00</td>
</tr>
<tr>
<td>Measuring and control of plasma parameters</td>
<td>H01J 37/00, G01N</td>
</tr>
<tr>
<td>Controlling gas-filled discharge tubes, e.g. plasma machines, by</td>
<td>H01J 37/32963</td>
</tr>
<tr>
<td>information coming from substrate; end-point detection</td>
<td></td>
</tr>
<tr>
<td>Testing of photovoltaic systems</td>
<td>H02S 50/00</td>
</tr>
</tbody>
</table>

H01L 22/00 (continued)

Definition statement

This place covers:

Methods for measurement of structural or electrical parameters as part of the device manufacturing process.

Measuring as part of the manufacturing process; the parameter may be for example the thickness of layers, refractive index of layers, line width, warp of wafers, bond strength, defect concentration, metallurgical parameters, diffusion depth, dopant concentration.

Relationships with other classification places

Measurement of parameters wherein the fabrication of semiconductor devices is not particularly relevant to the invention, or wherein the measurement of the parameter could equally be applied to the fabrication of other products than semiconductor products are typically not classified.
References

Limiting references

This place does not cover:

| Procedures, i.e. sequence of activities consisting of a plurality of measurement and correction, marking or sorting steps | H01L 22/20 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Measurement of parameters which is not part of the device fabrication process Measurement of parameters wherein the fabrication of semiconductor devices is not particularly relevant to the invention, and wherein the measurement of the parameter could equally be applied to the fabrication of other products than semiconductor devices | G01N or G01R. |
| Burn-in | G01R 31/2855 |

Special rules of classification

In H01L 22/00, the method for measuring a parameter is classified in H01L 22/20 as soon as it is part of a testing or controlling procedure.

H01L 22/12

{for structural parameters, e.g. thickness, line width, refractive index, temperature, warp, bond strength, defects, optical inspection, electrical measurement of structural dimensions, metallurgic measurement of diffusions (electrical measurement of diffusions H01L 22/14)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Electrical measurement of diffusion regions | H01L 22/14 |

H01L 22/20

{Sequence of activities consisting of a plurality of measurements, corrections, marking or sorting steps}

Definition statement

This place covers:

Multi-step processes comprising at least a measuring step followed by a correcting, marking or sorting step.

References

Limiting references

This place does not cover:

| Semiconductor factory control | G05B 19/418 |
Informative references

Attention is drawn to the following places, which may be of interest for search:

| Procedures applied to semiconductor fabrication but wherein the fabrication of semiconductor devices is not particularly relevant to the invention and wherein the procedure could equally be applied to the fabrication of products other than semiconductor devices | G01N or G01R |

H01L 22/24

{Optical enhancement of defects or not directly visible states, e.g. selective electrolytic deposition, bubbles in liquids, light emission, colour change (voltage contrast G01R 31/311)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Voltage contrast | G01R 31/311 |

H01L 22/26

{Acting in response to an ongoing measurement without interruption of processing, e.g. endpoint detection, in-situ thickness measurement (endpoint detection arrangements in CMP apparatus B24B 37/013, in discharge apparatus H01J 37/32)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| methods for plasma etching end point control | H01J 37/32 |

Special rules of classification

End point process detection, when it is exclusively based on the use of a machine which has been designed for that purpose, need not to be classified in H01L 22/00.
H01L 22/34

{Circuits for electrically characterising or monitoring manufacturing processes, e.g. whole test die, wafers filled with test structures, on-board-devices incorporated on each die, process control monitors or pad structures thereof, devices in scribe line (switching, multiplexing, gating devices G01R 19/25; process control with lithography, e.g. dose control, G03F 7/20; structures for alignment control by optical means G03F 7/7063)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Process control influencing process steps in general, e.g. CD correction by etch or diffusion | H01L 22/20 |
| Switching, multiplexing, gating devices | G01R 19/25 |
| Process control with lithography, e.g. dose control | G03F 7/20 |
| Structures for alignment control by optical means | G03F 9/7073 |

H01L 23/00

Details of semiconductor or other solid state devices (H01L 25/00 takes precedence {; structural arrangements for testing or measuring during manufacture or treatment, or for reliability measurements H01L 22/00; arrangements for connecting or disconnecting semiconductor or solid-state bodies, or methods related thereto H01L 24/00; finger print sensors G06K 9/0006})

Definition statement

This place covers:

- Details of semiconductor or other solid state devices including
- Structural arrangements for protection of semiconductor or other solid state devices against mechanical damage or moisture
- Containers or seals
- Mountings
- Fillings or auxiliary members in containers of encapsulations
- Encapsulations
- Holders for supporting the complete device in operation
- Arrangements for cooling, heating, ventilating or temperature compensation
- Arrangements for conducting electric current to or from the solid state body in operation
- Arrangements for conducting electric current within the solid state body in operation
- Marks applied to semiconductor or other solid state devices
- Protection against radiation of semiconductor or other solid state devices
- Structural electrical arrangements for semiconductor or other solid state devices not otherwise provided for
### References

#### Limiting references

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arrangements for connecting or disconnecting semiconductor or solid-state bodies, and methods related thereto</td>
<td>H01L 24/00</td>
</tr>
<tr>
<td>Assemblies consisting of a plurality of individual semiconductor or other solid state devices</td>
<td>H01L 25/00</td>
</tr>
<tr>
<td>Details of semiconductor devices adapted for rectifying, amplifying, oscillating or switching, or capacitors or resistors with at least one potential-jump barrier or surface barrier</td>
<td>H01L 29/00</td>
</tr>
<tr>
<td>Details peculiar to semiconductor devices sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation</td>
<td>H01L 31/00</td>
</tr>
<tr>
<td>Details peculiar to semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission</td>
<td>H01L 33/00</td>
</tr>
<tr>
<td>Details peculiar to thermo-electric devices comprising a junction of dissimilar materials</td>
<td>H01L 35/00</td>
</tr>
<tr>
<td>Details peculiar to thermoelectric devices without a junction of dissimilar materials</td>
<td>H01L 37/00</td>
</tr>
<tr>
<td>Details peculiar to devices using superconductivity</td>
<td>H01L 39/00</td>
</tr>
<tr>
<td>Details peculiar to piezo-electric devices; electrostrictive devices; magnetostrictive devices</td>
<td>H01L 41/00</td>
</tr>
<tr>
<td>Details peculiar to devices using galvano-magnetic or similar magnetic effects</td>
<td>H01L 43/00</td>
</tr>
<tr>
<td>Details peculiar to solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier</td>
<td>H01L 45/00</td>
</tr>
<tr>
<td>Details peculiar to bulk negative resistance effect devices</td>
<td>H01L 47/00</td>
</tr>
<tr>
<td>Details peculiar to solid state devices not provided for in groups H01L 27/00 - H01L 47/00 and H01L 51/00 and not provided for in any other subclass</td>
<td>H01L 49/00</td>
</tr>
<tr>
<td>Solid state devices using organic materials as the active part, or using a combination of organic materials with other materials as the active part</td>
<td>H01L 51/00</td>
</tr>
<tr>
<td>Microstructural devices or systems, e.g. micromechanical devices</td>
<td>B81B</td>
</tr>
</tbody>
</table>

#### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shape of semiconductor body</td>
<td>H01L 29/0657</td>
</tr>
<tr>
<td>Device electrodes</td>
<td>H01L 29/40</td>
</tr>
<tr>
<td>Non-electric welding by applying impact or other pressure, with or without the application of heat, e.g. cladding or plating</td>
<td>B23K 20/00</td>
</tr>
<tr>
<td>Laser working of semiconductors</td>
<td>B23K 26/0006, B23K 2101/40, B23K 2103/56</td>
</tr>
</tbody>
</table>
Rods, electrodes, materials, or media, for use in soldering, welding, or cutting
Injection moulding of electrical components
Optical interconnections, e.g. light guides
Photolithography
Record carriers for use with machines and containing semiconductor elements (credit cards, id cards)
Structure or manufacture of flux-sensitive heads using magneto-resistive devices or effects
Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor
Apparatus or processes specially adapted for manufacturing, assembling, maintaining, or repairing of line connectors or current connectors or for joining electric conductors (soldering / welding)

Special rules of classification
The use of Indexing Codes of the indexing scheme H01L 23/00 - H01L 23/66 is mandatory for additional information.

Glossary of terms
In this place, the following terms or expressions are used with the meaning indicated:

<table>
<thead>
<tr>
<th>Parts</th>
<th>All structural units which are included in a complete device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Container</td>
<td>Enclosure forming part of the complete device and is essentially a solid construction in which the body of the device is placed, or which is formed around the body without forming an intimate layer thereon. Generally comprises a base, a lid and leads for electrical connection</td>
</tr>
<tr>
<td>Encapsulation</td>
<td>Enclosure which consists of one or more layers formed on the body and in intimate contact therewith</td>
</tr>
</tbody>
</table>

H01L 23/02
Containers; Seals (H01L 23/12, H01L 23/34, H01L 23/48, H01L 23/552, {H01L 23/66} take precedence; {for memories G11C})

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Mountings</th>
<th>H01L 23/12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arrangements for cooling, heating, ventilating or temperature compensation</td>
<td>H01L 23/34</td>
</tr>
<tr>
<td>Arrangements for conducting electric current to or from the solid state body in operation</td>
<td>H01L 23/48</td>
</tr>
<tr>
<td>Protection against radiation</td>
<td>H01L 23/552</td>
</tr>
<tr>
<td>High-frequency adaptations</td>
<td>H01L 23/66</td>
</tr>
</tbody>
</table>
Containers for imagers, i.e. semiconductor components sensitive to radiation

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Housings for MEMs</th>
<th>B81B 7/0032</th>
</tr>
</thead>
<tbody>
<tr>
<td>Housings for sensors in general</td>
<td>G01D 11/24</td>
</tr>
<tr>
<td>Housings for acceleration sensors</td>
<td>G01P 15/0802</td>
</tr>
<tr>
<td>Housings for computers</td>
<td>G06F 1/16</td>
</tr>
<tr>
<td>Housings for record carriers, e.g. memory cards</td>
<td>G06K 19/077</td>
</tr>
<tr>
<td>Housings for memories</td>
<td>G11C 5/04</td>
</tr>
</tbody>
</table>

H01L 23/055
the leads having a passage through the base *(H01L 23/057 takes precedence)*

References
Limiting references
This place does not cover:

| The leads being parallel to the base | H01L 23/057 |

H01L 23/12
Mountings, e.g. non-detachable insulating substrates

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Chip carriers per se</th>
<th>H01L 23/498</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-chip modules in general</td>
<td>H01L 25/00</td>
</tr>
<tr>
<td>Printed circuit boards</td>
<td>H05K 1/00</td>
</tr>
</tbody>
</table>

H01L 23/147
{Semiconductor insulating substrates (semiconductor conductive substrates H01L 23/4926)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Semiconductor conductive substrates | H01L 23/4926 |
**H01L 23/16**

Fillings or auxiliary members in containers (or encapsulations), e.g. centering rings (H01L 23/42, H01L 23/552 take precedence)

**Definition statement**

*This place covers:*

Additional parts and fillings within container or encapsulation, e.g. stiffeners, spacing layers.

**References**

*Limiting references*

*This place does not cover:*

| Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling | H01L 23/42 |
| Protection against radiation | H01L 23/552 |

**H01L 23/20**

gaseous at the normal operating temperature of the device

**References**

*Limiting references*

*This place does not cover:*

| Materials for absorbing or reacting with moisture or other undesired substances | H01L 23/26 |

**H01L 23/22**

liquid at the normal operating temperature of the device

**References**

*Limiting references*

*This place does not cover:*

| Materials for absorbing or reacting with moisture or other undesired substances | H01L 23/26 |
H01L 23/24

solid or gel at the normal operating temperature of the device {{H01L 23/3135 takes precedence}}

References

Limiting references

This place does not cover:

| Materials for absorbing or reacting with moisture or other undesired substances | H01L 23/26 |
| Double encapsulation or coating and encapsulation | H01L 23/3135 |

H01L 23/28

Encapsulations, e.g. encapsulating layers, coatings, {e.g. for protection}  
(H01L 23/552 takes precedence; {insulating layers for contacts or interconnections H01L 23/5329})

References

Limiting references

This place does not cover:

| Protection against radiation | H01L 23/552 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Insulating layers for contacts or interconnections | H01L 23/5329 |

H01L 23/295

{containing a filler (H01L 23/296 takes precedence)}

References

Limiting references

This place does not cover:

| Organo-silicon compounds | H01L 23/296 |
H01L 23/3157
{Partial encapsulation or coating (mask layer used as insulation layer H01L 21/31)}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Mask layer used as insulation layer | H01L 21/31 |

H01L 23/3178
{Coating or filling in grooves made in the semiconductor body}

References

Limiting references
This place does not cover:

| Fillings of grooves in memory cells (e.g. capacitors of RAMs) | H01L 27/108 |

H01L 23/32

Holders for supporting the complete device in operation, i.e. detachable fixtures (H01L 23/40 takes precedence; connectors, {e.g. sockets}, in general H01R; for printed circuits H05K)

References

Limiting references
This place does not cover:

| Mountings or securing means for detachable cooling or heating arrangements | H01L 23/40 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Connectors, e.g. sockets, in general | H01R |
| For printed circuits | H05K |
H01L 23/34
Arrangements for cooling, heating, ventilating or temperature compensation {; Temperature sensing arrangements (thermal treatment apparatus H01L 21/00)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Thermal treatment apparatus</th>
<th>H01L 21/67098</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature control of computers</td>
<td>G06F 1/20</td>
</tr>
<tr>
<td>Thermal control of PCBs</td>
<td>H05K 1/0201</td>
</tr>
</tbody>
</table>

H01L 23/36
Selection of materials, or shaping, to facilitate cooling or heating, e.g. heatsinks {(H01L 23/28, H01L 23/40, H01L 23/42, H01L 23/44, H01L 23/46 take precedence; heating H01L 23/345)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Encapsulations</th>
<th>H01L 23/28</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mountings or securing means for detachable cooling or heating arrangements</td>
<td>H01L 23/40</td>
</tr>
<tr>
<td>Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling</td>
<td>H01L 23/42</td>
</tr>
<tr>
<td>The complete device being wholly immersed in a fluid other than air</td>
<td>H01L 23/44</td>
</tr>
<tr>
<td>Involving the transfer of heat by flowing fluids</td>
<td>H01L 23/46</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Arrangements for heating</th>
<th>H01L 23/345</th>
</tr>
</thead>
</table>

H01L 23/367
Cooling facilitated by shape of device {(H01L 23/38, H01L 23/40, H01L 23/42, H01L 23/44, H01L 23/46 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Cooling arrangements using the Peltier effect</th>
<th>H01L 23/38</th>
</tr>
</thead>
</table>
Mountings or securing means for detachable cooling or heating arrangements

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC (Class)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling</td>
<td>H01L 23/42</td>
</tr>
<tr>
<td>Cooling arrangements with the complete device being wholly immersed in a fluid other than air</td>
<td>H01L 23/44</td>
</tr>
<tr>
<td>Cooling arrangements involving the transfer of heat by flowing fluids</td>
<td>H01L 23/46</td>
</tr>
</tbody>
</table>

**H01L 23/3672**

{Foil-like cooling fins or heat sinks (being part of lead-frames H01L 23/49568)}

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC (Class)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heat sinks being part of lead-frames</td>
<td>H01L 23/49568</td>
</tr>
</tbody>
</table>

**H01L 23/3731**

{Ceramic materials or glass (H01L 23/3732, H01L 23/3733, H01L 23/3735, H01L 23/3737, H01L 23/3738 take precedence)}

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC (Class)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cooling facilitated by selection of materials: diamonds</td>
<td>H01L 23/3732</td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: having a heterogeneous or anisotropic structure</td>
<td>H01L 23/3733</td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: laminates or multilayers</td>
<td>H01L 23/3735</td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: organic materials with or without a thermoconductive filler</td>
<td>H01L 23/3737</td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: semiconductor materials</td>
<td>H01L 23/3738</td>
</tr>
</tbody>
</table>

**H01L 23/3732**

{Diamonds}

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC (Class)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diamond per se</td>
<td>C30B 29/04</td>
</tr>
</tbody>
</table>
H01L 23/3733
{having a heterogeneous or anisotropic structure, e.g. powder or fibres in a matrix, wire mesh, porous structures (H01L 23/3732, H01L 23/3737 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>H01L 23/3732</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cooling facilitated by selection of materials: diamonds</td>
<td></td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: organic materials with or</td>
<td></td>
</tr>
<tr>
<td>without a thermoconductive filler</td>
<td></td>
</tr>
</tbody>
</table>

H01L 23/3736
{Metallic materials (H01L 23/3732, H01L 23/3733, H01L 23/3735, H01L 23/3737, H01L 23/3738 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>H01L 23/3732</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cooling facilitated by selection of materials: diamonds</td>
<td></td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: having a heterogeneous or</td>
<td></td>
</tr>
<tr>
<td>anisotropic structure</td>
<td></td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: laminates or multilayers</td>
<td></td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: organic materials with or</td>
<td></td>
</tr>
<tr>
<td>without a thermoconductive filler</td>
<td></td>
</tr>
<tr>
<td>Cooling facilitated by selection of materials: semiconductor materials</td>
<td></td>
</tr>
</tbody>
</table>

H01L 23/4012
{for stacked arrangements of a plurality of semiconductor devices (assemblies per se H01L 25/00)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>H01L 25/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assemblies consisting of a plurality of individual semiconductor or other</td>
<td></td>
</tr>
<tr>
<td>solid-state bodies</td>
<td></td>
</tr>
</tbody>
</table>
H01L 23/42
Fillings or auxiliary members in containers {or encapsulations} selected or arranged to facilitate heating or cooling {{heating H01L 23/345} ; characterised by selection of materials for the device H01L 23/373}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Heating</th>
<th>H01L 23/345</th>
</tr>
</thead>
<tbody>
<tr>
<td>Selection of materials for the device</td>
<td>H01L 23/373</td>
</tr>
</tbody>
</table>

H01L 23/427
Cooling by change of state, e.g. use of heat pipes {{by liquefied gas H01L 23/445}}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Cooling by liquefied gas</th>
<th>H01L 23/445</th>
</tr>
</thead>
</table>

H01L 23/4334
{Auxiliary members in encapsulations (H01L 23/49568 takes precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Leadframes specifically adapted to facilitate heat dissipation</th>
<th>H01L 23/49568</th>
</tr>
</thead>
</table>

H01L 23/44
the complete device being wholly immersed in a fluid other than air {{H01L 23/427 takes precedence}}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Cooling by change of state</th>
<th>H01L 23/427</th>
</tr>
</thead>
</table>
H01L 23/46

involving the transfer of heat by flowing fluids (H01L 23/42, H01L 23/44 take precedence)

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fillings or auxiliary members in containers or encapsulations selected or</td>
<td>H01L 23/42</td>
</tr>
<tr>
<td>arranged to facilitate heating or cooling</td>
<td></td>
</tr>
<tr>
<td>Cooling arrangements with the complete device being wholly immersed in</td>
<td>H01L 23/44</td>
</tr>
<tr>
<td>a fluid other than air</td>
<td></td>
</tr>
</tbody>
</table>

H01L 23/467

by flowing gases, e.g. air {(H01L 23/473 takes precedence)}

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cooling involving the transfer of heat by flowing liquids</td>
<td>H01L 23/473</td>
</tr>
</tbody>
</table>

H01L 23/473

by flowing liquids {(H01L 23/4332, H01L 23/4338 take precedence)}

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auxiliary members in containers: bellows</td>
<td>H01L 23/4332</td>
</tr>
<tr>
<td>Auxiliary members in containers: pistons</td>
<td>H01L 23/4338</td>
</tr>
</tbody>
</table>

H01L 23/4735

{Jet impingement (H01L 23/4336 takes precedence)}

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auxiliary members in containers: in combination with jet impingement</td>
<td>H01L 23/4336</td>
</tr>
</tbody>
</table>
### H01L 23/48

**Arrangements for conducting electric current to or from the solid state body in operation, e.g. leads, terminal arrangements (in general H01R); {Selection of materials therefor}**

**References**

#### Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Arrangements for connecting or disconnecting semiconductor or other solid-state bodies, and methods related thereto</th>
<th>H01L 24/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Terminals, leads in general</td>
<td>H01R</td>
</tr>
</tbody>
</table>

### H01L 23/482

**consisting of lead-in layers inseparably applied to the semiconductor body {(electrodes H01L 29/40)}**

**References**

#### Limiting references

This place does not cover:

| Electrodes of semiconductor devices | H01L 29/40 |

### H01L 23/485

**consisting of layered constructions comprising conductive layers and insulating layers, e.g. planar contacts {(H01L 23/4821, H01L 23/4822, H01L 23/4824, H01L 23/4825 take precedence; materials H01L 23/532, bond pads H01L 24/02, bump connectors H01L 24/10)}**

**References**

#### Limiting references

This place does not cover:

| Lead-in layers inseparably applied to the semiconductor body: bridge structures with air gap | H01L 23/4821 |
| Lead-in layers inseparably applied to the semiconductor body: beam leads | H01L 23/4822 |
| Lead-in layers inseparably applied to the semiconductor body: pads with extended contours | H01L 23/4824 |
| Lead-in layers inseparably applied to the semiconductor body: for devices consisting of semiconductor layers on insulating or semi-insulating substrates | H01L 23/4825 |
| Materials | H01L 23/532 |
| Bond pads | H01L 24/02 |
| Bump connectors | H01L 24/10 |
H01L 23/488
consisting of soldered (or bonded) constructions {(bump connectors H01L 24/01)}

References
Limiting references
This place does not cover:

| Bump connectors | H01L 24/01 |

H01L 23/495
Lead-frames {or other flat leads (H01L 23/498 takes precedence; lead frame interconnections between components H01L 23/52)}

References
Limiting references
This place does not cover:

| Leads on insulating substrates | H01L 23/498 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Interconnections between components using lead-frames | H01L 23/52 |

H01L 23/49506
{an insulative substrate being used as a diepad, e.g. ceramic, plastic (H01L 23/49531 takes precedence)}

References
Limiting references
This place does not cover:

| Lead-frames with additional leads being a wiring board | H01L 23/49531 |

H01L 23/49544
{Deformation absorbing parts in the lead frame plane, e.g. meanderline shape (H01L 23/49562 takes precedence)}

References
Limiting references
This place does not cover:

| Lead-frames: geometry for devices being provided for in H01L 29/00 | H01L 23/49562 |
### H01L 23/49548

{Cross section geometry (H01L 23/49562 takes precedence)}

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Lead-frames: geometry for devices being provided for in H01L 29/00</th>
<th>H01L 23/49562</th>
</tr>
</thead>
</table>

### H01L 23/49572

{consisting of thin flexible metallic tape with or without a film carrier (H01L 23/49503 - H01L 23/49568 and H01L 23/49575 - H01L 23/49579 take precedence)}

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Thin flexible metallic tape with or without a film carrier provided in the context of subject-matter covered by groups H01L 23/49503 - H01L 23/49568 and H01L 23/49575 - H01L 23/49579</th>
<th>H01L 23/49503 - H01L 23/49568 and; H01L 23/49575 - H01L 23/49579</th>
</tr>
</thead>
</table>

### H01L 23/498

Leads, {i.e. metallisations or lead-frames} on insulating substrates, {e.g. chip carriers (shape of the substrate H01L 23/13)}

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Shape of the substrate</th>
<th>H01L 23/13</th>
</tr>
</thead>
</table>

### H01L 23/49811

{Additional leads joined to the metallisation on the insulating substrate, e.g. pins, bumps, wires, flat leads (H01L 23/49827 takes precedence)}

**References**

**Limiting references**

This place does not cover:

| Leads on insulating substrates: via connections through the substrates | H01L 23/49827 |
H01L 23/49822

{Multilayer substrates (multilayer metallisation on monolayer substrate H01L 23/498)}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Multilayer metallisation on monolayer substrate | H01L 23/498 |

H01L 23/49827

{Via connections through the substrates, e.g. pins going through the substrate, coaxial cables (H01L 23/49822, H01L 23/49833, H01L 23/4985, H01L 23/49861 take precedence)}

References

Limiting references
This place does not cover:

| Leads on insulating substrates: multilayer substrates | H01L 23/49822 |
| Leads on insulating substrates: consisting of a plurality of insulating substrates | H01L 23/49833 |
| Leads on insulating substrates: flexible insulating substrates | H01L 23/4985 |
| Leads on insulating substrates: lead-frames fixed on or encapsulated in insulating substrates | H01L 23/49861 |

H01L 23/4985

{Flexible insulating substrates (H01L 23/49572 and H01L 23/49855 take precedence)}

References

Limiting references
This place does not cover:

| Lead-frames consisting of thin flexible metallic tape with or without a film carrier | H01L 23/49572 |
| Leads on insulating substrates: for flat-cards, e.g. credit cards | H01L 23/49855 |
H01L 23/49855
{for flat-cards, e.g. credit cards (cards per se G06K 19/00)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Cards per se</th>
<th>G06K 19/00</th>
</tr>
</thead>
</table>

H01L 23/49861
{Lead-frames fixed on or encapsulated in insulating substrates (H01L 23/4985, H01L 23/49805 take precedence)}

References
Limiting references
This place does not cover:

| Leads on insulating substrates: the leads being also applied on the sidewalls or the bottom of the substrate | H01L 23/49805 |
| Leads on insulating substrates: flexible insulating substrates | H01L 23/4985 |

H01L 23/49866
{characterised by the materials (materials of the substrates H01L 23/14, of the lead-frames H01L 23/49579)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Materials of the substrates | H01L 23/14 |
| Materials of the lead-frames | H01L 23/49579 |
| Conductive materials for PCBs | H05K/09D |

H01L 23/49877
{Carbon, e.g. fullerenes (superconducting fullerenes H01L 39/123)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Superconducting fullerenes | H01L 39/123 |
H01L 23/49883
{the conductive materials containing organic materials or pastes, e.g. for thick
films (for printed circuits H05K 1/092)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| For printed circuits | H05K 1/092 |

H01L 23/50
for integrated circuit devices, {e.g. power bus, number of leads}
(H01L 23/482 - H01L 23/498 take precedence)

References
Limiting references
This place does not cover:

| Arrangements for conducting electric current to or from the solid state
circuit body in operation: lead-in layers inseparably applied to the semiconductor
body | H01L 23/482 |
| Leads on insulating substrates | H01L 23/498 |

H01L 23/5222
{Capacitive arrangements or effects of, or between wiring layers (other
capacitive arrangements H01L 23/642)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Other capacitive arrangements | H01L 23/642 |

H01L 23/5227
{Inductive arrangements or effects of, or between, wiring layers (other
inductive arrangements H01L 23/645)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Other inductive arrangements | H01L 23/645 |
H01L 23/5228
{Resistive arrangements or effects of, or between, wiring layers (other resistive arrangements H01L 23/647)}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Other resistive arrangements | H01L 23/647 |

H01L 23/528
{Geometry or} layout of the interconnection structure {((H01L 27/0207 takes precedence; algorithms G06F 17/50)}

References

Limiting references
This place does not cover:

| Devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate: geometrical layout of the components | H01L 27/0207 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Algorithms, e.g. computer aided design of layouts of integrated circuits | G06F 17/50 |

H01L 23/53209
{based on metals, e.g. alloys, metal silicides (H01L 23/53285 takes precedence)}

References

Limiting references
This place does not cover:

| Arrangements for conducting electric current within the device in operation from one component to another: containing superconducting materials | H01L 23/53285 |
H01L 23/53276
{containing carbon, e.g. fullerenes (superconducting fullerenes H01L 39/123)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Superconducting fullerenes</th>
<th>H01L 39/123</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nanosized carbon materials per se</td>
<td>C01B 32/15</td>
</tr>
</tbody>
</table>

H01L 23/535
including internal interconnections, e.g. cross-under constructions {(internal lead connections H01L 23/481)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Internal lead connections          | H01L 23/481 |

H01L 23/538
the interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates {{H05K takes precedence; manufacture or treatment H01L 21/4846} ; mountings per se H01L 23/12; {materials H01L 23/49866}}

References
Limiting references
This place does not cover:

| Printed circuits; casings or constructional details of electric apparatus; manufacture of assemblages of electrical components | H05K |

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Manufacture or treatment</th>
<th>H01L 21/4846</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mountings per se</td>
<td>H01L 23/12</td>
</tr>
<tr>
<td>Materials</td>
<td>H01L 23/49866</td>
</tr>
</tbody>
</table>
H01L 23/5383

{Multilayer substrates (H01L 23/5385 takes precedence; multilayer metallisation on monolayer substrates H01L 23/538)}

References

Limiting references

This place does not cover:

| Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: assembly of a plurality of insulating substrates | H01L 23/5385 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Multilayer metallisation on monolayer substrates | H01L 23/538 |

H01L 23/5384

{Conductive vias through the substrate with or without pins, e.g. buried coaxial conductors (H01L 23/5383, H01L 23/5385 take precedence; pins attached to insulating substrates H01L 23/49811)}

References

Limiting references

This place does not cover:

| Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: multilayer substrates | H01L 23/5383 |
| Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: assembly of a plurality of insulating substrates | H01L 23/5385 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Pins attached to insulating substrates | H01L 23/49811 |
H01L 23/5387

{Flexible insulating substrates (H01L 23/5388 takes precedence)}

References

Limiting references

This place does not cover:

| Interconnection structure between a plurality of semiconductor chips being formed on, or in, insulating substrates: for flat cards, e.g. credit cards | H01L 23/5388 |

H01L 23/5388

{for flat cards, e.g. credit cards (cards per se G06K 19/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Cards per se | G06K 19/00 |

H01L 23/544

Marks applied to semiconductor devices (or parts), e.g. registration marks, alignment structures, wafer maps (test patterns for characterising or monitoring manufacturing processes H01L 22/00)

Definition statement

This place covers:

Marks for identification purposes, including electrical structures used to generate identification information for electrical read out.
Typical views of marks of this type:

![Typical views of marks](image)

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Marking devices, scribers</th>
<th>B25H 7/04</th>
</tr>
</thead>
<tbody>
<tr>
<td>Marking methods</td>
<td>B41M 5/00</td>
</tr>
<tr>
<td>Marks used for overlay monitoring in photolithography</td>
<td>G03F 7/70633</td>
</tr>
<tr>
<td>Alignment marks used in photolithographic machines</td>
<td>G03F 9/7073</td>
</tr>
</tbody>
</table>

**H01L 23/552**

Protection against radiation, e.g. light (or electromagnetic waves)

**Definition statement**

*This place covers:*

Electromagnetic shielding arrangements; RF interference suppression.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Electrostatic shielding in general</th>
<th>H05F 3/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Screening of apparatuses or components of PCB</td>
<td>H05K 9/00</td>
</tr>
</tbody>
</table>
H01L 23/58

Structural electrical arrangements for semiconductor devices not otherwise provided for {e.g. in combination with batteries (H01L 23/49593, H01L 23/49596 take precedence)}

References

Limiting references

This place does not cover:

| Lead-frames: battery in combination with a lead-frame | H01L 23/49593 |
| Lead-frames: oscillators in combination with a lead-frame | H01L 23/49596 |

H01L 23/585

{comprising conductive layers or plates or strips or rods or rings (H01L 23/60, H01L 23/62, H01L 23/64, H01L 23/66 take precedence)}

Definition statement

This place covers:

Active and passive measures to prevent or detect tampering; reverse engineering protection structures; seal rings, protection against delamination of layers during dicing

References

Limiting references

This place does not cover:

| Protection against electrostatic charges or discharges | H01L 23/60 |
| Protection against overvoltage | H01L 23/62 |
| Impedance arrangements | H01L 23/64 |
| High-frequency adaptations | H01L 23/66 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Secure housings for data carriers (memories) | G06F 21/86 |
| Protective means for data carriers (memories) | G06K 19/073 |
**H01L 23/60**

Protection against electrostatic charges or discharges, e.g. Faraday shields (in general H05F)

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Protection against electrostatic discharge (ESD) provided in a semiconductor body | H01L 27/0248 |
| Faraday shields in general | H05F 3/00 |

**H01L 23/642**

{Capacitive arrangements (H01L 23/49589, H01L 23/645, H01L 23/647, H01L 23/66 take precedence; capacitive effects between wiring layers on the semiconductor body H01L 23/5222)}

**References**

*Limiting references*

This place does not cover:

| Lead-frames: capacitor integral with or on the lead-frame | H01L 23/49589 |
| Impedance arrangements: inductive arrangements | H01L 23/645 |
| Impedance arrangements: resistive arrangements | H01L 23/647 |
| High-frequency adaptations | H01L 23/66 |

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Capacitive effects between wiring layers on the semiconductor body | H01L 23/5222 |

**H01L 23/645**

{Inductive arrangements (H01L 23/647, H01L 23/66 take precedence)}

**References**

*Limiting references*

This place does not cover:

| Impedance arrangements: resistive arrangements | H01L 23/647 |
| High-frequency adaptations | H01L 23/66 |
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Inductors formed within interconnection layers</th>
<th>H01L 23/5227</th>
</tr>
</thead>
</table>

**H01L 23/647**

{Resistive arrangements ([H01L 23/66, H01L 23/62 take precedence])}

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Protection against overvoltage</th>
<th>H01L 23/62</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-frequency adaptations</td>
<td>H01L 23/66</td>
</tr>
</tbody>
</table>

**H01L 24/00**

{Arrangements for connecting or disconnecting semiconductor or solid-state bodies; Methods or apparatus related thereto}

**Definition statement**

This place covers:

Examples of first level interconnects

1 = [H01L 24/10] and subgroups,

2 = [H01L 24/26] and subgroups,

3 = [H01L 24/26] and subgroups,

4 = [H01L 24/42] and subgroups


### References

#### Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacture or treatment of parts</td>
<td>H01L 21/48</td>
</tr>
<tr>
<td>Assemblies of semiconductor devices</td>
<td>H01L 21/50 - H01L 21/568</td>
</tr>
<tr>
<td>Applying interconnections to be used for carrying current between separate components within a device</td>
<td>H01L 21/768</td>
</tr>
<tr>
<td>Containers or seals</td>
<td>H01L 23/02 - H01L 23/10</td>
</tr>
<tr>
<td>Mountings</td>
<td>H01L 23/12 - H01L 23/15</td>
</tr>
<tr>
<td>Arrangements for cooling, heating, ventilating or temperature compensation</td>
<td>H01L 23/34 - H01L 23/4735</td>
</tr>
<tr>
<td>Arrangements for conducting electric current</td>
<td>H01L 23/48 - H01L 23/50 and H01L 23/52 - H01L 23/5389</td>
</tr>
<tr>
<td>Structural electrical arrangements</td>
<td>H01L 23/58 - H01L 23/66</td>
</tr>
<tr>
<td>Assemblies consisting of a plurality of individual semiconductor or other solid state devices</td>
<td>H01L 25/00 - H01L 25/18</td>
</tr>
<tr>
<td>Details of semiconductor bodies or electrodes of semiconductor devices adapted for rectifying, amplifying, oscillating or switching, or capacitors or resistors with at least one potential-jump barrier or surface barrier</td>
<td>H01L 29/00</td>
</tr>
<tr>
<td>Details peculiar to semiconductor devices sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation</td>
<td>H01L 31/00</td>
</tr>
<tr>
<td>Details peculiar to semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission</td>
<td>H01L 33/00</td>
</tr>
<tr>
<td>Details peculiar to thermoelectric devices comprising a junction of dissimilar materials</td>
<td>H01L 35/00</td>
</tr>
<tr>
<td>Details peculiar to thermoelectric devices without a junction of dissimilar materials or of thermomagnetic devices</td>
<td>H01L 37/00</td>
</tr>
<tr>
<td>Details peculiar to devices using superconductivity</td>
<td>H01L 39/00</td>
</tr>
<tr>
<td>Details peculiar to piezo-electric, electrostrictive, magnetostrictive devices in general</td>
<td>H01L 41/00</td>
</tr>
<tr>
<td>Details peculiar to devices using galvano-magnetic or similar magnetic effects</td>
<td>H01L 43/00</td>
</tr>
<tr>
<td>Details peculiar to solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier or of Ovshinsky-effect devices</td>
<td>H01L 45/00</td>
</tr>
<tr>
<td>Details peculiar to bulk negative resistance effect devices</td>
<td>H01L 47/00</td>
</tr>
<tr>
<td>Details peculiar to solid state devices not provided for in groups H01L 27/00 - H01L 47/00 and H01L 51/00 and not provided for in any other subclass</td>
<td>H01L 49/00</td>
</tr>
<tr>
<td>Details peculiar to solid state devices using organic materials as the active part, or using a combination of organic materials with other materials as the active part</td>
<td>H01L 51/00</td>
</tr>
</tbody>
</table>
Special rules of classification

The use of Indexing Codes of the indexing schemes H01L 24/00 and subgroups, H01L 2224/00 and subgroups and H01L 2924/00 and subgroups is mandatory.

H01L 24/02

{Bonding areas (on insulating substrates, e.g. chip carriers, H01L 23/49816, H01L 23/49838, H01L 23/5389); Manufacturing methods related thereto}

Definition statement

This place covers:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Bonding areas on insulating substrates, e.g. chip carriers | H01L 23/49816, H01L 23/49838, H01L 23/5389 |
Special rules of classification
The following figures show some key technologies relating to H01L 24/00
H01L 24/06
(of a plurality of bonding areas)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Physical circuit design | G06F 17/5068 |
Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

H01L 24/10

{Bump connectors (bumps on insulating substrates, e.g. chip carriers, H01L 23/49816); Manufacturing methods related thereto}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Bumps on insulating substrates, e.g. chip carriers | H01L 23/49816 |
H01L 24/11

{Manufacturing methods (for bumps on insulating substrates H01L 21/4853)}

Definition statement

This place covers:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Manufacturing methods for bumps on insulating substrates</th>
<th>H01L 21/4853</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inks, e.g. metallic inks</td>
<td>C09D 11/00</td>
</tr>
</tbody>
</table>
**H01L 24/12**

{Structure, shape, material or disposition of the bump connectors prior to the connecting process}

**Definition statement**

This place covers:

![Diagram](image1)

**H01L 24/14**

{of a plurality of bump connectors}

**Definition statement**

This place covers:

![Diagram](image2)
H01L 24/18
{High density interconnect [HDI] connectors; Manufacturing methods related thereto (interconnection structure between a plurality of semiconductor chips H01L 23/5389)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Interconnection structure between a plurality of semiconductor chips | H01L 23/5389 |

H01L 24/26
{Layer connectors, e.g. plate connectors, solder or adhesive layers; Manufacturing methods related thereto}

Definition statement
This place covers:

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| metal powder in organic matrix | H01B 1/22 |

H01L 24/27
{Manufacturing methods}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Applying fluids in general | B05C 9/02 |
Applying adhesive films using preforms

H01L 24/34

{Strap connectors, e.g. copper straps for grounding power devices; Manufacturing methods related thereto}

Definition statement

This place covers:

H01L 24/50

{Tape automated bonding [TAB] connectors, i.e. film carriers; Manufacturing methods related thereto (thin flexible metallic tape with or without a film carrier H01L 23/49572, flexible insulating substrates H01L 23/4985, H01L 23/5387)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Thin flexible metallic tape with or without a film carrier | H01L 23/49572 |
| Flexible insulating substrates | H01L 23/4985, H01L 23/5387 |

H01L 24/71

{Means for bonding not being attached to, or not being formed on, the surface to be connected (holders for supporting the complete device in operation H01L 23/32)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Holders for supporting the complete device in operation | H01L 23/32 |
| H01L 23/32 |
**H01L 24/80**

{Methods for connecting semiconductor or other solid state bodies using means for bonding being attached to, or being formed on, the surface to be connected}

**Definition statement**

*This place covers:*

![Diagram of interconnection methods](image)

**H01L 24/82**

{by forming build-up interconnects at chip-level, e.g. for high density interconnects [HDI] (interconnection structure between a plurality of semiconductor chips *H01L 23/5389*)}

**Definition statement**

*This place covers:*

![Diagram of build-up interconnects](image)

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Interconnection structure between a plurality of semiconductor chips | H01L 23/5389 |

**H01L 24/85**

{using a wire connector (wire bonding in general *B23K 20/004*)}

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Wire bonding in general | B23K 20/004 |
H01L 24/93
{Batch processes}

Definition statement
This place covers:

H01L 24/96
{the devices being encapsulated in a common layer, e.g. neo-wafer or pseudo-wafer, said common layer being separable into individual assemblies after connecting}

Definition statement
This place covers:

H01L 25/00
Assemblies consisting of a plurality of individual semiconductor or other solid state devices {; Multistep manufacturing processes thereof} (devices consisting of a plurality of solid state components formed in or on a common substrate H01L 27/00; photovoltaic modules or arrays of photovoltaic cells H01L 31/042 {; panels or arrays of photo electrochemical cells H01G 9/2068})

References
Limiting references
This place does not cover:

| Devices consisting of a plurality of solid state components formed in or on a common substrate | H01L 27/00 |
| Photovoltaic modules or arrays of photovoltaic cells | H01L 31/042 |
| Panels or arrays of photo electrochemical cells | H01G 9/2068 |
Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assembling semiconductor devices using processes or apparatus not provided for in a single one of the subgroups</td>
<td>H01L 21/06 - H01L 21/326</td>
</tr>
<tr>
<td>Assemblies of semiconductor devices on lead-frames</td>
<td>H01L 23/49575</td>
</tr>
<tr>
<td>Leads on insulating substrates (chip carriers)</td>
<td>H01L 23/498</td>
</tr>
<tr>
<td>Interconnection structures for a plurality of bare semiconductor chips provided on or in an insulating substrate</td>
<td>H01L 23/538</td>
</tr>
<tr>
<td>Arrangements for connecting or disconnecting semiconductor or solid-state bodies; methods related thereto</td>
<td>H01L 24/00</td>
</tr>
<tr>
<td>Integrated photodetecting devices on a substrate</td>
<td>H01L 27/146</td>
</tr>
<tr>
<td>Integration of organic light emitting devices (OLEDs), e.g. OLED displays</td>
<td>H01L 27/32</td>
</tr>
<tr>
<td>Tandem solar cells, meaning monolithically integrated solar cells with different wavelengths sensibilities deposited on one another by coating processes</td>
<td>H01L 31/0687, H01L 31/0725, H01L 31/076, H01L 31/078</td>
</tr>
<tr>
<td>Light sensitive devices structurally associated with, e.g. formed in or on a common substrate with, one or more electric light sources, and electrically or optically coupled thereto (e.g. opto-couplers)</td>
<td>H01L 31/12</td>
</tr>
<tr>
<td>Organic light emitting devices [OLEDs]</td>
<td>H01L 51/50</td>
</tr>
<tr>
<td>Couplings of light guides with optoelectronic elements</td>
<td>G02B 6/42</td>
</tr>
<tr>
<td>Static Stores</td>
<td>G11C</td>
</tr>
<tr>
<td>Generators using solar cells or photovoltaic modules</td>
<td>H02S</td>
</tr>
<tr>
<td>Details of complete circuit assemblies provided for in another subclass, e.g. details of television receivers, see the relevant subclass, e.g.</td>
<td>H04N</td>
</tr>
<tr>
<td>Details of assemblies of electrical components in general</td>
<td>H05K</td>
</tr>
</tbody>
</table>

Special rules of classification

The classification of additional information is mandatory in this main group.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assembly of a Device</td>
<td>The &quot;assembly&quot; of a device is the building up of the device from its component constructional units and includes the provision of fillings in containers.</td>
</tr>
</tbody>
</table>

H01L 25/03

all the devices being of a type provided for in the same subgroup of groups H01L 27/00 - H01L 51/00, e.g. assemblies of rectifier diodes

Definition statement

This place covers:

- "package in package" devices
- assemblies of rectifier diodes
H01L 25/042
{the devices being arranged next to each other (solar cells H01L 31/042)}

**Definition statement**
*This place covers:*
Arrays of photodetectors disposed next to one another on a common substrate.

**References**

**Limiting references**
*This place does not cover:*

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multicolour imagers having a stacked pixel-element structure</td>
<td>H01L 27/14647</td>
</tr>
<tr>
<td>Multispectral infra-red imagers, having a stacked pixel-element structure</td>
<td>H01L 27/14652</td>
</tr>
<tr>
<td>Assemblies of thin film solar cells</td>
<td>H01L 31/042</td>
</tr>
</tbody>
</table>

**Informative references**
*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanically stacked solar cells</td>
<td>H01L 31/043</td>
</tr>
</tbody>
</table>

**Glossary of terms**
*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disposed</td>
<td>means that photodetectors already manufactured are individually placed on the common substrate, as opposed to &quot;integrated&quot; which means the devices are all formed on or in said substrate during the same process</td>
</tr>
</tbody>
</table>
**H01L 25/043**

{Stacked arrangements of devices}

**Definition statement**

*This place covers:*

Photodetectors mechanically stacked on one another:

![FIG. 8](image)

**H01L 25/047**

{the devices being of a type provided for in group H01L 51/42, e.g. photovoltaic modules based on organic solar cells}

**Definition statement**

*This place covers:*

Mechanically stacked organic solar cells

Example:

EP1603169

![Diagram](image)
References

Limiting references

This place does not cover:

| Devices consisting of a plurality of light sensitive organic semiconductor components, e.g. organic thin film solar cells, formed in or on a common substrate | H01L 27/301 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Organic light sensitive devices | H01L 51/42 |

H01L 25/048

{the devices being of a type provided for in group H01L 51/50, e.g. assembly of organic light emitting devices}

Definition statement

This place covers:

Assemblies consisting of a plurality of devices specially adapted for light emission and using organic materials as the active part, e.g. assembly of OLEDs.

Examples:

US2006/0244374
References

Limiting references
This place does not cover:

| Tiled displays | H01L 27/3293 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| OLEDs electrically connected in parallel | H01L 27/3202 |
| OLEDs electrically connected in series | H01L 27/3204 |
| Stacked OLEDs | H01L 27/3209 |
| Dual displays | H01L 27/3267 |
| Light sources using semiconductor devices as light-generating elements, e.g. using light-emitting diodes [LED] or lasers | F21K 9/00 |
H01L 25/075
the devices being of a type provided for in group H01L 33/00

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Light sources using semiconductor devices as light-generating elements, e.g. using light-emitting diodes [LED] or lasers | F21K 9/00 |

H01L 25/16
the devices being of types provided for in two or more different main groups of H01L 27/00 - H01L 49/00 (and H01L 51/00), e.g. forming hybrid circuits (interconnections for hybrid circuits H01L 23/5389)

Definition statement
This place covers:
Hybrid modules of active and passive components

References
Limiting references
This place does not cover:

| Interconnections for hybrid circuits | H01L 23/5389 |

H01L 25/18
the devices being of types provided for in two or more different subgroups of the same main group of groups H01L 27/00 - H01L 51/00 (comprising devices provided for in H01L 27/144 and subgroups, see H01L 27/144 and subgroups)

Definition statement
This place covers:
Arrangement of memory and logic chips
Arrangement of diode and IGBT

References
Limiting references
This place does not cover:

| Devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate and controlled by radiation | H01L 27/144 |
H01L 25/50

{Multistep manufacturing processes of assemblies consisting of devices, each device being of a type provided for in group H01L 27/00 or H01L 29/00 (H01L 21/50 takes precedence)}

Definition statement

This place covers:

Processes to fabricate devices formed of an assembly of a multiplicity of components on a host substrate.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Assembly of semiconductor devices using processes or apparatus not provided for in a single one of the subgroups H01L 21/06 - H01L 21/326</th>
<th>H01L 21/50</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assemblies consisting of a plurality of individual semiconductor or other solid state devices</td>
<td>H01L 25/00</td>
</tr>
</tbody>
</table>

H01L 27/00

Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate (details thereof H01L 23/00, H01L 29/00 - H01L 51/00; assemblies consisting of a plurality of individual solid state devices H01L 25/00)

Definition statement

This place covers:

Semiconductor devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate, i.e. integrated circuits.

Examples of integrated circuits are: memory arrays (SRAM, DRAM, MRAM, ROM, PROM, EPROM, EEPROM), image sensors (CMOS-type image sensors, CCD-type image sensors), organic and inorganic light emitting diode (LED, OLED) displays, logic integrated circuits, switching integrated circuits, arrangements of active or passive semiconducting components in or on a common substrate, electrostatic discharge (ESD) protection integrated circuits.

This main group covers the following areas:

Semiconductor devices formed in or on a common substrate including only passive thin-film or thick-film components.

Semiconductor devices formed in or on a common substrate including inorganic semiconductor components adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier, e.g. memory arrays.

Semiconductor devices formed in or on a common substrate including inorganic semiconductor components sensitive to electromagnetic radiation, e.g. imagers.

Semiconductor devices formed in or on a common substrate including inorganic semiconductor components having at least one potential-jump barrier or surface barrier and adapted for light emission, e.g. LED arrays.
Semiconductor devices formed in or on a common substrate including thermoelectric or thermomagnetic components.

Semiconductor devices formed in or on a common substrate including components exhibiting superconductivity.

Semiconductor devices formed in or on a common substrate including piezo-electric, electrostrictive or magnetostrictive components.

Semiconductor devices formed in or on a common substrate including components using galvanomagnetic effects or similar magnetic field effects.

Semiconductor devices formed in or on a common substrate including solid state components for rectifying, amplifying or switching without a potential-jump barrier or surface barrier.

Semiconductor devices formed in or on a common substrate including bulk negative resistance effect components.

Semiconductor devices formed in or on a common substrate including components using organic materials as the active part, or using a combination of organic materials with other materials as the active part, e.g. OLED displays, OTFT arrays, OPV modules.

Example:

---

**Relationships with other classification places**

Only the physical structure of integrated circuits is covered by H01L 27/00. Electrical circuit arrangements are classified elsewhere. For instance, electrical circuit arrangements for driving OLED displays are covered by G09G 3/3208. Electrical circuit arrangements for driving semiconductor imagers are covered by H04N 5/335.

Examples:
References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single step processes or apparatus specially adapted for the manufacture or treatment of integrated circuits or of parts thereof</td>
<td>H01L 21/70, H01L 31/00 - H01L 51/00</td>
</tr>
<tr>
<td>Details of integrated circuits</td>
<td>H01L 23/00, H01L 24/00, H01L 29/00 - H01L 51/00</td>
</tr>
<tr>
<td>Assemblies consisting of a plurality of individual semiconductor or other solid state devices</td>
<td>H01L 25/00</td>
</tr>
<tr>
<td>Printed circuits</td>
<td>H05K 1/00</td>
</tr>
</tbody>
</table>
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Components for integrated circuits | H01L 29/00 - H01L 51/00 |
| Processes or apparatus specially adapted for the manufacture or treatment of organic semiconductor integrated devices | H01L 51/0001 |
| Encapsulations specially adapted for OLED displays | H01L 51/5237 |
| Processes or apparatus specially adapted for the manufacture or treatment of OLED displays | H01L 51/56 |
| Coatings | C23C 14/00 |
| Light sources | F21K 2/00 |
| Light sources using semiconductor devices as light-generating elements, e.g. using light-emitting diodes [LED] or lasers | F21K 9/00 |
| Bolometers | G01J 5/20 |
| Measuring electrical variables | G01R |
| Measuring X-radiation, gamma radiation, corpuscular radiation, or cosmic radiation | G01T 1/00 |
| Lenses | G02B 3/00 |
| Optical filters | G02B 5/20 |
| Polarisers | G02B 5/30 |
| Light guides | G02B 6/00 |
| Photonic crystals | G02B 6/1225 |
| Liquid crystal displays | G02F 1/13 |
| Non-retroactive systems for regulating electric variables by using an uncontrolled element, or an uncontrolled combination of elements, such element or such combination having self-regulating properties | G05F 3/00 |
| Touch screens | G06F 3/041 |
| Computer aided physical circuit design, e.g. layout for integrated circuits | G06F 17/5068 |
| Control circuits for electroluminescent panels based on semiconductive elements, e.g. LEDs | G09G 3/32 |
| Circuit arrangements for driving OLED displays | G09G 3/3208 |
| Digital stores | G11C 11/00, G11C 13/00, G11C 16/00, G11C 17/00 |
| Alloys | H01B 1/02 |
| Field emission displays | H01J 1/62 |
| Plasma display panels | H01J 11/00 |
| Semiconductor Lasers | H01S 5/00 |
| Electronic switching or gating | H03K 17/00 |
| Logic circuits, inverting circuits | H03K 19/00 |
| Circuit arrangements for driving semiconductor imagers | H04N 5/335 |
| Light sources with substantially two-dimensional radiating surfaces | H05B 33/12 |
**Special rules of classification**

Only monolithically integrated devices are covered by main group [H01L 27/00](#), in contrast to assemblies consisting of a plurality of individual semiconductor or other solid state devices which are covered by main group [H01L 25/00](#).

In this main group, in the absence of an indication to the contrary, classification is made in the last appropriate place.

In this main group the use of Indexing Code-codes is mandatory to classify additional information. Keywords are assigned to define the invention whenever no appropriate group symbol is available, as well as to define further relevant aspects of the invention.

In this main group the circulation of documents to other related fields is mandatory, whenever appropriate.

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Passive semiconductor component:</th>
<th>semiconductor component not introducing energy into the integrated circuit where they are integrated. Examples thereof are resistors, capacitors, inductors.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active semiconductor component:</td>
<td>semiconductor component introducing energy into the integrated circuit where they are integrated. Examples thereof are transistors, diodes, and thyristors.</td>
</tr>
<tr>
<td>SOI (Semiconductor on insulator):</td>
<td>Thin monocrystalline semiconductor layer bonded to a support substrate by means of an intermediate insulating layer. Generally a very thin silicon wafer is molecular-bonded to a support substrate by means of a SiO2 layer.</td>
</tr>
</tbody>
</table>
CMOS structure: Complementary metal oxide semiconductor structure comprising a PMOSFET and an NMOSFET connected the following way. Example:

- Their sharp I-V curve results in low power consumption. They are used as inverters.
<table>
<thead>
<tr>
<th>Static random access memory (SRAM):</th>
<th>semiconductor memory wherein each bit of data is stored on four transistors that form two cross coupled inverters. It does not need to be refreshed periodically (static). Example:</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Six-transistor CMOS SRAM cell" /></td>
<td>A six-transistor CMOS SRAM cell.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dynamic random access memory (DRAM):</th>
<th>semiconductor memory wherein each bit of data is stored in a separate capacitor. In general it comprises a transistor and a capacitor. The information fades unless the capacitor charge is refreshed periodically (dynamic). Example: US-A-3387286</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image2.png" alt="Diagram of DRAM cell" /></td>
<td>FIG. 2</td>
</tr>
</tbody>
</table>

186
**EEPROM:**

Electrically erasable programmable read only memory. It generally comprises a select transistor and a memory cell being a MOSFET transistor having a double gate: a floating gate for charge accumulation and state determination, and a control gate, capacitively coupled to the floating gate to determine its state. Example:

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>SITL structure</td>
<td>Static induction transistor logic structure</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
</tr>
<tr>
<td>I2L structure</td>
<td>Integrated injection logic structure</td>
</tr>
<tr>
<td>RAM</td>
<td>Random access memory</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static random access memory</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic random access memory</td>
</tr>
<tr>
<td>FerriRAM, FeRAM</td>
<td>Ferroelectric RAM</td>
</tr>
<tr>
<td>MRAM</td>
<td>Magnetic RAM</td>
</tr>
<tr>
<td>ROM</td>
<td>Read only memory</td>
</tr>
<tr>
<td>PROM</td>
<td>Programmable read only memory</td>
</tr>
<tr>
<td>EPROM</td>
<td>Electrically programmable read only memory</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Electrically erasable programmable read only memory</td>
</tr>
<tr>
<td>APS</td>
<td>Active pixel sensor</td>
</tr>
<tr>
<td>ReRAM, RRAM</td>
<td>Resistance random access memory</td>
</tr>
<tr>
<td>PRAM, PCRAM</td>
<td>Phase-change memory</td>
</tr>
<tr>
<td>PPS</td>
<td>Passive pixel sensor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>CCD imager</td>
<td>Charge coupled device imager</td>
</tr>
<tr>
<td>OLED display</td>
<td>Organic light emitting diode display</td>
</tr>
<tr>
<td>TOLED display</td>
<td>Transparent OLED display</td>
</tr>
<tr>
<td>AMOLED display</td>
<td>Active matrix OLED display</td>
</tr>
</tbody>
</table>
PMOLED display | Passive matrix OLED display
---|---
OTFT array | Organic thin film transistor array
TFT array | Thin film transistor array
SOI | Semiconductor on insulator
CCM | Colour changing medium

**H01L 27/01**

comprising only passive thin-film or thick-film elements formed on a common insulating substrate {(passive two-terminal components without a potential-jump or surface barrier for integrated circuits, details thereof and multistep manufacturing processes therefor H01L 28/00)}

**Definition statement**

This place covers:
Integration of only passive components such as resistors, inductors, capacitors

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Integration of passive components with components specially adapted for rectifying, oscillating, amplifying or switching on a substrate being an insulating body (e.g. SOI):</th>
<th>H01L 27/13</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passive components as such</td>
<td>H01L 28/00, H01L 29/8605, H01L 29/92</td>
</tr>
</tbody>
</table>

**H01L 27/013**

{Thick-film circuits}

**Definition statement**

This place covers:
Devices formed in a bulk semiconductor substrate

**H01L 27/016**

{Thin-film circuits}

**Definition statement**

This place covers:
Devices formed on a substrate by thin-film technology.
H01L 27/02
including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier

Definition statement
This place covers:
Integration of active and passive components
Reverse Engineering

H01L 27/0207
{Geometrical layout of the components, e.g. computer aided design; custom LSI, semi-custom LSI, standard cell technique}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Master slice integrated circuits</th>
<th>H01L 27/118</th>
</tr>
</thead>
<tbody>
<tr>
<td>Computer aided physical circuit design, e.g. layout for integrated circuits</td>
<td>G06F 17/50</td>
</tr>
</tbody>
</table>

H01L 27/0211
{adapted for requirements of temperature}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Cooling arrangements per se                          | H01L 23/34                      |

H01L 27/0222
{Charge pumping, substrate bias generation structures}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Circuits therefor                                    | G05F 3/205                     |
H01L 27/0225
{Charge injection in static induction transistor logic structures [SITL]}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Circuits therefor</th>
<th>H03K 19/0912</th>
</tr>
</thead>
</table>

H01L 27/0233
{Integrated injection logic structures [I2L]}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Circuits therefor</th>
<th>H03K 19/091</th>
</tr>
</thead>
</table>

H01L 27/0248
{for electrical or thermal protection, e.g. electrostatic discharge [ESD] protection}

Definition statement

This place covers:
Integration aspects of protecting structures, directed to increase the reliability of integrated circuits, e.g. integrated device arrangements protecting against over-voltage damages, against over-current damages, against thermal runaway, ESD protections, EOS protections.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Protection arrangements not implemented within the integrated circuit, e.g. protections at packaging level, at printed circuit board level, or at the system level. | H01L 23/34, H01L 23/60, H01L 23/62, H05K/02, H05K 7/20; H02H 9/04 |
| Components per se, including components used as protecting elements | H01L 29/00 |
| Emergency protective circuit arrangements | H02H |
| Circuit arrangements for protecting amplifiers | H03F 1/52 |
| Circuit arrangements for protecting electronic switches | H03K 17/08 |
| Circuit arrangements for protecting logic circuits | H03K 19/003 |

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| IC | Integrated Circuit |
Electro Static Discharge (ESD)
Electrical Over-Stress (EOS)
Safe Operating Area (SOA)

H01L 27/0251
{for MOS devices}

Definition statement
This place covers:
Integration aspects of protecting device arrangements, wherein the device to be protected includes at least a MOS device.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:
- Latch-up prevention in CMOS

H01L 27/0255
{using diodes as protective elements}

Definition statement
This place covers:
Integration aspects of protecting diodes

References
Informative references
Attention is drawn to the following places, which may be of interest for search:
- Multistep processes for the fabrication of diodes
- Using diode connected bipolar transistors
- Using diode connected field effect transistors
- IC including a plurality of component not having an active region in common
- IC including a plurality of component not having an active region in common
- Structural association of diodes and VDMOS
- Structural association of diodes and LDMOS
- Diodes per se
**H01L 27/0259**

{using bipolar transistors as protective elements}

**Definition statement**

*This place covers:*
Integration aspects of protecting structures including bipolar transistors, and of the biasing arrangements which render structures adapted to be used as protecting elements

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>References</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multistep processes for the fabrication of bipolar transistors</td>
<td>H01L21/331</td>
</tr>
<tr>
<td>Bipolar transistors per se</td>
<td>H01L 29/73</td>
</tr>
</tbody>
</table>

**H01L 27/0262**

{including a PNP transistor and a NPN transistor, wherein each of said transistors has its base coupled to the collector of the other transistor, e.g. silicon controlled rectifier [SCR] devices}

**Definition statement**

*This place covers:*
Integration aspects of protecting silicon controlled rectifiers, and of their triggering structures.

Example: (from EP 2246885 A1)

![Diagram](image)

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>References</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multistep processes for the fabrication of thyristors</td>
<td>H01L21/332</td>
</tr>
<tr>
<td>Latch-up prevention in CMOS</td>
<td>H01L 27/0921</td>
</tr>
<tr>
<td>Thyristors per se</td>
<td>H01L 29/74</td>
</tr>
</tbody>
</table>
**H01L 27/0266**

{using field effect transistors as protective elements}

**Definition statement**

*This place covers:*

Integration aspects of protecting field effect transistors, and of the triggering structures which render said field effect transistors adapted to be used as protecting elements

**References**

*Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multistep processes for the fabrication of field effect transistors</td>
<td>H01L21/335</td>
</tr>
<tr>
<td>Field effect transistors per se</td>
<td>H01L 29/772</td>
</tr>
<tr>
<td>Voltage or current sensing structures in VDMOS</td>
<td>H01L 29/7815</td>
</tr>
<tr>
<td>Voltage or current sensing structures in LDMOS</td>
<td>H01L 29/7826</td>
</tr>
</tbody>
</table>

**H01L 27/027**

{specially adapted to provide an electrical current path other than the field effect induced current path}

**Definition statement**

*This place covers:*

Integration aspects of structural adaptations of the field effect transistors which make them electrically behave in a way which substantially differs from the usual one; modifications aimed to enhance parasitic effects, e.g. the bipolar transistor inherently present in MOS transistors.
Example:

H01L 27/027

{involving a parasitic bipolar transistor triggered by the local electrical biasing of the layer acting as base of said parasitic bipolar transistor}

Definition statement

This place covers:
Integration details concerning the doping profile, the shape, the structure, the dimensioning of the layer acting as base of the bipolar transistor and of its contact region
Example:

**FIG. 10A**

**FIG. 10B**

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Prevention of punch-through</th>
<th>H01L 29/1083</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prevention of bipolar effect</td>
<td>H01L 29/1087</td>
</tr>
</tbody>
</table>

**H01L 27/0281**

(field effect transistors in a "Darlington-like" configuration)

Definition statement

This place covers:

Integration of an active clamp by means of a field effect transistor, which is driven in a conducting state by a further field effect transistor coupled to its gate electrode.
Example:

References

Limiting references

This place does not cover:

Active clamps driven by an inverter

H01L 27/0285

{bias arrangements for gate electrode of field effect transistors, e.g. RC networks, voltage partitioning circuits (H01L 27/0281 takes precedence)}

Definition statement

This place covers:

Integration of an active clamp by means of a field effect transistor, which is driven in a conducting state by a RC discriminating circuit or by other voltage partitioning circuits.
References

Limiting references

This place does not cover:

| Field-effect transistors in a "Darlington-like" configuration as protective elements | H01L 27/0281 |

H01L 27/0288

{using passive elements as protective elements, e.g. resistors, capacitors, inductors, spark-gaps}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Structural details of fuses | H01L 23/525, H01L 23/62 |
| Impedance arrangements | H01L 23/64 |
| Multistep processes for the fabrication of resistors, capacitors, inductors | H01L 28/00 |
| Resistors or capacitors per se | H01L 29/8605, H01L 29/92, H01L 28/00 |

H01L 27/0292

{using a specific configuration of the conducting means connecting the protective devices, e.g. ESD buses}

Definition statement

This place covers:

Details concerning the electrical interconnections between the protecting structures and/or the connections between the protecting structures and the circuit to be protected; specific routing schemes or the provision of dedicated conducting path for the triggering of the protecting structures as well as for the evacuation of the discharge current.
Example:

![Diagram of ESD protection circuit](image)

**FIG. 2**

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Interconnections</th>
<th>H01L 23/522</th>
</tr>
</thead>
<tbody>
<tr>
<td>Routing algorithms</td>
<td>G06F 17/50</td>
</tr>
</tbody>
</table>

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>ESD buses</th>
</tr>
</thead>
<tbody>
<tr>
<td>conductive traces dedicated to the evacuation of current produced by an electrostatic discharge, or to the propagation of triggering signal for the protecting elements</td>
</tr>
</tbody>
</table>

**H01L 27/0296**

(involving a specific disposition of the protective devices)

**Definition statement**

*This place covers:*

Integration of the protecting devices in specific areas of the integrated circuit, such as under the bonding pads, or within the scribe-lines, in peripheral regions of memories or TFT displays, in the substrate region below the insulator layer of SOI wafers.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>IC having three dimensional layout</th>
<th>H01L 27/06</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid SOI</td>
<td>H01L 27/1207</td>
</tr>
<tr>
<td>Arrangements to prevent high voltage or static electricity failures in active matrix liquid crystal display cells</td>
<td>G02F 1/136204</td>
</tr>
</tbody>
</table>

**H01L 27/0617**

{comprising components of the field-effect type (H01L 27/0251 takes precedence)}

References

Limiting references

This place does not cover:

| Electrical or thermal protection for MOS devices | H01L 27/0251 |

**H01L 27/10**

including a plurality of individual components in a repetitive configuration

Definition statement

This place covers:

Cross-point memories using a fuse or anti-fuse as the active element.

**H01L 27/101**

{including resistors or capacitors only}

Definition statement

This place covers:

Cross-point memories

**H01L 27/1021**

{including diodes only}

Definition statement

This place covers:

Cross-point memories in which a diode is the selection element.
H01L 27/1023
{Bipolar dynamic random access memory structures}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Circuits             | G11C 11/24, G11C 11/34 |

H01L 27/1025
{Static bipolar memory cell structures}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Circuits         | G11C 11/40 |

H01L 27/1026
{Bipolar electrically programmable memory structures (using fuses H01L 23/525)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Using fuses | H01L 23/525 |

H01L 27/105
including field-effect components

Definition statement
This place covers:
Integration of memories (e.g. SRAM, ROM, PROM) with peripheral circuits.

References
Limiting references
This place does not cover:

| Integration of DRAM memories with peripheral circuits | H01L 27/10894, H01L 27/10897 |
| Integration of FeRAM memories with peripheral circuits | H01L 27/11509, H01L 27/11592 |
| Integration of floating-gate memories with peripheral circuits | H01L 27/11526 |
Integration of nitride-based memories (e.g. NROM, MONOS, SONOS) with peripheral circuits

H01L 27/108

Dynamic random access memory structures

Definition statement
This place covers:
Dynamic random access memory structures and corresponding multistep manufacturing methods.

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Bipolar DRAMs</th>
<th>H01L 27/1023</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuits</td>
<td>G11C 11/24, G11C 11/401</td>
</tr>
</tbody>
</table>

Special rules of classification
In this group and its groups the last place rule is not used and multi-aspect classification is used, i.e. classification is made in any appropriate place.

H01L 27/10802

{comprising floating-body transistors, e.g. floating-body cells}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Floating-body transistors per se | H01L 27/7841 |

H01L 27/10805

{with one-transistor one-capacitor memory cells}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Capacitors for integrated circuits per se | H01L 28/00, H01L 29/92 |
H01L 27/10823
{the transistor having a trench structure in the substrate}

References

Limiting references
This place does not cover:

One-transistor one-capacitor cells in which both the transistor and the capacitor are in one substrate trench  

H01L 27/10826
{the transistor being of the FinFET type}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

FinFETs per se  

H01L 27/10829
{the capacitor being in a substrate trench}

References

Limiting references
This place does not cover:

One-transistor one-capacitor cells in which both the transistor and the capacitor are in one substrate trench  

Informative references
Attention is drawn to the following places, which may be of interest for search:

Conductor-insulator-semiconductor capacitors (e.g. formed in a substrate trench) per se  

H01L 27/10844
{Multistep manufacturing methods}

References

Limiting references
This place does not cover:

Manufacturing methods for DRAM cells based on floating-body transistors  

H01L 27/10802
H01L 27/1085
{with at least one step of making the capacitor or connections thereto}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Making the capacitor per se | H01L 28/40, H01L 29/66181 |

H01L 27/1087
{with at least one step of making the trench}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Making the capacitor per se | H01L 29/66181 |

H01L 27/10873
{with at least one step of making the transistor}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Making the transistor per se | H01L 29/66409 |

H01L 27/10876
{the transistor having a trench structure in the substrate (vertical transistor in combination with a capacitor formed in a substrate trench H01L 27/10864)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Vertical transistor in combination with a capacitor formed in a substrate trench | H01L 27/10864 |
H01L 27/10879
{the transistor being of the FinFET type}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| FinFETs per se | H01L 29/785 |

H01L 27/10888
{with at least one step of making a bit line contact}

References

Limiting references
This place does not cover:

| Integration of SRAM memories with peripheral circuits | H01L 27/105 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Making contacts per se | H01L 21/768 |
| Circuits | G11C 11/41 |

H01L 27/11
Static random access memory structures

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Manufacture of resistors per se | H01L 28/20 |
| circuits | G11C 11/40 |

H01L 27/112
Read-only memory structures {[ROM] and multistep manufacturing processes therefor}

Definition statement
This place covers:
ROM (e.g. mask ROM) and PROM (e.g. memory cells comprising a field-effect transistor and a fuse or anti-fuse) memories.
References

Limiting references

This place does not cover:

| Cross-point memories without a field-effect transistor | H01L 27/10, H01L 27/101, H01L 27/1021 |
| Integration of ROM or PROM memories with peripheral circuits | H01L 27/105 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Circuits and programmation of ROMs and PROMs | G11C 17/00 |

H01L 27/115

Electrically programmable read-only memories; Multistep manufacturing processes therefor

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Circuits and programmation of EEPROMs | G11C 11/22, G11C 16/00 |

H01L 27/11502

with ferroelectric memory capacitors

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Ferroelectric capacitors per se | H01L 28/55 |

H01L 27/11517

with floating gate

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Floating-gate transistors per se | H01L 29/788 |

Special rules of classification

In groups H01L 27/11517 - H01L 27/1156, in the absence of indication to the contrary, an invention is classified in the last appropriate place.
**H01L 27/11563**
with charge-trapping gate insulators, e.g. MNOS or NROM

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Memory transistors in which the charge is stored in an insulating charge-trapping layer per se | H01L 29/792 |

**H01L 27/11585**
with the gate electrodes comprising a layer used for its ferroelectric memory properties, e.g. metal-ferroelectric-semiconductor [MFS] or metal-ferroelectric-metal-insulator-semiconductor [MFMIS]

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Memory transistors with a ferroelectric layer in the gate stack per se | H01L 29/78391 |

**H01L 27/118**
Masterslice integrated circuits

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Computer aided physical circuit design, e.g. layout design for integrated circuits | G06F 17/50 |

**Special rules of classification**

If a layout is shown, the group symbol H01L 27/0207 is also allocated.

**H01L 2027/11829**

{Isolation techniques}

**Definition statement**

This place covers:

Electrical and thermal isolation structures between pixels.
Example of an electrical isolation structure

Example of a thermal isolation structure

**H01L 27/12**

the substrate being other than a semiconductor body, e.g. an insulating body

**Definition statement**

*This place covers:*
Integration of TFTs on an insulating or insulator-covered substrate, such as
Glass, plastic, insulator coated metal or other non-semiconducting substrates.

**References**

*Limiting references*

*This place does not cover:*

AMOLED displays

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

Manufacture of a plurality of TFTs on a non-semiconducting substrate
Multistep processes to manufacture TFTs

Thin film unipolar field-effect transistors, i.e. TFTs, per se

Active matrix LCD displays

Circuit arrangements for AM displays

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMLCD display</td>
<td>active matrix liquid crystal display</td>
</tr>
<tr>
<td>TFT</td>
<td>Thin film unipolar field-effect transistor</td>
</tr>
<tr>
<td>AMOLED display</td>
<td>active matrix organic light emitting diode display</td>
</tr>
</tbody>
</table>

H01L 27/1203

{the substrate comprising an insulating body on a semiconductor body, e.g. SOI (three-dimensional layout H01L 27/0688)}

Definition statement

This place covers:
SOI integrated circuits.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>H01L 21/762</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric regions, such as EPIC dielectric isolation, LOCOS; Trench refilling techniques, SOI technology</td>
<td>H01L 21/84</td>
</tr>
<tr>
<td>Multistep processes to manufacture devices on a substrate being other than a semiconductor body</td>
<td>H01L 29/66772</td>
</tr>
<tr>
<td>Multistep processes to manufacture monocrystalline silicon TFTs on insulating substrates</td>
<td>H01L 29/78654</td>
</tr>
<tr>
<td>Monocrystalline TFTs per se</td>
<td>H01L 29/78654</td>
</tr>
</tbody>
</table>

H01L 27/1207

{combined with devices in contact with the semiconductor body, i.e. bulk/SOI hybrid circuits}

Definition statement

This place covers:
Integrated circuits employing partial SOI.
H01L 27/1211
{combined with field-effect transistors with a horizontal current flow in a vertical sidewall of a semiconductor body, e.g. FinFET, MuGFET}

Definition statement
This place covers:
Integrated circuits with FinFETs on an insulating substrate

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Arrangements including only transistors with a horizontal current flow in a vertical sidewall of a semiconductor body, e.g. FinFET, MuGFET | H01L 27/0886 |
| Arrangements including only CMISFET transistors with a horizontal current flow in a vertical sidewall of a semiconductor body, e.g. FinFET, MuGFET | H01L 27/0924 |
| Multistep processes to manufacture transistors with a gate at the side of the channel and a horizontal current flow | H01L 29/66795 |
| Transistors with a gate at the side of the channel and a horizontal current flow | H01L 29/785 |

Synonyms and Keywords
In patent documents, the following abbreviations are often used:

| FinFET | MuGFET, BarFET, Triple gate FET, OMEGA FET, Pi-Gate FET |

H01L 27/1274
{using crystallisation of amorphous semiconductor or recrystallisation of crystalline semiconductor}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Crystallisation per se | H01L 21/2022, H01L 21/02667 |

H01L 27/13
combined with thin-film or thick-film passive components

Definition statement
This place covers:
Integrated circuits having TFTs integrated with passive components, e.g. antennas, capacitors
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>References</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memories employing capacitors, e.g. DRAM passive two-terminal components without a potential-jump or surface barrier for integrated circuits, details thereof and multistep manufacturing processes therefor</td>
<td>H01L 27/108</td>
</tr>
<tr>
<td>SOI arrangements</td>
<td>H01L 27/12</td>
</tr>
<tr>
<td>Storage capacitors associated with the pixel electrode in AMLCD displays</td>
<td>G02F 1/136213</td>
</tr>
<tr>
<td>RFID circuits</td>
<td>G06K 19/07749</td>
</tr>
</tbody>
</table>

**H01L 27/14**

including semiconductor components sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and specially adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation (radiation-sensitive components structurally associated with one or more electric light sources only **H01L 31/14**; couplings of light guides with optoelectronic elements **G02B 6/42**)

**Definition statement**

*This place covers:*

Arrangements of solar cells or other semiconducting energy conversion devices, arrangements of photo-detecting elements such as 2D-detectors, imagers

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>References</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiation-sensitive components structurally associated with one or more electric light sources only</td>
<td>H01L 31/14</td>
</tr>
<tr>
<td>Couplings of light guides with optoelectronic elements</td>
<td>G02B 6/42</td>
</tr>
</tbody>
</table>

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>References</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiation detecting components</td>
<td>H01L 31/00</td>
</tr>
</tbody>
</table>
**H01L 27/142**

Energy conversion devices (photovoltaic modules or arrays of single photovoltaic cells comprising bypass diodes integrated or directly associated with the devices H01L 31/0443; photovoltaic modules composed of a plurality of thin film solar cells deposited on the same substrate H01L 31/046)

**Definition statement**

This place covers:

- Single discrete photovoltaic cells integrated or directly associated with one or more electric components in or on the same substrate, e.g. single thin film photovoltaic cell with integrated bypass diode.
- Devices consisting of PV cells and other semiconductor components, e.g. transistors, on a common substrate, typically PV cells being used as an energy source to drive the other semiconductors.
- Examples:

![Diagram](image.png)

**FIG. 1**

211
References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photovoltaic modules or arrays of single photovoltaic cells comprising</td>
<td>H01L 31/0443</td>
</tr>
<tr>
<td>bypass diodes integrated or directly associated with the devices</td>
<td></td>
</tr>
<tr>
<td>Photovoltaic modules composed of a plurality of thin film solar cells</td>
<td>H01L 31/046</td>
</tr>
<tr>
<td>deposited on the same substrate</td>
<td></td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuitry connections of bypass diodes in solar</td>
<td>H01L 31/05</td>
</tr>
<tr>
<td>panel(s)</td>
<td></td>
</tr>
<tr>
<td>Solar cell structures</td>
<td>H01L 31/06</td>
</tr>
<tr>
<td></td>
<td>H01L 31/078</td>
</tr>
<tr>
<td>Semiconductor organic solar cells</td>
<td>H01L 51/42</td>
</tr>
</tbody>
</table>

H01L 27/144

Devices controlled by radiation

Definition statement

This place covers:

Integration of devices controlled by radiation. These can be for detection purposes, such as photodiode arrays, or for imaging purposes, such as imagers.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Organic semiconductor devices controlled by</td>
<td>H01L 27/305</td>
</tr>
<tr>
<td>radiation</td>
<td></td>
</tr>
<tr>
<td>Radiation detecting components</td>
<td>H01L 31/08</td>
</tr>
</tbody>
</table>
**H01L 27/1443**

{with at least one potential jump or surface barrier}

**Definition statement**

*This place covers:*

Example: integration of a visible and an infrared sensor

**Special rules of classification**

This group is not exclusive with H01L 27/1446

**H01L 27/1446**

{in a repetitive configuration}

**Definition statement**

*This place covers:*

Spatially repeated sensors of the same type such as photodiode arrays, position-sensitive sensors. The repetition can be linear or in form or a matrix, but not for imaging purposes.

Example:
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Imaging devices | H01L 27/146 |

Special rules of classification

This group is not exclusive with H01L 27/1443.

The spatial repetition should not be for imaging purposes.

H01L 27/146

Imager structures

Definition statement

This place covers:
Inorganic semiconductor imaging devices

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Optical filters | G02B 5/20 |
| Waveguides | G02B 6/00 |
| Details of semiconductor imagers (for television systems) | H04N 3/14 |
| Control circuit arrangements for driving solid state imagers | H04N 5/335 |

Special rules of classification

Imaging devices having components using inorganic materials only are classified in H01L 27/146.

Imaging devices having components using organic materials or a combination of organic materials and other materials are classified in H01L 27/307.

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

<p>| Active pixel sensor (APS) | Sensor comprising pixel amplification means, e.g. a transistor as source follower |
| Aperture ratio | Ratio between light sensitive area of a pixel and the total area occupied by that pixel |
| Backside illumination | Illumination of the imagers from the of the device where the imager circuitry has not been formed |
| Blooming | Spilling over of charges from one pixel to the next one after overexposure |
| Charge coupled device | Architecture of an integrated circuit based on the transport of charge packets by capacitive coupling from one capacitor to the next one |</p>
<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge injection device</td>
<td>Architecture of semiconductor device based on measuring currents induced in MOS capacitors at the moment charge packets are injected into the substrate</td>
</tr>
<tr>
<td>Dark current</td>
<td>Signal generated by the image sensor when the device is in the dark.</td>
</tr>
<tr>
<td>Delay line</td>
<td>Component used to delay an electrical signal over a defined time.</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>Ratio of the largest possible signal (full well capacity of the pixel) divided by the smallest possible signal (background noise) of a sensor.</td>
</tr>
<tr>
<td>Frame-transfer CCD</td>
<td>Two dimensional architecture of a CCD imager that has an analogue memory cell for every pixel below the total array of light sensitive pixels.</td>
</tr>
<tr>
<td>Full-frame CCD</td>
<td>Two dimensional architecture of a CCD imager transferring collected charge directly to readout.</td>
</tr>
<tr>
<td>Integration time</td>
<td>Time that an imager is collecting charges (photon generated and/or dark current generated).</td>
</tr>
<tr>
<td>Interlaced scanning</td>
<td>Scanning mode in which only part (odd or even lines) of the lines of the image are captured in an exposure period.</td>
</tr>
<tr>
<td>Interline-transfer CCD</td>
<td>Two dimensional architecture of a CCD imager wherein each photodiode has a parallel CCD storage region covered by an opaque mask. After image data has been collected and transferred to the adjacent CCD storage region charge is CCD-shifted vertically to the readout IC.</td>
</tr>
<tr>
<td>Overflow drain</td>
<td>Doped region to extract undesired charge resulting from blooming.</td>
</tr>
<tr>
<td>Passive pixel sensor</td>
<td>Pixels comprising per pixel only a photodiode or a photodiode and an addressing transistor.</td>
</tr>
<tr>
<td>Photoconductor</td>
<td>Material changing its conductivity when light impinges on it. The delta in conductivity is measured and the incoming radiation calculated in imagers.</td>
</tr>
<tr>
<td>TDI-type CCD-Imager</td>
<td>Time delay and integration (TDI) is a type of CCD wherein a TDI clock is used to synchronize the movement of charged packets in a CCD with that of another movement.</td>
</tr>
<tr>
<td>Wafer level processing</td>
<td>Processing of several semiconductor devices in a single wafer in the same processing cycle.</td>
</tr>
</tbody>
</table>

**Synonyms and Keywords**

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Synonym</th>
</tr>
</thead>
<tbody>
<tr>
<td>APS</td>
<td>Active pixel sensor</td>
</tr>
<tr>
<td>CCD</td>
<td>Charge coupled device</td>
</tr>
<tr>
<td>PPS</td>
<td>Passive pixel sensor</td>
</tr>
</tbody>
</table>
H01L 27/14601

{Structural or functional details thereof}

Definition statement

This place covers:

Details of organic semiconductor imaging structures such as encapsulations, geometry of disposition of passive and active elements, lenses, isolation, etc, whenever they are specific for semiconductor imaging devices, i.e. they solve problems specific to semiconductor imaging devices.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Encapsulation of integrated circuits  H01L 23/28

H01L 27/14603

{Special geometry or disposition of pixel-elements, address-lines or gate-electrodes}

Definition statement

This place covers:

The disposition of the elements within the pixel, such as the transfer, driving, reset transistors, capacitor, photodetector. Also covered are the disposition of electrodes and wiring lines such as the power, bit and data lines. Disposition of the different doped regions within the pixel also fall within the scope of the definition of this subclass.

Examples:

FIG. 8
H01L 27/14605

{Structural or functional details relating to the position of the pixel elements, e.g. smaller pixel elements in the center of the imager compared to pixel elements at the periphery}

Definition statement

This place covers:

Example:
H01L 27/14607

{Geometry of the photosensitive area}

Definition statement

This place covers:

Only geometrical issues of the photosensitive area.

References

Limiting references

This place does not cover:

Details of an APS photosensitive area such as doping or depth

H01L 27/1461

H01L 27/14609

{Pixel-elements with integrated switching, control, storage or amplification elements (scanning details of imagers H04N 3/15; circuitry of imagers H04N 5/369)}

Definition statement

This place covers:

Active pixel sensors [APS], i.e. sensors having in each pixel a photodetecting element and amplifications means within the pixel. Very often CMOS technology is used.
Example:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Scanning details of imagers                  | H04N 5/335 |
| Circuitry of imagers                        | H04N 5/369 |

H01L 27/1461

{characterised by the photosensitive area}

Definition statement

This place covers:

An APS wherein the photosensitive area is characterised by its doping, depth, etc.
Example:

References

Limiting references

This place does not cover:

Only geometrical (i.e., layout) aspects of a photosensitive area in imagers

H01L 27/14607

H01L 27/14612

{involving a transistor}

Definition statement

This place covers:

APS-imagers wherein the invention concerns a specific feature of at least one of the transistor within the unit cell (transfer transistor, reset transistor, source follower,...).
H01L 27/14614
{having a special gate structure}

Definition statement

This place covers:

Example:

US 2011/241080
H01L 27/14616
{characterised by the channel of the transistor, e.g. channel having a doping gradient}

Definition statement
This place covers:
Example:

H01L 27/14618
{Containers}

Definition statement
This place covers:
Containers and encapsulations specially adapted for imagers
Example:
References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Containers of integrated circuits in general | H01L 23/02 |
| Encapsulation of integrated circuits in general | H01L 23/28 |

H01L 27/1462
{Coatings}

Definition statement
This place covers:
Any kind of coatings within the imager (e.g. interlayer dielectric (ILD), antireflective coatings (ARC)).

Example:

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Coatings | C23C 14/00 |
| Optical filters | G02B 5/20 |

H01L 27/14621
{Colour filter arrangements}

Definition statement
This place covers:
arrangement of color filters, e.g. Bayer pattern
Examples:

**FIG. 9**

**FIG. 7**

**H01L 27/14623**

{Optical shielding}

**Definition statement**

*This place covers:*

Examples:

**FIG. 1B**

**References**

**Limiting references**

*This place does not cover:*

| Shielding in CCD-type imagers | H01L 27/14818 |
H01L 27/14625
{Optical elements or arrangements associated with the device}

Definition statement

This place covers:
Optical elements in devices such as lenses, reflectors, light guiding structures within the device. Such
devices include, but are not limited to, CCD-imagers.

Example of an optical element:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Lenses</th>
<th>G02B 3/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photonic crystals</td>
<td>G02B 6/1225</td>
</tr>
</tbody>
</table>
H01L 27/14627
{Microlenses}

Definition statement
This place covers:
Example:

H01L 27/14629
{Reflectors}

Definition statement
This place covers:
Elements reflecting light towards the light detecting portion
Example:
H01L 27/1463
{Pixel isolation structures}

Definition statement

This place covers:
Electrical or thermal isolation structures between pixels.

H01L 27/14632
{Wafer-level processed structures}

Definition statement

This place covers:
Structures processed at a wafer level.

Example:

![Diagram](image.png)

Fig. 5

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Manufacture thereof | H01L 27/14687 |

H01L 27/14634
{Assemblies, i.e. Hybrid structures}

Definition statement

This place covers:
Image sensor in one substrate connected to its driving IC in another substrate.
Example:

References

Limiting references

This place does not cover:

| Hybrid-type infrared imagers                  | H01L 27/1465 |
| Hybrid-type X-ray imagers                    | H01L 27/1466 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Interconnect structures                     | H01L 27/14636 |
| Hybrid Infrared CCD or CID imagers          | H01L 27/14881 |
H01L 27/14636
{Interconnect structures}

Definition statement
This place covers:
Structures to connect e.g. one imaging substrate with its driving substrate, or an image sensor with the external driving circuitry, or special connections within the device.

FIG. 2

H01L 27/14638
{Structures specially adapted for transferring the charges across the imager perpendicular to the imaging plane}

Definition statement
This place covers:
Imagers having the circuitry beneath the photosensitive area whenever special arrangements are made to transfer the charges from the sensor to the circuitry.

H01L 27/1464
{Back illuminated imager structures}

Definition statement
This place covers:
Imagers wherein light impinges from the surface of the semiconductor wafer opposite to the surface where the imaging structure has been created.
Example:

H01L 27/14641

{Electronic components shared by two or more pixel-elements, e.g. one amplifier shared by two pixel elements}

Definition statement

This place covers:

Components (doped regions, transistors, lines) shared by adjacent pixels.

Example:
H01L 27/14643
{Photodiode arrays; MOS imagers}

**Definition statement**

*This place covers:*
Photodiode arrays for imaging purposes and MOS imagers.

H01L 27/14645
{Colour imagers}

**Definition statement**

*This place covers:*
Imagers with pixels each for a primary colour, e.g. RGB, e.g. achieved by means of filters.

**References**

*Limiting references*

*This place does not cover:*

| Colour imagers having photoconductive layer | H01L 27/14667 |

H01L 27/14647
{Multicolour imagers having a stacked pixel-element structure, e.g. npn, npnnpn or MQW elements}

**Definition statement**

*This place covers:*
Colour imager with stacked configuration, such as a multiple pn-junction stack each to detect a colour.

Example:
H01L 27/14649

{Infra-red imagers}

**Definition statement**

*This place covers:*

Imagers for sensing infrared radiation

**References**

**Limiting references**

*This place does not cover:*

- Infrared imagers having photoconductive layer

---

H01L 27/1465

{of the hybrid type}

**Definition statement**

*This place covers:*

Imagers for sensing infrared radiation having an infrared sensor in a substrate and the driving circuitry in a separate substrate both being connected together.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Hybrid type imagers in general</th>
<th>H01L 27/14634</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect structures</td>
<td>H01L 27/14636</td>
</tr>
<tr>
<td>Hybrid type X-ray imagers</td>
<td>H01L 27/14661</td>
</tr>
<tr>
<td>Infrared imagers having photoconductive layer</td>
<td>H01L 27/14669</td>
</tr>
</tbody>
</table>

---

H01L 27/14652

{Multispectral infra-red imagers, having a stacked pixel-element structure, e.g. npn, npnnpn or MQW structures}

**Definition statement**

*This place covers:*

Infrared imagers having generally a stack: LWIR, MWIR, SWIR. The structure is generally similar to that in H01L 27/14647 but for sensing infrared radiation.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Stacked colour imagers                             | H01L 27/14647 |

**H01L 27/14654**

**{Blooming suppression}**

**Definition statement**

*This place covers:*

Structural arrangements to suppress blooming (see glossary of terms in H01L 27/146) such as overflow drains.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Blooming suppression in imagers having photoconductive layer | H01L 27/14672 |

**H01L 27/14656**

**{Overflow drain structures}**

**Definition statement**

*This place covers:*

Vertical and horizontal overflow drains

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Overflow drains in imagers having photoconductive layer | H01L 27/14674 |

**H01L 27/14658**

**{X-ray, gamma-ray or corpuscular radiation imagers (measuring X-, gamma- or corpuscular radiation G01T 1/00)}**

**Definition statement**

*This place covers:*

Imagers for sensing X-ray, G-rays or corpuscular radiation

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| X-ray imagers having photoconductive layer | H01L 27/14676 |
| Measuring X-, gamma- or corpuscular radiation | G01T 1/00 |
H01L 27/14659
{Direct radiation imagers structures}

Definition statement
This place covers:
The semiconductor layers convert directly the incoming radiation into charges, without need of a scintillator

H01L 27/14661
{of the hybrid type}

Definition statement
This place covers:
Imagers for sensing X-ray, gamma-ray or corpuscular radiation having an infrared sensor in a substrate and the driving circuitry in a separate substrate both being connected together.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Hybrid type imagers in general</th>
<th>H01L 27/14634</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect structures</td>
<td>H01L 27/14636</td>
</tr>
<tr>
<td>Hybrid type infrared imagers</td>
<td>H01L 27/1465</td>
</tr>
</tbody>
</table>

H01L 27/14663
{Indirect radiation imagers, e.g. using luminescent members}

Definition statement
This place covers:
This group comprises X-ray radiation imagers having a scintillator (an ionic solid) which converts incoming X-ray radiation into visible light. The detector detects the visible light converted by the scintillator (also called phosphor).

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Measuring X-ray radiation with a scintillation-diode combination | G01T 1/2018 |
H01L 27/14665
{Imagers using a photoconductor layer}

Definition statement
This place covers:
These imagers work on the principle that the photoconductive layer changes its conductivity with the incoming radiation. The change in conductivity is measured and the incoming radiation derived.

H01L 27/1467
{of the hybrid type}

Definition statement
This place covers:
Photoconductive imagers having a substrate with the imagers formed therein and another connected thereto with the electronic circuit.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Hybrid type imagers in general | H01L 27/14634 |
| Interconnect structures        | H01L 27/14636 |
| Hybrid type infrared imagers   | H01L 27/1465  |
| Hybrid type X-ray imagers      | H01L 27/14661 |

H01L 27/14672
{Blooming suppression}

References
Limiting references
This place does not cover:

| Blooming suppression in PD- or MOS-imagers | H01L 27/14654 |

H01L 27/14674
{Overflow drain structures}

References
Limiting references
This place does not cover:

| Overflow structures in PD- or MOS-imagers | H01L 27/14656 |
H01L 27/14676
{X-ray, gamma-ray or corpuscular radiation imagers (measuring X-, gamma- or corpuscular radiation G01T 1/00)}

References

Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>X-ray detecting PD- or MOS-imagers</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 27/14658</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Measuring X-, gamma- or corpuscular radiation</th>
</tr>
</thead>
<tbody>
<tr>
<td>G01T 1/00</td>
</tr>
</tbody>
</table>

H01L 27/14678
{Contact-type imagers}

Definition statement
This place covers:
Imagers having integrated light sources, wherein the light emitted from the integrated light source is reflected on the object to be detected and enters the imagers. Examples thereof are scanning heads, photocopier heads or fingerprint detectors

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>CID-type CCD-imagers wherein the object to be imaged in contact with the sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 27/14862</td>
</tr>
<tr>
<td>Fingerprint recognition</td>
</tr>
<tr>
<td>G06K 9/00</td>
</tr>
<tr>
<td>Scanning heads</td>
</tr>
<tr>
<td>H04N 1/00</td>
</tr>
</tbody>
</table>

H01L 27/14683
{Processes or apparatus peculiar to the manufacture or treatment of these devices or parts thereof (not peculiar thereto H01L 21/00)}

Definition statement
This place covers:
Multistep processes specially adapted for the manufacture of imagers
H01L 27/14685
{Process for coatings or optical elements}

Definition statement
This place covers:
Formation of coatings (antireflective coatings, filters, shielding) as well as microlenses and other optical elements.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Coatings</th>
<th>H01L 27/1462</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical elements</td>
<td>H01L 27/14625</td>
</tr>
<tr>
<td>Coatings in general</td>
<td>C23C 14/00</td>
</tr>
<tr>
<td>Lenses</td>
<td>G02B 3/00</td>
</tr>
<tr>
<td>Optical filters</td>
<td>G02B 5/20</td>
</tr>
<tr>
<td>Photonic crystals</td>
<td>G02B 6/1225</td>
</tr>
</tbody>
</table>

H01L 27/14687
{Wafer level processing}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Wafer level imagers               | H01L 27/14634 |

H01L 27/14689
{MOS based technologies}

Definition statement
This place covers:
Manufacturing process of imagers using technology of the MOS-type

H01L 27/1469
{Assemblies, i.e. hybrid integration}

Definition statement
This place covers:
Manufacture of hybrid-type imagers.

The manufacture is in general for any kind of hybrid-type imagers (see types below under informative references).
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Hybrid-type imagers in general</th>
<th>H01L 27/14634</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid-type infrared imagers</td>
<td>H01L 27/1465</td>
</tr>
<tr>
<td>Hybrid-type X-ray imagers</td>
<td>H01L 27/14661</td>
</tr>
<tr>
<td>Hybrid-type infrared photoconductive</td>
<td>H01L 27/1467</td>
</tr>
</tbody>
</table>

H01L 27/148

Charge coupled imagers {individual charge coupled devices H01L 29/765}

Definition statement

This place covers:
CCD-type imagers

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Charge coupled devices per se</th>
<th>H01L 29/765</th>
</tr>
</thead>
</table>

H01L 27/14812

{Special geometry or disposition of pixel-elements, address lines or gate-electrodes}

Definition statement

This place covers:
Lines and electrodes layouts, disposition of pixel elements such as the transfer gates, photodetectors of CCD-type imagers.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Circuit arrangements for driving solid state imagers</th>
<th>H04N 5/335</th>
</tr>
</thead>
</table>

H01L 27/14818

{Optical shielding}

Definition statement

This place covers:
Shielding specific to CCDs.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Shielding in general for imagers | H01L 27/14623 |

**H01L 27/14825**

{Linear CCD imagers}

**Definition statement**

*This place covers:*

CCD-imagers having a linear arrangement of the pixels, e.g. as fax heads or photocopiers

**H01L 27/14831**

{Area CCD imagers}

**Definition statement**

*This place covers:*

Pixels in a 2D matrix form

**H01L 27/14837**

{Frame-interline transfer}

**Definition statement**

*This place covers:*

Combination of interline transfer with a frame transfer (see hereafter).

Each photodiode has a parallel CCD region which shifts charge vertically to a storage 2D matrix (one storage pixel per one photosensitive pixel). The charges stored in the storage matrix are then read out.

Example:
H01L 27/14843
{Interline transfer}

Definition statement

This place covers:
Each photodiode has a parallel CCD storage region covered by an opaque mask. After image data has been collected and transferred to the adjacent CCD storage region charge is CCD-shifted vertically to the readout IC.

H01L 27/1485
{Frame transfer}

Definition statement

This place covers:
The photosensitive 2D array has adjacent a 2D storage area, having a storage pixel per photosensitive pixel. The charges collected are transferred in parallel to the storage area for readout.

Example:

H01L 27/14856
{Time-delay and integration}

Definition statement

This place covers:
Time delay and integration type CCD imager. Time delay and integration (TDI) relates to details of CCD imaging arrays operating in a TDI mode (the pixel clock rate must be matched to the image velocity).

H01L 27/14862
{CID imagers}

Definition statement

This place covers:
CID place the object to be imaged in contact with the sensor and use, typically, LEDs for the illumination of the object to be imaged.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Contact-type imagers | H01L 27/14678 |

H01L 27/15

including semiconductor components with at least one potential-jump barrier or surface barrier specially adapted for light emission \{(monolithically integrated components including semiconductor laser components H01S 5/026)\}

Definition statement

This place covers:

Devices consisting of a plurality of monolithically integrated inorganic semiconductor light emitting diode (LED) components or consisting of inorganic semiconductor LED components monolithically integrated with other semiconductor components.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Hybrid assemblies of a plurality of individual LED devices | H01L 25/075 |
| Hybrid assemblies of LED devices with other semiconductor devices | H01L 25/167 |
| Displays having an organic semiconductor light emitting material or comprising a mixture of an inorganic and an organic semiconductor light emitting material (OLED displays) | H01L 27/32 |
| LED devices | H01L 33/00 |
| LED devices with a plurality of light emitting regions | H01L 33/08 |
| Printing devices using LED arrays as print heads | B41J 2/45 |
| LCD displays | G02F 1/13 |
| Devices consisting of semiconductor laser diode components monolithically integrated with other components | H01S 5/026 |

H01L 27/16

including thermoelectric components with or without a junction of dissimilar materials; including thermomagnetic components (using the Peltier effect only for cooling of semiconductor or other solid state devices H01L 23/38)

Definition statement

This place covers:

This group covers thermoelectric generators using the Seebeck effect to convert heat to electrical energy, thermoelectric coolers using the Peltier effect to create a temperature gradient and the related devices.
Devices monolithically integrating components individually covered by groups H01L 35/00 or H01L 37/00, e.g. Seebeck or Peltier components, either with components of the same kind, e.g. thermocouple arrays, or with components of a different kind, e.g. semiconductor diodes, transistors.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Peltier effect devices only for cooling of semiconductor or other solid state devices | H01L 23/38 |
| Infrared imagers based on semiconductor devices, e.g. - photodiodes - photoconductors - CCDs- using organic semiconductors | H01L 27/14649, H01L 27/14669, H01L 27/14875, H01L 27/30 |
| Thermoelectric devices comprising a junction of dissimilar materials | H01L 35/00 |
| Measuring thermal radiation - using thermocouples - using resistors, e.g. bolometers- using capacitors, e.g. pyroelectric sensors | G01J 5/00, G01J 5/12, G01J 5/20, G01J 5/34 |
| Measuring temperature based on the use of electric or magnetic elements directly sensitive to heat | G01K 7/00 |
| Generators or motors not provided for elsewhere | H02N 11/00 |

Special rules of classification

Classification of relevant details of the individual thermoelectric or thermomagnetic devices such as structure, materials, or manufacturing steps is mandatory and needs to be done in groups H01L 35/00 or H01L 37/00, by allocating at least Indexing Code symbols thereof.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEG</td>
<td>thermoelectric generator</td>
</tr>
<tr>
<td>TEC</td>
<td>thermoelectric cooler</td>
</tr>
<tr>
<td>TEM</td>
<td>thermoelectric module</td>
</tr>
<tr>
<td>ZT</td>
<td>dimensionless figure of merit</td>
</tr>
</tbody>
</table>

H01L 27/18

including components exhibiting superconductivity

Definition statement

This place covers:

Devices monolithically integrating components individually covered by main group H01L 39/00, i.e. superconductive components, either with components of the same kind, e.g. Josephson junction arrays, or with components of a different kind, e.g. semiconductor diodes, transistors.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Quantum computers | G06N 10/00 |
Digital memories \( \text{G11C} \ 11/44 \)
Electronic switching circuits \( \text{H03K} \ 17/92 \)
Logic circuits \( \text{H03K} \ 19/195 \)

**Special rules of classification**

Classification of relevant details of the individual superconductive devices such as structure, materials, or manufacturing steps is mandatory and needs to be done in group \( \text{H01L} \ 39/00 \), by allocating at least Indexing Code symbols thereof.

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JJ</td>
<td>Josephson junction</td>
</tr>
<tr>
<td>RSFQ</td>
<td>Rapid single flux quantum</td>
</tr>
</tbody>
</table>

**H01L 27/20**

including piezo-electric components; including electrostrictive components; including magnetostrictive components

**Definition statement**

*This place covers:*

Devices monolithically integrating components individually covered by group \( \text{H01L} \ 41/00 \), e.g. piezoelectric [PE] or magnetostrictive [MS] components, either with components of the same kind, e.g. actuator arrays, or with components of a different kind, e.g. semiconductor diodes, transistors

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ultrasonic transducer arrays</td>
<td>( \text{B06B} \ 1/0622 )</td>
</tr>
<tr>
<td>Ink-jet print heads</td>
<td>( \text{B41J} \ 2/14233 )</td>
</tr>
<tr>
<td>Digital memories, e.g. FRAMs</td>
<td>( \text{G11C} \ 11/22 )</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Classification of relevant details of the individual PE or MS devices such as structure, materials, or manufacturing steps is mandatory and needs to be done in group \( \text{H01L} \ 41/00 \), by allocating at least Indexing Code symbols thereof.

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAW</td>
<td>Bulk acoustic wave</td>
</tr>
<tr>
<td>SAW</td>
<td>Surface acoustic wave</td>
</tr>
<tr>
<td>MS</td>
<td>Magnetostrictive</td>
</tr>
<tr>
<td>PE</td>
<td>Piezoelectric or electrostrictive</td>
</tr>
</tbody>
</table>
**H01L 27/22**

including components using galvano-magnetic effects, e.g. Hall effects; using similar magnetic field effects

**Definition statement**

*This place covers:*

Devices monolithically integrating components individually covered by main group **H01L 43/00**, e.g. magneto-resistive components, either with components of the same kind, e.g. arrays, or with components of a different kind, e.g. semiconductor diodes, transistors

Further classification information:

**H01L 27/222**

covers MRAM structures comprising multiple (arrayed) MR components, e.g. bit or word lines arrangements.

**H01L 27/224**

covers MRAM structures comprising MR components and two-terminal selection components, e.g. semiconductor diodes, MIM switches.

**H01L 27/226**

covers MRAM structures comprising MR components and selection components having more than two terminals, e.g. bipolar transistors.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Measuring magnetic quantities; Magnetometers</th>
<th>G01R 33/06</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronic switching circuits- Logic circuits</td>
<td>H03K 17/90, H03K 19/18</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Classification of relevant details of the individual devices such as structure, materials, or manufacturing steps is mandatory and needs to be done in group **H01L 43/00**, by allocating at least Indexing Code symbols thereof.

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>GMR</th>
<th>Giant magnetoresistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>Magnetoresistance</td>
</tr>
<tr>
<td>MTJ</td>
<td>Magnetic tunnel junctionMR tunnel junction</td>
</tr>
<tr>
<td>TMR</td>
<td>Tunnel magnetoresistance</td>
</tr>
<tr>
<td>MRAM</td>
<td>Magnetoresistive RAM</td>
</tr>
</tbody>
</table>
H01L 27/24

including solid state components for rectifying, amplifying or switching without a potential-jump barrier or surface barrier, {e.g. resistance switching non-volatile memory structures}

Definition statement

This place covers:
Devices monolithically integrating components individually covered by main group H01L 45/00, e.g. bulk switching components, either with components of the same kind, e.g. arrays, or with components of a different kind, e.g. semiconductor diodes, transistors

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Resistor or anti-fuse arrays - integrated with junction diodes- integrated with transistors | H01L 27/101, H01L 27/1021, H01L 27/112 |
| Devices integrating bulk negative differential resistance components, e.g. Gunn elements | H01L 27/26 |
| RRAM digital memories | G11C 13/0002 |
| Dielectric breakdown anti-fuse memories | G11C 17/16 |

Special rules of classification

Classification of relevant details of the individual bulk switching devices such as structure, materials, or manufacturing steps is mandatory and needs to be done in group H01L 45/00, by allocating at least Indexing Code symbols thereof.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

| CBRAM | Conductive bridging RAM |
| PCM | Phase change materialPhase change memory |
| PRAM | Phase change RAM |
| PCRAM | Resistance switching RAM |

H01L 27/26

including bulk negative resistance effect components

Definition statement

This place covers:
Devices monolithically integrating components individually covered by main group H01L 47/00, e.g. Gunn effect components, either with components of the same kind, e.g. arrays, or with components of a different kind, e.g. semiconductor diodes, transistors
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Devices integrating bulk bi-stable switching components, e.g. RRAM cells | H01L 27/24 |
| Digital memories | G11C 11/39 |
| Electronic switching circuits | H03K 17/70 |

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

| NDR | Negative differential resistance |

H01L 27/28

including components using organic materials as the active part, or using a combination of organic materials with other materials as the active part

Definition statement

This place covers:

Semiconductor devices wherein the active layer or part of it is made of an organic material (or combination organic and inorganic). This covers organic ICs, organic solar cells, organic imagers, organic displays.

H01L 27/281

{Integrated circuits having a three-dimensional layout}

Definition statement

This place covers:

Monolithically stacked organic semiconductor devices

References

Limiting references

This place does not cover:

| Monolithically stacked light sensitive devices | H01L 27/302 |
| Integration of organic light emitting devices | H01L 27/32 |
**H01L 27/283**

*{comprising components of the field-effect type}*

**Definition statement**

*This place covers:*
Integration of an OTFT with another device falling under the definition of H01L, e.g. inverters:

![Diagram](image)

EP2006929

**H01L 27/285**

*{Integrated circuits with a common active layer, e.g. cross point devices}*

**Definition statement**

*This place covers:*
Cross point devices, e.g.:

![Diagram](image)

Figure 1
EP2096672.

References

Limiting references

This place does not cover:

| Resistance random access memory [RRAM] elements comprising cells based on organic memory material | G11C 13/0014 |
| Digital stores using elements whose operation depends on a chemical change | G11C 13/02 |

H01L 27/286

{with an active region comprising an inorganic semiconductor}

Definition statement

This place covers:

Combination of an organic TFT (e.g. pentacene) with an inorganic TFT (e.g. a-Si:H) :

US 6528816

H01L 27/288

{Combination of organic light sensitive components with organic light emitting components, e.g. optocoupler}

Definition statement

This place covers:

Example:
combination of an organic phototransistor with an OLED:

![Integrated OLED diagram]

WO2008042859

References

Limiting references

This place does not cover:

| Integration of an OLED display with a photo sensor. | H01L 27/3239 |
| Integration of a photodiode in each cell of an OLED display to measure the emission of the OLED and to adjust the intensity accordingly | H01L 27/3269 |

H01L 27/30

with components specially adapted for sensing infra-red radiation, light, electromagnetic radiation of shorter wavelength, or corpuscular radiation; with components specially adapted for either the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation {(combination of organic light sensitive components with organic light emitting components, e.g. optocoupler H01L 27/288)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Integration of inorganic energy conversion devices | H01L 27/142 |
| Integration of inorganic devices controlled by radiation, e.g. inorganic CCDs | H01L 27/144 |
**H01L 27/301**

*{Energy conversion devices}*

**Definition statement**

*This place covers:*

Organic solar cell modules; assembly of organic light sensitive devices specially adapted for conversion of light into electrical energy.

**H01L 27/302**

*{comprising multiple junctions, e.g. tandem cells}*

**Definition statement**

*This place covers:*

Organic tandem solar cells

---

**Diagram**

![Solar cell diagram](WO02101838)
**H01L 27/304**

{in form of a fiber or a tube, e.g. photovoltaic fibers}

**Definition statement**

*This place covers:*

Fibres based on organic photovoltaic cells.

---

**H01L 27/305**

{Devices controlled by radiation}

**Definition statement**

*This place covers:*

Organic light sensitive devices specially adapted for the measuring of light intensity or light colour.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Investigating or analysing materials by the use of optical means</th>
<th>G01N 21/00</th>
</tr>
</thead>
</table>
H01L 27/307

{Imager structures}

Definition statement
This place covers:
Imager structures based on organic light sensitive devices.

US2007120045

H01L 27/308

{Devices specially adapted for detecting X-ray radiation (measuring X-radiation G01T 1/00)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Measuring X-radiation | G01T 1/00 |

H01L 27/32

with components specially adapted for light emission, e.g. flat-panel displays using organic light-emitting diodes [OLED] ((combination of organic light sensitive components with organic light emitting components, e.g. optocoupler H01L 27/288))

Definition statement
This place covers:
Arrangements of OLEDs such as OLED displays or OLED integrated with another component
### References

#### Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assemblies of OLEDs</td>
<td>H01L 25/048</td>
</tr>
<tr>
<td>Single step processes for manufacturing OLED devices</td>
<td>H01L 51/0001</td>
</tr>
<tr>
<td>Organic semiconducting materials for OLEDs</td>
<td>H01L 51/0032</td>
</tr>
<tr>
<td>Single OLEDs</td>
<td>H01L 51/50</td>
</tr>
<tr>
<td>Aspects of electrodes</td>
<td>H01L 51/5203</td>
</tr>
<tr>
<td>Aspects of encapsulation</td>
<td>H01L 51/5237</td>
</tr>
<tr>
<td>Aspects of light extraction</td>
<td>H01L 51/5262</td>
</tr>
<tr>
<td>Aspects of contrast improvement</td>
<td>H01L 51/5281</td>
</tr>
<tr>
<td>Multistep processes for the manufacture of OLED display</td>
<td>H01L 51/56</td>
</tr>
<tr>
<td>Circuit arrangements for driving OLED displays</td>
<td>G09G 3/3208</td>
</tr>
</tbody>
</table>

#### Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD-displays</td>
<td>G02F 1/133</td>
</tr>
<tr>
<td>Plasma displays</td>
<td>H01J 11/00</td>
</tr>
<tr>
<td>Inorganic LED-displays</td>
<td>H01L 27/156</td>
</tr>
<tr>
<td>FE-displays</td>
<td>H01J 31/00</td>
</tr>
<tr>
<td>2D-radiation sources</td>
<td>H05B 33/12</td>
</tr>
<tr>
<td>Surface treatment of glass substrates by at least two coatings</td>
<td>C03C 17/34</td>
</tr>
<tr>
<td>Optical coatings</td>
<td>G02B 1/10</td>
</tr>
<tr>
<td>Chemical coating by decomposition of gaseous compounds</td>
<td>C23C 16/00</td>
</tr>
</tbody>
</table>

#### Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>OLED display</td>
<td>Organic light emitting diode display</td>
</tr>
<tr>
<td>TOLED display</td>
<td>Transparent OLED display</td>
</tr>
<tr>
<td>AMOLED display</td>
<td>Active matrix OLED display</td>
</tr>
<tr>
<td>PMOLED display</td>
<td>Passive matrix OLED display</td>
</tr>
<tr>
<td>OTFT array</td>
<td>Organic thin film transistor array</td>
</tr>
<tr>
<td>TFT array</td>
<td>Thin film transistor array</td>
</tr>
<tr>
<td>CCM</td>
<td>Colour changing medium</td>
</tr>
<tr>
<td>RGB</td>
<td>Red Green Blue</td>
</tr>
<tr>
<td>RGBW</td>
<td>Red Green Blue White</td>
</tr>
</tbody>
</table>
**H01L 27/3202**

{OLEDs electrically connected in parallel}

**Definition statement**

*This place covers:*

Arrangements of OLEDs connected in parallel or series and parallel

**Examples**

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>OLED logos</th>
<th>H01L 27/3239</th>
</tr>
</thead>
</table>

US 2004/233140

US 2007/222746
**H01L 27/3204**

{**OLEDs electrically connected in series**}

**Definition statement**

*This place covers:*

Arrangements of OLEDs connected in series or series and parallel frequently used for illumination or fixed information purposes.

**Examples**

![Diagram](image)

EP 1 970 960 A2

US2008218061

**References**

**Limiting references**

*This place does not cover:*

| Stacked OLEDs | H01L 27/3209, H01L 51/5278 |

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| OLED logos | H01L 27/3239 |
**H01L 27/3206**

*Muti-colour light emission*

**Definition statement**

*This place covers:*

In the headgroup H01L 27/3206, multi-colour OLED displays in which the RGB sub-pixels are formed with an identical emissive layer making use of resonant cavity (adapting the optical path length).

Example:

EP1672962:

The sub-pixels each have an identical emissive layer, the optical distance of the resonant section between the reflectors is adjusted for the generation of RGB sub-pixels.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Resonant cavities | H01L 51/5265 |

**Special rules of classification**

The class H01L 51/5265 is given in combination with H01L 27/3206 for multi-colour OLED displays in which the RGB sub-pixels are formed with an identical emissive layer making use of resonant cavity (adapting the optical path length).

If in addition to the resonant cavity, a colour filter is used for further light purification, the Indexing Code-code H01L 27/322 should be added.

**H01L 27/3209**

*{using stacked OLED}*

**Definition statement**

*This place covers:*

Stack of OLEDs for multi-colour emission.
Example:

In this example the group symbol H01L 25/048 is additionally given for the lamination (formed on different substrates)

In this example the group symbol H01L 51/504 is additionally given for the stack 212 of emissive layers in contact

References

Limiting references

This place does not cover:

| Stack of RGB emissive layers in contact                       | H01L 51/5036 |
| Stacked arrangements of OLEDs emitting the same colour       | H01L 51/5278 |
Informative references
Attention is drawn to the following places, which may be of interest for search:

| OLEDs formed on different substrates | H01L 25/048 |

H01L 27/3211
{using RGB sub-pixels}

Definition statement

This place covers:
Arrangements wherein Red Green and Blue sub-pixels comprise a layer emitting in the corresponding primary colour.

Examples

![Diagram of OLED structure]

In this example, the group symbol H01L 51/5278 is additionally given for the stacked arrangement of OLEDs emitting the same colour (green and blue sub-pixels)

References

Limiting references

This place does not cover:

| Displays with the same emissive layer for the sub-pixels (e.g. white or blue) and making use of filters or colour changing media for RGB colour emission | H01L 27/322 |
Special rules of classification

An Indexing Code [H01L 27/322] is to be given if the filters are used in addition to RGB emissive layers.

In this example the group symbol [H01L 51/5278] is also given for the stacked formation of the green and blue sub-pixels.

**H01L 27/3213**

{using more than three sub-pixels, e.g. RGBW}

**Definition statement**

*This place covers:*

Arrangements wherein an extra pixel (generally white, but also yellow or from another colour) is used to improve emission efficiency, reduce power consumption or improve lifetime (all related problems).

Example

![Diagram](image)

**H01L 27/3216**

{the areas of RGB sub-pixels being different}

**Definition statement**

*This place covers:*

Multi-colour light emission whereby the sub-pixels have different areas.
Example:

![Diagram of RGB sub-pixels arrangement]

US2012/097933:

**References**

*Limiting references*

*This place does not cover:*

| Light emitting logos | H01L 27/3239 |

**H01L 27/3218**

{characterised by the geometrical arrangement of the RGB sub-pixels}

**Definition statement**

*This place covers:*

Multicolour light emission characterised by the geometrical arrangement of the sub-pixels.

Example:
Definition statement

This place covers:

Arrangements wherein the filters and CCM are used for generation of the RGB sub-pixels. They can be monolithically formed with the light emitting elements or on a separate substrate which is then bonded to the display.
Examples

References

Limiting references

This place does not cover:

| Single OLED with filter or CCM | H01L 51/5036 |

H01L 27/3223

{combined with dummy elements, i.e. non-functional features}

Definition statement

This place covers:

Arrangements having dummy elements. These are elements having no functionality in the display but being therein provided for e.g. manufacturing, or testing.
Examples

EP1209744

Formation of dummy pixels (111') in area B

EP1335431

Dummy electrodes 44b and 45b for testing

**H01L 27/3225**

{OLED integrated with another component (**H01L 27/3223** takes precedence)}

**Definition statement**

*This place covers:*

The OLED is integrated with other components (not forming part of the AMOLED driving circuit) such as a solar cell, an inorganic photodiode, a touch panel an LCD
## References

### Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Integration of an OLED display array with a dummy component</th>
<th>H01L 27/3223</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMOLED (OLED integrated with TFT)</td>
<td>H01L 27/3244</td>
</tr>
<tr>
<td>Dual display</td>
<td>H01L 27/3267,</td>
</tr>
<tr>
<td></td>
<td>H01L 27/3286</td>
</tr>
</tbody>
</table>

### Informative references

Attention is drawn to the following places, which may be of interest for search:

| Backlighting for LCD                                      | G02F 1/1336   |

## H01L 27/3227

{the other component being a light sensitive element, e.g. inorganic solar cell, inorganic photodiode (H01L 27/288 takes precedence)}

### Definition statement

This place covers:

An OLED device integrated with an inorganic light sensitive device

Example

![Diagram](image)

US 2008/054276

100: OLED, 115: photodetector

### References

#### Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Combination of organic light sensitive devices with organic light emitting devices e.g. optocoupler</th>
<th>H01L 27/288</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integration of AMOLED and photosensor(s) to control luminance</td>
<td>H01L 27/3269</td>
</tr>
</tbody>
</table>
H01L 27/323
{the other component being a touch screen}

Definition statement
This place covers:
Integration of an OLED display and a touch screen

Example

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Contact type imagers</th>
<th>H01L 27/14678</th>
</tr>
</thead>
<tbody>
<tr>
<td>Touch panels</td>
<td>G06F 3/00</td>
</tr>
</tbody>
</table>

H01L 27/3232
{the other component being a light modulating element, e.g. electrochromic element, photochromic element, liquid crystal element}

Definition statement
This place covers:
Integration of an OLED device and a light modulating element
Examples

AMOLED combined with an electrophoretic display for light control, e.g. for shielding or control of light transmission

OLED and LCD region integrated
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Backlights for LCD-displays | G02F1/13357 |

H01L 27/3234

{the other component being an imager structure (H01L 27/146 takes precedence)}

Definition statement

This place covers:
Integration of an OLED display with an imager.

Examples

US2010/155578
A1: light emitting regions; A2 light detecting regions

PX11, PX12, PX21, PX22: pixels; 11A, 11B: optoelectronic transducers, they may function either as light emitting elements or light-receiving elements by only changing the method of driving of these optoelectronic transducers

References

Limiting references

This place does not cover:

| Organic semiconductor imagers | H01L 27/307 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Inorganic semiconductor imagers | H01L 27/146 |
| Contact type Inorganic semiconductor imagers | H01L 27/14678 |
H01L 27/3237

{Displays not provided for in group H01L 27/3241 and subgroups, e.g. segment-type displays}

Definition statement

This place covers:

OLED displays not being matrix-type displays, such as 7-segment-type numeric displays:

Further information:

This is a residual group of the matrix-type display group H01L 27/3241.
H01L 27/3239

{Light emitting logos}

Definition statement

This place covers:

Fixed information (shop or trademark logo) OLED display, e.g. formed by patterning the electrodes in the desired form or by modifying electrical properties of regions of the electrodes or of (one of) the active layers between the electrodes.

References

Limiting references

This place does not cover:

| Tiled displays                     | H01L 27/3293 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Illuminated signs                  | G09F 13/00   |
H01L 27/3241

{Matrix-type displays}

Definition statement

This place covers:
Displays having a two-dimensional array of OLED pixels

References

Limiting references

This place does not cover:

| Segment type OLED displays | H01L 27/3237 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Inorganic LED displays | H01L 27/156 |

Special rules of classification

If the display can be either an active and passive matrix display, both groups H01L 27/3244 and H01L 27/3281 are given rather than H01L 27/3241. Groups H01L 27/3295 and H01L 27/3297 are no longer used for classification. Their subject matter is now covered by H01L 27/3244 - H01L 27/3293.

H01L 27/3244

{Active matrix displays}

Definition statement

This place covers:
OLED displays having pixel driving circuitry (such as transistors and capacitors) within the pixel.

Example:

![Diagram of active matrix display](image)

FIG. 1 EP 1 480 272 A2

References

Limiting references

This place does not cover:

| Circuit arrangements for AMOLED displays | G09G 3/3225 |
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multistep processes for AMOLED</td>
<td>H01L 2227/323</td>
</tr>
<tr>
<td>AM-LCD displays</td>
<td>G02F 1/1362</td>
</tr>
</tbody>
</table>

H01L 27/3246
{Banks, i.e. pixel defining layers}

Definition statement
This place covers:
Particular details of the insulating layer that defines and separates the light emitting pixel regions, e.g. material, taper angle:

ILI: pixel defining layer

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Banks in PMOLED displays</td>
<td>H01L 27/3283</td>
</tr>
<tr>
<td>Deposition of organic semiconductor materials using liquid deposition (often using spacers for the deposition of the liquid)</td>
<td>H01L 51/0003</td>
</tr>
</tbody>
</table>

Special rules of classification
If the display device can be either an active or passive matrix display, both the groups H01L 27/3246 AND H01L 27/3283. Group H01L 27/3295 is no longer used for classification.
**H01L 27/3248**

**{Connection of the pixel electrode to the TFT}**

**Definition statement**

*This place covers:*

Particular connection details of the driving TFT to the pixel electrode of the OLED e.g. OLED is formed on same plane as driving TFT. (i.e. not the normal connection of the anode with the TFT via contact hole), cathode is connected with TFT, planarisation layer inside the contact opening

**Examples**

![Diagram of pixel electrode connection](image1)

Pixel electrode 160 extends from drain electrode 125

![Diagram of pixel electrode connection](image2)

One end of the drain electrode 265 is electrically connected with the drain region 220-2, the other end is electrically connected with the pixel electrode
Pixel structure having a plurality of OLEDs connected in series to the TFT

116: pixel electrode, 200: planarisation layer inside contact opening 114

**H01L 27/3251**

{Double substrate, i.e. with OLED and TFT on different substrates}

**Definition statement**

*This place covers:*

Hybrid-type OLED display having the OLED array on a substrate bonded to its driving circuitry on another substrate.
Example:

H01L 27/3253

{Electrical connection of the two substrates}

Definition statement

This place covers:
Particular electrical connection details of the TFT substrate and the OLED substrate.

Examples

US2008/174239

310: substrate with driving circuitry, 320: substrate with OLED array

US2005/127825
132: connecting electrode connected to the TFT, 160: pixel electrode

Tp: driving TFT, 115b: drain electrode, 141: connection electrode, C: contact part

**H01L 27/3255**

{Chiplets}

**Definition statement**

This place covers:

Integrated circuit chiplets bonded to the OLED panel. The chiplets drive the OLED panel.

Example:

**H01L 27/3258**

{Insulating layers formed between TFT elements and OLED elements}

**Definition statement**

This place covers:

Insulating layers formed between TFT elements and OLED elements, which layers can be of any kind. They can be inter alia planarising layers, diffusion barriers, buffer layers, combinations of them.
Examples

27: insulating layer between TFT and OLED elements

Slits in interlayer insulating layer 114, banks are not necessary, improved aperture ratio

**H01L 27/326**

{*special geometry or disposition of pixel-elements*}

**Definition statement**

*This place covers:*

An AMOLED display having special geometry or disposition of the pixel (driving) elements within the pixel, e.g. to improve aperture ratio. Examples of pixel driving elements are transistors, capacitor.
Examples

OLED formed above power line

Special positioning of the OLEDs.
In this example, an additional class (H01L 27/3258) is given for the special shape of the insulating layer between TFTs and OLEDs.

OLED display having a plurality of pixels on the substrate (P1, P2) each having a first region configured to emit light (31) and a second region configured to transmit external light (32). E.g. pixel (driving) elements are not formed in the second region (32).

**H01L 27/3262**

{of TFT}

**Definition statement**

*This place covers:*

An AMOLED display having special geometry or disposition of TFT(s) within the pixel.
Examples:

Height difference is created between upper surfaces of OLED and TFT

References

Limiting references

This place does not cover:

| TFTs and OLEDs formed on different substrates | H01L 27/3251 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| TFT arrays | H01L 27/12 |
| Manufacture of TFT arrays | H01L 27/1214 |
| AMOLED with OTFT | H01L 27/3274 |
Special rules of classification

The present group is directed to TFTs which have certain special properties within the structure of the AMOLED display. TFTs as such are covered by H01L 27/12.

If the gist of the invention concerns only a TFT (and/or its formation) and in the application it is also mentioned that the TFT is used in an AMOLED (also in an AMLCD, etc) then an EC group symbol is given in the TFT-field (H01L 27/12, H01L 27/1214) in combination with the Indexing Code H01L 27/3262.

However if the gist of the invention concerns a TFT within an AMOLED display, for instance the position within the pixel, the formation within the display (combined with H01L 51/56), the use of other common elements (e.g., electrode common with the capacitor's plate, etc., then an EC group symbol is given in H01L 27/3262 and an Indexing Code is given in H01L 27/12 or H01L 27/1214.

The circulation of these documents to examiners working in H01L 27/12 or H01L 27/1214 is mandatory.

H01L 27/3265

{of capacitor}

Definition statement

This place covers:

An AMOLED display having special geometry or disposition of the capacitor within the pixel.

Example:

Special positioning of the capacitor 102

102a,102b: capacitor electrodes; 103g,103s: gate, source electrode of driving TFT
**H01L 27/3267**

{Dual display, i.e. having two independent displays}

**Definition statement**

*This place covers:*

Display emitting different information in its two major surfaces. Generally it comprises two displays stacked on top of another, at least one of the displays is an AMOLED or a single AMOLED display with a double unitary cell emitting in the two main surfaces,

Examples:

In this example, also H01L 25/048 is given for the assembly
Active and passive matrix display combined (H01L 25/048 is given in addition)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Displays on different substrates</th>
<th>H01L 25/048</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMOLED displays side-by-side emitting in the same direction</td>
<td>H01L 27/3225 and H01L 27/3244</td>
</tr>
<tr>
<td>PMOLED displays side-by-side emitting in the same direction</td>
<td>H01L 27/3225 and H01L 27/3281</td>
</tr>
<tr>
<td>PMOLED dual display</td>
<td>H01L 27/3286</td>
</tr>
<tr>
<td>Telephones having more than one display unit</td>
<td>H04M 2250/16</td>
</tr>
</tbody>
</table>

Special rules of classification

Transparent OLED displays having a single light emitting cell emitting in the two main directions of the display are classified elsewhere depending on characterizing feature e.g. H01L 51/5234 (transparent cathode).

H01L 27/3269

{Including photosensors to control luminance}

Definition statement

This place covers:

Arrangements wherein each pixel comprises a photosensor which receives the light emitted from the OLED of that pixel and adjusts its luminance accordingly or a photosensor is used at a display level to measure the intensity of the ambient light and adjust accordingly the overall intensity of the whole OLED display
Examples

Each pixel incorporated with photosensor for optical feedback compensation

Luminance of each OLED is adjusted based on signal from ambient light sensor.

References

Limiting references

This place does not cover:

Integration of organic light sensitive components with organic light emitting devices e.g. Optocouplers

Integration of OLED and inorganic light sensitive element

H01L 27/288

H01L 27/3272

{Shielding, e.g. of TFT}

Definition statement

This place covers:

Shielding of the pixel elements, for instance, light shielding of the TFTs.
Example:

![Diagram of an AMOLED display with organic thin film transistors (OTFT)](image)

153: shield layer

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| TFT with light shield | H01L 29/78633 |

**H01L 27/3274**

{including organic thin film transistors [OTFT]}

**Definition statement**

This place covers:

AMOLED display having a TFT wherein the active region of the TFT comprises organic material

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| ICs having OTFTs | H01L 27/283 |
| Organic TFT | H01L 51/0508 |
| Organic light emitting TFT | H01L 51/5296 |


H01L 27/3276

{Wiring lines}

Definition statement

This place covers:

Special disposition, geometry or construction of wiring lines in AMOLEDs.
source signal line (101a, 101b) and current supply line (104a, 104b) are formed on different layers with insulating layers interposed between the lines to overlap with each other.

External connection of cathode:

Cathode 437 is electrically connected to flexible printed circuit 411 via connecting wirings 410a-410c.

References

Limiting references

This place does not cover:

| External connection of electrodes for non-matrix type displays | H01L 51/5203 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Wiring lines in PMOLEDs | H01L 27/3288 |

Special rules of classification

If the display can be either an active or passive matrix display, both the groups H01L 27/3276 and H01L 27/3288 are given rather than H01L 27/3297.

H01L 27/3279

{comprising structures specially adapted for lowering the resistance}

Definition statement

This place covers:

Materials, additional layers, geometry, and disposition of layers that reduce resistance in the AMOLED display device.
Examples

In the present example the structure minimizes electrical resistance between upper electrode 17 and upper electrode power source line 16

**H01L 27/3281**

**{Passive matrix displays}**

**Definition statement**

*This place covers:*

OLED display wherein the pixels are driven by circuitry out of the display region, e.g. peripheral circuitry. The pixels are basically formed by the crossing of the column and row wiring lines.

Example:

**H01L 27/3283**

**{Including banks or shadow masks}**

**Definition statement**

*This place covers:*

Particular details of the insulating layer or insulating structures formed between the emissive portions of the PMOLED e.g. to pattern the cathode
Examples

20: anode stripes, 60: pixel defining layer, 50: ramparts

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Banks in AMOLED displays                        | H01L 27/3246 |
| Deposition of organic semiconductor materials using liquid deposition (often using spacers for the deposition of the liquid) | H01L 51/0003 |

Special rules of classification

If the display device can be either an active or passive matrix display, both the groups H01L 27/3246 AND H01L 27/3283 are given. H01L 27/3295 is no longer used for classification.

H01L 27/3286

{Dual display, i.e. having two independent displays}

Definition statement

This place covers:

Display emitting different information in its two major surfaces. Generally it comprises two displays stacked on top of another, at least one of the displays is a passive matrix OLED display.

Example:
The passive matrix displays are each emitting through their supporting substrate. In this example, the additional class H01L 25/048 is given for the assembly.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

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<thead>
<tr>
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<tr>
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</tr>
<tr>
<td>AMOLED dual display</td>
<td>H01L 27/3267</td>
</tr>
<tr>
<td>Telephones having more than one display unit</td>
<td>H04M 2250/16</td>
</tr>
</tbody>
</table>

Special rules of classification

Transparent OLED displays having a single light emitting cell emitting in the two main directions of the display are classified elsewhere depending on characterizing feature e.g. H01L 51/5234 (transparent cathode) and H01L 2251/5323 (Indexing Code-code for transparent OLED).

H01L 27/3288

{Wiring lines}

Definition statement

This place covers:

Special disposition, geometry or construction (e.g. layout) of wiring lines in PMOLEDs.
Examples:

External connection of electrodes:
anode 502 electrically connected to flexible printed circuit 512 via printed wiring board side wiring 511 and anisotropic conductive films 508

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Wiring lines in AMOLEDs</th>
<th>H01L 27/3276</th>
</tr>
</thead>
<tbody>
<tr>
<td>External connection of electrodes in non-matrix type displays</td>
<td>H01L 51/5203</td>
</tr>
</tbody>
</table>

Special rules of classification

If the display can be either an active or passive matrix display, both the groups H01L 27/3276 AND H01L 27/3288 are given. H01L 27/3297 is no longer used for classification.
H01L 27/329
{comprising structures specially adapted for lowering the resistance}

Definition statement
This place covers:
Materials, additional layers, geometry and disposition of layers that reduce electrical resistance of the wiring lines in the PMOLED display device

References
Limiting references
This place does not cover:
ITO stripes with auxiliary metal lines to lower the resistance

H01L 27/3293
{Tiled displays}

Definition statement
This place covers:
Displays comprising a superposition of smaller interconnected OLED panels in order to achieve large area displays

Examples

![Diagram of tiled displays]

US2006/044215

![Diagram of tiled displays]

EP1903378
**H01L 27/3295**

{including banks or shadow masks}

**Special rules of classification**

This group is no longer used for classification of new documents. Its subject matter is covered by groups H01L 27/3244 - H01L 27/3293.

**H01L 27/3297**

{Wiring lines, e.g. power supply lines}

**Special rules of classification**

This group is no longer used for classification of new documents. Its subject matter is covered by groups H01L 27/3244 - H01L 27/3293.

**H01L 28/00**

{Passive two-terminal components without a potential-jump or surface barrier for integrated circuits; Details thereof; Multistep manufacturing processes therefor (testing or measuring during manufacture H01L 22/00; integration methods H01L 21/70; integrated circuits H01L 27/00; two-terminal components with a potential-jump or surface barrier H01L 29/00; resistors in general H01C; inductors in general H01F; capacitors in general H01G)}

**Definition statement**

This place covers:

- Passive two-terminal devices, i.e. resistors, capacitors and inductors, specially adapted for being integrated with other semiconductor devices
- Multistep processes for the fabrication of these two terminal devices

**References**

**Limiting references**

This place does not cover:

| Integration methods                              | H01L 21/70                          |
| Testing or measuring during manufacture          | H01L 22/00                          |
| Integrated circuits                              | H01L 27/00                          |
| Two-terminal components with a potential-jump or surface barrier | H01L 29/00                          |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Resistors in general                              | H01C                                |
| Inductors in general                              | H01F                                |
| Capacitors in general                             | H01G                                |
Special rules of classification

In case a single step of the multistep sequence would appear peculiar, it should also be classified in the corresponding single step, for example:

- **H01L 21/02107** for the formation of insulating layers,
- **H01L 21/283 - H01L 21/288** for the formation of conductive layers,
- **H01L 21/027 - H01L 21/033** for lithographic aspects
- **H01L 21/311** for etching insulating layers
- **H01L 21/3213** for etching conductive layers

**H01L 29/00**

Semiconductor devices adapted for rectifying, amplifying, oscillating or switching, or capacitors or resistors with at least one potential-jump barrier or surface barrier, e.g. PN junction depletion layer or carrier concentration layer; Details of semiconductor bodies or of electrodes thereof; {Multistep manufacturing processes therefor} (**H01L 31/00 - H01L 47/00, H01L 51/05** take precedence; processes or apparatus adapted for the manufacture or treatment thereof or of parts thereof **H01L 21/00**; details other than of semiconductor bodies or of electrodes thereof **H01L 23/00**; devices consisting of a plurality of solid state components formed in or on a common substrate **H01L 27/00**; {passive two-terminal components without a potential-jump or surface barrier for integrated circuits, details thereof and multistep manufacturing processes therefor **H01L 28/00**; } resistors in general **H01C**; capacitors in general **H01G**, {e.g. ceramic barrier-layer capacitors **H01G 4/1272**})

**Definition statement**

*This place covers:*

- Types of inorganic semiconductor components with at least one potential-jump barrier or surface barrier, adapted for rectifying, amplifying, oscillating or switching; Multistep manufacturing processes therefor.
- Types of components for integrated circuits being capacitors or resistors with at least one potential-jump barrier or surface barrier; Multistep manufacturing processes therefor.
- Details of semiconductor bodies of said components; Details of semiconductor bodies not otherwise provided for; Multistep manufacturing processes therefor.
- Details of electrodes of said components; Details of electrodes of semiconductor components not otherwise provided for; Multistep manufacturing processes therefor.

Further information:

In this main group:

Said potential-jump or surface barrier may be of the PN junction type, the metal-semiconductor junction type, the metal-insulator-semiconductor type, the high-low junction type, the heterojunction type.

Said details of semiconductor bodies and said multistep manufacturing processes therefor are covered by groups **H01L 29/02 - H01L 29/365**.

Said details of electrodes are covered by groups **H01L 29/40 - H01L 29/518** except group **H01L 29/401**, and said multistep manufacturing processes therefor are covered by group **H01L 29/401** (pending reorganisation see group **H01L 21/28** and subgroups).
Said types of inorganic semiconductor components are covered by groups H01L 29/66 - H01L 29/945 except groups H01L 29/66007 and subgroups, H01L 29/8605, H01L 29/92 - H01L 29/945, and said multistep manufacturing processes therefor are covered by group H01L 29/66007 and subgroups except H01L 29/66022 and H01L 29/66166 - H01L 29/66189.

Said resistors are covered by group H01L 29/8605, and said multistep manufacturing processes therefor are covered by groups H01L 29/66022, H01L 29/6606 and H01L 29/66166.

Said capacitors are covered by groups H01L 29/92 - H01L 29/945, and said multistep manufacturing processes therefor are covered by groups H01L 29/66022, H01L 29/6606 and H01L 29/66174 - H01L 29/66189.

**References**

**Limiting references**

This place does not cover:

| Processes or apparatuses adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof | H01L 21/00 |
| Details of semiconductor or other solid state devices other than details of semiconductor bodies or of electrodes thereof | H01L 23/00, H01L 24/00 |
| Assemblies consisting of a plurality of individual semiconductor or other solid state devices | H01L 25/00 |
| Devices consisting of a plurality of solid state components formed in or on a common substrate | H01L 27/00 |
| Passive two-terminal components without a potential-jump or surface barrier for integrated circuits; Details thereof; Multistep manufacturing processes therefor | H01L 28/00 |
| Semiconductor devices sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof; Details thereof | H01L 31/00 |
| Semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission; Processes or apparatus specially adapted for the manufacture or treatment thereof or of parts thereof; Details thereof | H01L 33/00 |
| Thermo-electric devices comprising a junction of dissimilar materials, i.e. exhibiting Seebeck or Peltier effect with or without other thermo-electric effects or thermomagnetic effects; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof; Details thereof | H01L 35/00 |
| Thermoelectric devices without a junction of dissimilar materials; Thermomagnetic devices, e.g. using Nernst-Ettinghausen effect; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof | H01L 37/00 |
| Devices using superconductivity; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof | H01L 39/00 |
| Piezo-electric devices; Electrostrictive devices; Magnetostrictive devices; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof; Details thereof | H01L 41/00 |
### Devices using galvano-magnetic or similar magnetic effects; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof

H01L 43/00

### Solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof

H01L 45/00

### Bulk negative resistance effect devices, e.g. Gunn-effect devices; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof

H01L 47/00

### Solid state devices not provided for in groups H01L 27/00 - H01L 47/00 and H01L 51/00 and not provided for in any other subclass; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof

H01L 49/00

### Solid state devices using organic materials as the active part, or using a combination of organic materials with other materials as the active part; Processes or apparatus specially adapted for the manufacture or treatment of such devices, or of parts thereof

H01L 51/00

### Semiconductor lasers

H01S 5/00

### Printed circuits

H05K 1/00, H05K 3/00

### References out of a residual place

Examples of places in relation to which this place is residual:

| Details of semiconductor bodies or of electrodes of semiconductor components | H01L 31/00 - H01L 47/00, H01S 5/00, G01 |

### Informative references

Attention is drawn to the following places, which may be of interest for search:

| Encapsulations, e.g. encapsulating layers, coatings, e.g. for protection | H01L 23/28 |
| Single-crystal-growth, e.g. of semiconductor material, in general | C30B |
| Ion-sensitive or chemical field-effect transistors | G01N 27/414 |
| Digital stores characterised by the use of particular electric elements; Storage elements therefore | G11C 11/00 |
| Conversion of electric power | H02M |
| Generation of oscillations | H03B |
| Amplifiers with semiconductor devices as amplifying elements | H03F 3/00, H03F 5/00 |
| Electronic switching or gating | H03K 17/00 |
| Logic circuits; Inverting circuits | H03K 19/00 |

### Special rules of classification

Classification of invention information is made in any one of the following 3 sets of groups if these sets of groups are relevant:

- **H01L 29/02 - H01L 29/36** for details of semiconductor bodies and multistep manufacturing processes therefor;
• **H01L 29/40** - **H01L 29/51** for details of electrodes and multistep manufacturing processes therefor; and

• **H01L 29/66** - **H01L 29/94** for types of components and multistep manufacturing processes therefor.

In any one of the a.m. sets of groups classification is made in any appropriate place, i.e. multi-aspect classification is used.

Classification of additional information through allocation of the Indexing Codes **H01L 29/00** - **H01L 29/94** is mandatory.

### Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Alloy</strong></td>
<td>homogeneous material having chemically combined atoms or ions in variable proportions, e.g. AlxGa(1-x)As</td>
</tr>
<tr>
<td><strong>Bidirectional</strong></td>
<td>conducting main current in opposite directions</td>
</tr>
<tr>
<td><strong>Bandgap, band gap</strong></td>
<td>difference between energy levels of electrons bound to their nuclei (valence electrons) and energy levels allowing electrons to migrate freely (conduction electrons)</td>
</tr>
<tr>
<td><strong>Bipolar device</strong></td>
<td>device using both charge carrier types in operation, i.e. both electrons and holes</td>
</tr>
<tr>
<td><strong>Breakdown</strong></td>
<td>sudden change to a very low dynamic electrical resistance, e.g. in a reverse biased pn-junction</td>
</tr>
<tr>
<td><strong>Channel stopper</strong></td>
<td>means for limiting parasitic surface channel formation, usually a highly doped surface region in a lightly doped substrate of same conductivity type</td>
</tr>
<tr>
<td><strong>Charge carrier</strong></td>
<td>electron (having a negative charge) or hole (having a positive charge)</td>
</tr>
<tr>
<td><strong>Circuit</strong></td>
<td>plurality of electric elements interconnected to perform an electrical or electronic function</td>
</tr>
<tr>
<td><strong>Conductivity</strong></td>
<td>ability of a material to conduct electric current</td>
</tr>
<tr>
<td><strong>Component</strong></td>
<td>a single active or passive electric circuit element that may be formed in or on a common substrate</td>
</tr>
<tr>
<td><strong>Compound</strong></td>
<td>homogeneous material having chemically combined atoms or ions in definite proportions, e.g. gallium arsenide (GaAs), silicon carbide (SiC)</td>
</tr>
<tr>
<td><strong>Device</strong></td>
<td>electric circuit element</td>
</tr>
<tr>
<td><strong>Diode</strong></td>
<td>two-terminal semiconductor component with non linear current-voltage characteristic</td>
</tr>
<tr>
<td><strong>Electrode</strong></td>
<td>region other than the semiconductor body itself, which exerts an influence on the solid state body electrically, whether or not an external electrical connection is made thereto. The term covers capacitive or inductive coupling arrangements and an electrode may include several portions, e.g. metallic and dielectric regions of a capacitive coupling arrangement. Only those portions which exert an influence on the solid state body by virtue of their shape, size or disposition or the material of which they are formed are considered to be part of the electrode.</td>
</tr>
<tr>
<td><strong>Electron</strong></td>
<td>negative charge carrier</td>
</tr>
<tr>
<td><strong>Field plate</strong></td>
<td>electric field shaping field-effect electrode</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Guard region</td>
<td>electric field shaping semiconductor region, e.g. to increase the breakdown voltage of an adjacent pn-junction</td>
</tr>
<tr>
<td>Guard ring</td>
<td>electric field shaping ring-shaped semiconductor region</td>
</tr>
<tr>
<td>High-low junction</td>
<td>junction of materials with relatively high and low doping concentration</td>
</tr>
<tr>
<td>Heterojunction</td>
<td>junction of different materials</td>
</tr>
<tr>
<td>Hole</td>
<td>positive charge carrier, i.e. missing valence electron, valence band vacancy</td>
</tr>
<tr>
<td>Homo junction</td>
<td>junction of same material</td>
</tr>
<tr>
<td>Multiple quantum well</td>
<td>quantum structure composed of a plurality of uncorrelated quantum wells</td>
</tr>
<tr>
<td>N-type</td>
<td>negative conductivity type, i.e. with electrons as majority charge carriers</td>
</tr>
<tr>
<td>Ohmic contact</td>
<td>non-rectifying contact</td>
</tr>
<tr>
<td>Part</td>
<td>any structural unit included in a complete device</td>
</tr>
<tr>
<td>Pn-junction</td>
<td>junction of materials of opposite conductivity types, i.e. n-type and p-type materials</td>
</tr>
<tr>
<td>P-type</td>
<td>positive conductivity type, i.e. with holes as majority charge carriers</td>
</tr>
<tr>
<td>Quantum well</td>
<td>potential well with one-dimensional confinement whereby quantum effects are achieved</td>
</tr>
<tr>
<td>Quantum wire</td>
<td>potential well with two-dimensional confinement whereby quantum effects are achieved</td>
</tr>
<tr>
<td>Quantum box</td>
<td>potential well with three-dimensional confinement whereby quantum effects are achieved</td>
</tr>
<tr>
<td>Schottky contact</td>
<td>rectifying metal-semiconductor contact</td>
</tr>
<tr>
<td>Semiconductor body</td>
<td>body of semiconductor material within which, or at the surface of which, the physical effects characteristic of the component occur</td>
</tr>
<tr>
<td>Silicide</td>
<td>silicon-metal compound</td>
</tr>
<tr>
<td>Structurally associated with</td>
<td>with a built-in</td>
</tr>
<tr>
<td>Superlattice</td>
<td>quantum structure with a plurality of correlated quantum wells leading to the formation of mini-bands and mini-bandgaps across the whole structure</td>
</tr>
<tr>
<td>Unipolar device</td>
<td>device using only one of both charge carrier types, i.e. either electrons or holes</td>
</tr>
</tbody>
</table>

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1DEG</td>
<td>one-dimensional electron gas</td>
</tr>
<tr>
<td>1DHG</td>
<td>one-dimensional hole gas</td>
</tr>
<tr>
<td>2DEG</td>
<td>two-dimensional electron gas</td>
</tr>
<tr>
<td>2DHG</td>
<td>two-dimensional hole gas</td>
</tr>
<tr>
<td>ACCUFET</td>
<td>accumulation layer field-effect transistor</td>
</tr>
<tr>
<td>ALD</td>
<td>atomic layer doping</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>BARRITT</td>
<td>barrier injection transit time diode</td>
</tr>
<tr>
<td>BBD</td>
<td>bucket brigade device</td>
</tr>
<tr>
<td>BJT</td>
<td>bipolar junction transistor</td>
</tr>
<tr>
<td>BK</td>
<td>breakdown</td>
</tr>
<tr>
<td>BSIT</td>
<td>bipolar static induction transistor</td>
</tr>
<tr>
<td>CCD</td>
<td>charge coupled device</td>
</tr>
<tr>
<td>COMFET</td>
<td>conductivity modulation field-effect transistor</td>
</tr>
<tr>
<td>DDD</td>
<td>double diffused drain</td>
</tr>
<tr>
<td>DH</td>
<td>double heterojunction</td>
</tr>
<tr>
<td>DEMOS</td>
<td>drain extended metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>DIAC</td>
<td>diode for alternating current</td>
</tr>
<tr>
<td>DMOS</td>
<td>double diffused metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>FAMOS</td>
<td>floating gate avalanche injection metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>FCD</td>
<td>field-controlled diode</td>
</tr>
<tr>
<td>FET</td>
<td>field-effect transistor</td>
</tr>
<tr>
<td>FG</td>
<td>floating gate</td>
</tr>
<tr>
<td>FinFET</td>
<td>field-effect transistor with fin-shaped active layer</td>
</tr>
<tr>
<td>FLR</td>
<td>field limiting ring</td>
</tr>
<tr>
<td>FN tunnelling</td>
<td>Fowler-Nordheim tunnelling</td>
</tr>
<tr>
<td>FW diode</td>
<td>freewheel diode</td>
</tr>
<tr>
<td>FW voltage</td>
<td>forward voltage</td>
</tr>
<tr>
<td>GTO</td>
<td>gate turn-off thyristor</td>
</tr>
<tr>
<td>HBT</td>
<td>heterojunction bipolar transistor</td>
</tr>
<tr>
<td>HEMT</td>
<td>high electron mobility transistor</td>
</tr>
<tr>
<td>HET</td>
<td>hot electron transistor</td>
</tr>
<tr>
<td>HV</td>
<td>high voltage</td>
</tr>
<tr>
<td>HVMOS</td>
<td>high voltage metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>IGBT</td>
<td>insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IGFET</td>
<td>insulated gate field-effect transistor</td>
</tr>
<tr>
<td>IMPATT</td>
<td>impact avalanche transit time diode</td>
</tr>
<tr>
<td>JFET</td>
<td>junction-gate field-effect transistor</td>
</tr>
<tr>
<td>JTE</td>
<td>junction termination extension</td>
</tr>
<tr>
<td>LDD</td>
<td>lightly doped drain</td>
</tr>
<tr>
<td>LDMOS</td>
<td>lateral double-diffused metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>LOCOS</td>
<td>local oxidation of silicon</td>
</tr>
<tr>
<td>MBT</td>
<td>metal base transistor</td>
</tr>
<tr>
<td>MCT</td>
<td>MOS-controlled thyristor</td>
</tr>
<tr>
<td>MESFET</td>
<td>metal-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>MGT</td>
<td>metal-oxide-semiconductor-gated thyristor</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>MIS</td>
<td>metal-insulator-semiconductor</td>
</tr>
<tr>
<td>MISFET</td>
<td>metal-insulator-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>MNOS</td>
<td>metal nitride oxide semiconductor</td>
</tr>
<tr>
<td>MODFET</td>
<td>modulation doped field-effect transistor</td>
</tr>
<tr>
<td>MOSTOT</td>
<td>metal-oxide-semiconductor turn-off thyristor</td>
</tr>
<tr>
<td>MQW</td>
<td>multiple quantum well</td>
</tr>
<tr>
<td>NDR</td>
<td>negative differential resistance</td>
</tr>
<tr>
<td>NERFET</td>
<td>negative resistance field-effect transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-type channel metal-oxide-semiconductor (transistor)</td>
</tr>
<tr>
<td>PBT</td>
<td>permeable base transistor</td>
</tr>
<tr>
<td>PDB</td>
<td>planar doped barrier</td>
</tr>
<tr>
<td>PIN</td>
<td>P intrinsic N</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-type channel metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>RCT</td>
<td>reverse conducting thyristor</td>
</tr>
<tr>
<td>RESURF</td>
<td>reduced surface field</td>
</tr>
<tr>
<td>ROX</td>
<td>recessed oxide isolation</td>
</tr>
<tr>
<td>RT</td>
<td>resonant tunnelling</td>
</tr>
<tr>
<td>RTD</td>
<td>resonant tunnelling diode</td>
</tr>
<tr>
<td>SBD</td>
<td>Schottky barrier diode</td>
</tr>
<tr>
<td>SCR</td>
<td>silicon controlled rectifier</td>
</tr>
<tr>
<td>SET</td>
<td>single electron transistor</td>
</tr>
<tr>
<td>SIT</td>
<td>static induction transistor</td>
</tr>
<tr>
<td>SITH</td>
<td>static induction thyristor</td>
</tr>
<tr>
<td>SJ</td>
<td>superjunction</td>
</tr>
<tr>
<td>SL</td>
<td>superlattice</td>
</tr>
<tr>
<td>SOI</td>
<td>silicon-on-insulator</td>
</tr>
<tr>
<td>SQW</td>
<td>single quantum well</td>
</tr>
<tr>
<td>STI</td>
<td>shallow trench isolation</td>
</tr>
<tr>
<td>TFET</td>
<td>tunnel field-effect transistor</td>
</tr>
<tr>
<td>TFT</td>
<td>thin film transistor</td>
</tr>
<tr>
<td>TRAPATT</td>
<td>trapped plasma avalanche transit time diode</td>
</tr>
<tr>
<td>TRIAC</td>
<td>triode for alternating current</td>
</tr>
<tr>
<td>UMOS</td>
<td>U-shaped trench gate metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>VMOS</td>
<td>V-shaped trench gate metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>VDMOS</td>
<td>vertical double-diffused metal-oxide-semiconductor transistor</td>
</tr>
<tr>
<td>VTh</td>
<td>threshold voltage</td>
</tr>
<tr>
<td>QID</td>
<td>quantum interference device</td>
</tr>
<tr>
<td>QW</td>
<td>quantum well</td>
</tr>
<tr>
<td>ZD</td>
<td>Zener diode</td>
</tr>
</tbody>
</table>
In patent documents the following expressions/words are often used as synonyms:

<table>
<thead>
<tr>
<th>Expression/Word</th>
<th>Synonym</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic layer doping, atomic plane doping, delta doping</td>
<td>planar doping</td>
</tr>
<tr>
<td>Chip</td>
<td>die</td>
</tr>
<tr>
<td>Depletion region</td>
<td>space charge region</td>
</tr>
<tr>
<td>Electrode</td>
<td>contact</td>
</tr>
<tr>
<td>Group IV</td>
<td>group 14: C, Si, Ge, Sn, Pb</td>
</tr>
<tr>
<td>II-VI</td>
<td>group 12/16, e.g. CdTe</td>
</tr>
<tr>
<td>III-V, AlIIIBV, AlIII-BV</td>
<td>group 13/15, e.g. GaAs</td>
</tr>
<tr>
<td>Intrinsic</td>
<td>undoped, not intentionally doped</td>
</tr>
<tr>
<td>Impurity</td>
<td>dopant, doping material</td>
</tr>
<tr>
<td>Polysilicon, poly-Si</td>
<td>polycrystalline silicon</td>
</tr>
<tr>
<td>Charge compensation, coolMOS, multi-RESURF</td>
<td>superjunction</td>
</tr>
<tr>
<td>Channel stopper</td>
<td>channel stop, chanstop</td>
</tr>
</tbody>
</table>

In patent documents the expression/word is often used with the meaning:

<table>
<thead>
<tr>
<th>Expression/Word</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakover</td>
<td>start of regenerative current flow in a thyristor</td>
</tr>
<tr>
<td>Chip</td>
<td>piece of semiconductor material, e.g. single crystal semiconductor substrate, having one or more active or passive electric circuit elements</td>
</tr>
<tr>
<td>(charge or carrier) confinement</td>
<td>restriction of charge carriers to locations of reduced dimensions, e.g. quantum wells, field-effect induced potential wells</td>
</tr>
<tr>
<td>Crystal defect</td>
<td>non-uniformity in crystal lattice</td>
</tr>
<tr>
<td>De Broglie wavelength</td>
<td>wavelength of a particle</td>
</tr>
<tr>
<td>Depletion region</td>
<td>region from which free charge carriers are expelled</td>
</tr>
<tr>
<td>Direct bandgap material</td>
<td>semiconductor material wherein transition from the conduction to the valence band does not require a change in crystal momentum for an electron, e.g. gallium arsenide (GaAs)</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>number of dopant atoms per a given volume of semiconductor material, e.g. per cubic centimetre</td>
</tr>
<tr>
<td>Doping density</td>
<td>number of dopant atoms per a given surface of semiconductor material, e.g. per square centimetre</td>
</tr>
<tr>
<td>Doping profile</td>
<td>point-to-point doping concentration throughout a semiconductor body or region thereof</td>
</tr>
<tr>
<td>Epitaxial layer</td>
<td>added layer of semiconductor crystal taking on the same crystalline orientation as a semiconductor crystal substrate</td>
</tr>
<tr>
<td>Field oxide</td>
<td>oxide layer overlying a major surface of a device semiconductor body</td>
</tr>
<tr>
<td>Floating gate</td>
<td>electrically floating gate electrode, e.g. having no direct electrical connection, usually used for charge storage</td>
</tr>
<tr>
<td>Forward bias</td>
<td>voltage applied in a current conducting direction</td>
</tr>
</tbody>
</table>
Indirect bandgap material: semiconductor material wherein transition from the conduction to the valence band requires a change in crystal momentum for an electron, e.g., silicon (Si).

Inversion layer: surface region in a semiconductor material wherein the minority carrier concentration is larger than the majority carrier concentration, e.g., induced by field-effect.

Latch-up: regenerative feedback loop thyristor-type conducting state, being parasitic in e.g., non-thyristor-type components due to loss of gating capability.

Lifetime killer: deep level impurity creating a potential trap for charge carriers in the forbidden band remote from the conduction and valence bands thereby reducing charge carrier lifetime.

Majority carrier: more abundant charge carrier.

Minority carrier: less abundant charge carrier.

Polycide: polysilicon-silicide stack.

Recombination center, deep level center: potential trap for charge carriers in the forbidden band remote from the conduction and valence bands.

Reverse bias: voltage applied in a current blocking direction.

Shockley diode: two-terminal thyristor.

Silicon controlled rectifier (SCR): three-terminal thyristor.

Salicide process: self-aligned silicide process.

Wide band gap semiconductor material: semiconductor material with a band gap larger than 1.7 eV, e.g., SiC, GaN, diamond.

**H01L 29/00 (continued)**

**H01L 29/66227**

{the devices being controllable only by the electric current supplied or the electric potential applied, to an electrode which does not carry the current to be rectified, amplified or switched, e.g., three-terminal devices}

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BBT</td>
<td>Bulk Barrier Transistor</td>
</tr>
<tr>
<td>CHINT</td>
<td>CHarge INjection Transistor</td>
</tr>
<tr>
<td>FCTh</td>
<td>Field Controlled Thyristor</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>IPG</td>
<td>In-plane Gate Transistor</td>
</tr>
<tr>
<td>HET</td>
<td>Hot Electron Transistor</td>
</tr>
<tr>
<td>HFET</td>
<td>Heterojunction Field Effect Transistor</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction Field Effect Transistor</td>
</tr>
<tr>
<td>MBT</td>
<td>Metal Base Transistor</td>
</tr>
<tr>
<td>MISFET</td>
<td>Metal-Insulator-Field Effect Transistor</td>
</tr>
<tr>
<td>PBT</td>
<td>Permeable Base Transistor</td>
</tr>
<tr>
<td>PDBT</td>
<td>Planar Doped Barrier Transistor</td>
</tr>
</tbody>
</table>
H01L 29/66227 (continued)

<table>
<thead>
<tr>
<th>RHET</th>
<th>Resonant Tunnelling Hot Electron Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTT</td>
<td>Resonant Tunnelling Transistor</td>
</tr>
<tr>
<td>SET</td>
<td>Single Electron Transistor</td>
</tr>
<tr>
<td>SIT</td>
<td>Static field Induction Transistor</td>
</tr>
<tr>
<td>SiTh</td>
<td>Thyristor</td>
</tr>
<tr>
<td>VMT</td>
<td>Velocity Modulation Transistor</td>
</tr>
</tbody>
</table>

H01L 29/66242

{Heterojunction transistors [HBT] (with an active layer made of a group 13/15 material H01L 29/66318)}

Definition statement

This place covers:

For multistep processes, a junction between two regions of the same material but in a different crystalline state, e.g. amorphous silicon or polysilicon emitters on single crystalline silicon, is not considered as an heterojunction.

H01L 29/66363

{Thyristors}

Definition statement

This place covers:

So-called FCTh, SITh and FCD are classified in H01L 29/6609.

H01L 29/665

{using self aligned silicidation, i.e. salicide (formation of conductive layers comprising silicides H01L 21/28518)}

Special rules of classification

Documents are classified in this group when they are concerned with avoiding a short circuit between source or drain and gate.

Improving the source or drain contact is classified elsewhere, e.g. H01L 21/28518.

Improving the gate is also classified elsewhere, e.g. H01L 21/28052.

To note the mere presence of salicide, the corresponding Indexing Code is systematically allocated.

H01L 29/66507

{providing different silicide thicknesses on the gate and on source or drain}

Definition statement

This place covers:

It follows from the definition that source / drain with different silicide thicknesses are also classified here, as at least one of the thickness of the source / drain silicide is different from the thickness of the gate silicide.
H01L 29/66545

{using a dummy, i.e. replacement gate in a process wherein at least a part of the final gate is self aligned to the dummy gate}

Special rules of classification

Processes where only a part of the gate is a dummy layer, e.g. part of a silicide stemming from the silicidation of polysilicon, are also classified in this group.

H01L 29/66863

{Lateral single gate transistors}

References

Limiting references

This place does not cover:

Manufacturing of the gate itself H01L 21/28

Special rules of classification

Processes wherein there are no source and drain semiconductor regions formed in the active layer, i.e. no high-temperature, e.g. a 800°C, step is required for these regions, are classified in this group.

Examples: S&D deposited on the active layer;
No S&D regions at all, e.g. alloyed contacts;
Gate recess etched through S&D layer(s).

H01L 29/66871

{Processes wherein the final gate is made after the formation of the source and drain regions in the active layer, e.g. dummy-gate processes}

Definition statement

This place covers:
Processes wherein the drain is formed before the final gate but wherein a LDD or the like is formed after

H01L 29/66969

{of devices having semiconductor bodies not comprising group 14 or group 13/15 materials (comprising selenium or tellurium in uncombined form other than as impurities in semiconductor bodies of other materials, comprising cuprous oxide or cuprous iodide H01L 21/02365)}

Special rules of classification

The single step processes forming the multistep should also be classified independently of the multistep, provided the single step gives significant information.
H01L 31/00

Semiconductor devices sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof; Details thereof (H01L 51/42 takes precedence; devices consisting of a plurality of solid state components formed in, or on, a common substrate, other than combinations of radiation-sensitive components with one or more electric light sources, H01L 27/00; measurement of X-radiation, gamma radiation, corpuscular radiation or cosmic radiation with semiconductor detectors G01T 1/24, with resistance detectors G01T 1/26; measurement of neutron radiation with semiconductor detectors G01T 3/08; couplings of light guides with optoelectronic elements G02B 6/42; obtaining energy from radioactive sources G21H)

References

Limiting references

This place does not cover:

| Devices consisting of a plurality of solid state components formed in, or on, a common substrate, other than combinations of radiation-sensitive components with one or more electric light sources | H01L 27/00 |
| Organic photosensitive devices | H01L 51/42 |
| Electrolytic light sensitive devices, e.g. dye sensitized solar cells | H01G 9/20 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Imager structures consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate | H01L 27/146 |
| Production of heat using solar heat | F24S |
| Measurement of X-radiation, gamma radiation, corpuscular radiation or cosmic radiation with semiconductor detectors | G01T 1/24 |
| Measurement of X-radiation, gamma radiation, corpuscular radiation or cosmic radiation with resistance detectors | G01T 1/26 |
| Measurement of neutron radiation with semiconductor detectors | G01T 3/08 |
| Couplings of light guides with optoelectronic elements | G02B 6/42 |
| Arrangement for obtaining electrical energy from radioactive sources | G21H 1/00 |

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

<p>| Homojunction | p-n junction involving both p and n regions made out of the same material, with the same composition and the same structure (only the doping species change). |</p>
<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heterojunction</td>
<td>p-n junction involving two different materials, the difference being in the structure and/or the composition (examples: p-type amorphous silicon / n-type crystalline silicon; GaAs/GaAlAs)</td>
</tr>
<tr>
<td>Tandem solar cell</td>
<td>A plurality of junctions are monolithically stacked on one another, forming a multiple junction solar cell</td>
</tr>
<tr>
<td>Schottky contact</td>
<td>Rectifying (non-ohmic) metal/semiconductor contact</td>
</tr>
<tr>
<td>Group 14 elements</td>
<td>Formerly known as group IVa elements (C, Si, Ge, Sn, Pb)</td>
</tr>
<tr>
<td>Coating</td>
<td>A &quot;coating&quot; is a thin layer deposited on the surface of the semiconductor device and only on its surface, having passivating or optical (ex: AR) effects.</td>
</tr>
<tr>
<td>Encapsulation</td>
<td>An &quot;encapsulation&quot; is an enclosure which consists of one or more layers formed on the body and in intimate contact therewith. Compared to a &quot;coating&quot;, an &quot;encapsulation&quot; is usually a much thicker film (used for protecting the device from the outside) which also usually wraps the edges of the device.</td>
</tr>
<tr>
<td>Container</td>
<td>Enclosure forming part of the complete device and is essentially a solid construction in which the body of the device is placed, or which is formed around the body without forming an intimate layer thereon.</td>
</tr>
<tr>
<td>Apparatus</td>
<td>A category of subject matter which is a machine or device, described in terms of its functional capabilities or structural features, that is used to make a product, or to carry out a non-manufacturing process or activity.</td>
</tr>
<tr>
<td>Electrodes</td>
<td>Regions in or on the body of the device (other than the solid state body itself), which exert an influence on the solid state body electrically, whether or not an external electrical connection is made thereto. In electrode arrangements including several portions only those portions which exert an influence on the solid state body by virtue of their shape, size or disposition or the material of which they are formed are considered to be part of the electrode. The other portions are considered to be &quot;arrangements for conducting electric current to or from the solid state body&quot; or &quot;interconnections between solid state components formed in or on a common substrate&quot;, i.e. leads.</td>
</tr>
<tr>
<td>Up- or down conversion</td>
<td>Transformation of incident photons having wavelengths into different wavelengths (longer or shorter) in order to increase absorption of the photoactive part of the device (usually using luminescent materials)</td>
</tr>
<tr>
<td>Photoelectric devices</td>
<td>Light sensitive devices based on the photoelectric effect, including both photovoltaic devices (solar cells) and photodetecting devices (photosensors)</td>
</tr>
<tr>
<td>Photoconductive material</td>
<td>Material in which the electrical conductivity changes when light is absorbed by said material</td>
</tr>
<tr>
<td>Superlattice</td>
<td>Periodic structure involving alternating semiconductor layers, the thickness of each layer being typically of a few nanometres and in which quantum effects take place. The difference between adjacent layers lies in the composition and/or the doping.</td>
</tr>
<tr>
<td>Intrinsic layer</td>
<td>Semiconductor layer which is not intentionally doped</td>
</tr>
</tbody>
</table>
### Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-Si, α-Si</td>
<td>amorphous silicon</td>
</tr>
<tr>
<td>C-Si</td>
<td>crystalline silicon</td>
</tr>
<tr>
<td>Mc-Si, muc-Si, μc-Si, μ-Si</td>
<td>microcrystalline silicon</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>polycrystalline silicon</td>
</tr>
<tr>
<td>PIN</td>
<td>P-N junction with thick intrinsic layer in between</td>
</tr>
<tr>
<td>AlIBIIICVI compound</td>
<td>I-III-VI compound, chalcogenides, chalcopyrites</td>
</tr>
<tr>
<td>CIS</td>
<td>CuInSe₂</td>
</tr>
<tr>
<td>CIGS</td>
<td>CuInGaSe₂</td>
</tr>
<tr>
<td>CIGSS</td>
<td>CuInGaAsSe</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent conducting oxide</td>
</tr>
<tr>
<td>ITO</td>
<td>Indium Tin Oxide</td>
</tr>
<tr>
<td>FTO</td>
<td>Fluorine doped tin oxide</td>
</tr>
<tr>
<td>AZO</td>
<td>Aluminium doped Zinc oxide</td>
</tr>
<tr>
<td>GZO</td>
<td>Gallium doped Zinc oxide</td>
</tr>
<tr>
<td>QW</td>
<td>Quantum well</td>
</tr>
<tr>
<td>MQW</td>
<td>Multiple Quantum Well</td>
</tr>
<tr>
<td>HIT</td>
<td>Heterojunction with Intrinsic Thin-layer</td>
</tr>
<tr>
<td>PERL solar cell</td>
<td>Passivated Emitter Rear Locally Diffused solar cell</td>
</tr>
<tr>
<td>ARC, AR</td>
<td>Anti-reflective coating</td>
</tr>
<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
</tr>
<tr>
<td>MWT</td>
<td>Metal Wrap Through</td>
</tr>
<tr>
<td>FMWT</td>
<td>Front Metal Wrap Through</td>
</tr>
<tr>
<td>EWT</td>
<td>Emitter Wrap Through</td>
</tr>
<tr>
<td>IBC</td>
<td>Interdigitated Back Contact (solar cells)</td>
</tr>
<tr>
<td>BSR</td>
<td>Back Surface Reflector</td>
</tr>
<tr>
<td>BSF</td>
<td>Back Surface Field</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>IR</td>
<td>Infrared</td>
</tr>
<tr>
<td>UV</td>
<td>Ultraviolet</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapour Deposition</td>
</tr>
<tr>
<td>PVD</td>
<td>Physical Vapour Deposition</td>
</tr>
<tr>
<td>LPE</td>
<td>Liquid Phase Epitaxy</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic Layer Deposition</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal Organic Chemical Vapour Deposition</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma Enhanced Chemical Vapour Deposition</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>MIS</td>
<td>Metal Insulator Semiconductor</td>
</tr>
</tbody>
</table>
**H01L 31/02**

**Details**

**Definition statement**

*This place covers:*

- Identification marks
- Nozzles for washing solar modules
- Storage details or shipping means for solar cells
- Design details, camouflage

**References**

*Limiting references*

*This place does not cover:*

<table>
<thead>
<tr>
<th>Particular substrate for thin film solar cells</th>
<th>H01L 31/0392</th>
</tr>
</thead>
<tbody>
<tr>
<td>Particular substrate for bulk photovoltaic cells</td>
<td>H01L 31/06</td>
</tr>
<tr>
<td>Processes or apparatus peculiar to the manufacture or treatment of these devices or of parts thereof, e.g. deposition methods</td>
<td>H01L 31/18</td>
</tr>
</tbody>
</table>

**H01L 31/02002**

*(Arrangements for conducting electric current to or from the device in operations)*

**Definition statement**

*This place covers:*

Details of electrical interconnection of packaging;

Arrangements being portions of the electrical connections to the devices but not being an electrode, i.e. having direct electrical contact with the body of the device.

**References**

*Limiting references*

*This place does not cover:*

<table>
<thead>
<tr>
<th>Electrodes</th>
<th>H01L 31/022425, H01L 31/022466</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical interconnection between solar cells for thin film solar cells</td>
<td>H01L 31/046</td>
</tr>
<tr>
<td>Electrical interconnection between solar cells for bulk solar cells</td>
<td>H01L 31/05</td>
</tr>
</tbody>
</table>

**Special rules of classification**

This specific subgroup *(H01L 31/02002)* is only relevant if the potential barrier of the device is not mentioned, i.e. when it is not clear if the device concerned is a photoconductive or a junction device;

If there is a potential junction, then *H01L 31/02005*, if the device is a solar cell or a solar module, then *H01L 31/02008*. 
H01L 31/02005
{for device characterised by at least one potential jump barrier or surface barrier}

Definition statement
This place covers:
Details of electrical interconnection of packaging for devices involving a potential barrier.

H01L 31/02008
{for solar cells or solar cell modules}

Definition statement
This place covers:
Special electrical connections of a solar cell or a solar module, i.e. to conduct electrical current to an external load.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Connection between cells within a module for thin film solar cells | H01L 31/046 |
| Connection between cells within a module for bulk solar cells     | H01L 31/05  |
| Wiring substrates, e.g. for back contacted solar cells             | H01L 31/0516|
| Electrical connection means, e.g. junction boxes, specially adapted for structural association with photovoltaic modules | H02S 40/34 |
**H01L 31/02016**
{Circuit arrangements of general character for the devices}

**References**

**Informative references**
Attention is drawn to the following places, which may be of interest for search:

| Systems for regulating electric or magnetic variables | G05F |
| Circuits arrangements or systems for supplying or distributing electric power | H02J |

**H01L 31/02021**
{for solar cells (electrical connection means, e.g. junction boxes, specially adapted for structural association with photovoltaic modules H02S 40/34)}

**References**

**Limiting references**
This place does not cover:

| Electrical connection means, e.g. junction boxes, specially adapted for structural association with photovoltaic modules | H02S 40/34 |

**Informative references**
Attention is drawn to the following places, which may be of interest for search:

| Circuitry associated to or formed in the module, e.g. bypass diodes associated with the serial interconnection between cells of the module | H01L 31/044, H01L 31/05 |
| MPPT systems | G05F 1/67 |

**H01L 31/02024**
{Position sensitive and lateral effect photodetectors; Quadrant photodiodes}

**Definition statement**
This place covers:
Photodetectors sensitive to the position of the light beam, for alignment
Quadrant photodiodes, i.e. 4 pixels-photodetectors - and only 4 -, for position adjustment.

**References**

**Limiting references**
This place does not cover:

| Photodetectors having more than 4 pixels | H01L 27/146 |
H01L 31/02027
{for devices working in avalanche mode}

Definition statement
This place covers:
Specific circuitry used with avalanche photodiodes

H01L 31/0203
Containers; Encapsulations {, e.g. encapsulation of photodiodes} (for photovoltaic devices H01L 31/048; for organic photosensitive devices H01L 51/44)

Definition statement
This place covers:
Packaging aspects for single photosensitive components: Housing, transparent windows, resins.

References

Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Housing/encapsulation for photovoltaic devices</td>
<td>H01L 31/048</td>
</tr>
<tr>
<td>Containers/encapsulation for organic photosensitive devices</td>
<td>H01L 51/448</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Containers not specific to light sensitive devices (microelectronic)</td>
<td>H01L 23/02</td>
</tr>
<tr>
<td>Assemblies consisting of a plurality of individual semiconductor or other solid state devices, e.g. the devices having separate containers</td>
<td>H01L 25/00</td>
</tr>
<tr>
<td>Optical elements or arrangements associated with semiconductor devices sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength specially adapted for the control of electrical energy by such radiation</td>
<td>H01L 31/0232</td>
</tr>
<tr>
<td>Optical elements directly associated or integrated with the PV cell</td>
<td>H01L 31/054</td>
</tr>
<tr>
<td>Light absorption and re-emission at a different wavelength by the optical element directly associated or integrated with the PV cell, e.g. luminescent sheets for up or down-conversion</td>
<td>H01L 31/055</td>
</tr>
<tr>
<td>Packaging for devices classified in H01L 31/14, H01L 31/16</td>
<td>H01L 31/14, H01L 31/16</td>
</tr>
<tr>
<td>Semiconductor devices specially adapted for light emission, characterised by the semiconductor body package</td>
<td>H01L 33/48</td>
</tr>
<tr>
<td>Encapsulation of light emitting devices</td>
<td>H01L 51/52</td>
</tr>
<tr>
<td>Sealing arrangements of electroluminescent light sources</td>
<td>H05B 33/04</td>
</tr>
</tbody>
</table>
**H01L 31/0216**

**Coatings (H01L 31/041 takes precedence)**

**Definition statement**

*This place covers:*

Photosensitive semiconductor devices on which one or more layer(s) are directly deposited - as opposed to "optical elements" which are placed above or upon the device) - e.g. involving electrically passivating properties or optical enhancing properties.

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Provision</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provisions for preventing damage caused by corpuscular radiation, e.g. for space applications</td>
<td>H01L 31/041</td>
</tr>
</tbody>
</table>

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Luminescent layers for photodetectors</td>
<td>H01L 31/02322</td>
</tr>
<tr>
<td>Encapsulation of solar cells</td>
<td>H01L 31/048</td>
</tr>
<tr>
<td>PV devices comprising luminescent layers</td>
<td>H01L 31/055</td>
</tr>
<tr>
<td>Processes or apparatus specially adapted for the manufacture or treatment of these devices or of parts thereof, e.g. passivation methods</td>
<td>H01L 31/18</td>
</tr>
<tr>
<td>Passivation and encapsulation of organic photosensitive devices</td>
<td>H01L 51/448</td>
</tr>
</tbody>
</table>

**Special rules of classification**

If the layer is texturized, then classify in both (subgroup of) H01L 31/0216 and H01L 31/0236.

**H01L 31/02161**

{for devices characterised by at least one potential jump barrier or surface barrier}

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coatings of integrated photosensitive devices ( imagers)</td>
<td>H01L 27/1462</td>
</tr>
</tbody>
</table>
H01L 31/02162
{for filtering or shielding light, e.g. multicolour filters for photodetectors}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Colour filter arrangements of integrated photosensitive devices ( imagers) | H01L 27/14621 |

H01L 31/02164
{for shielding light, e.g. light blocking layers, cold shields for infra-red detectors}

Definition statement
This place covers:
Light shielding layers to protect circuitry, for instance the transistor of the pixel.
Also used to detect and subtract dark current in photodetectors.

References

Limiting references
This place does not cover:

| Optical shielding of integrated devices | H01L 27/14623 |

H01L 31/02165
{using interference filters, e.g. multilayer dielectric filters (interference filters G02B 5/28)}

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Interference filters | G02B 5/28 |

H01L 31/02167
{for solar cells}

Definition statement
This place covers:
Passivation layer or any kind of coating protection specially adapted for photovoltaic cells.
References

**Limiting references**

This place does not cover:

| Special textures or texturization of surfaces | H01L 31/0236 |
| Solar cell encapsulations | H01L 31/048 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Interference filters | G02B 5/28 |

**H01L 31/02168**

{the coatings being antireflective or having enhancing optical properties for the solar cells}

**Definition statement**

This place covers:

Multilayer coatings, e.g. double layer AR coatings for solar cells.

References

**Limiting references**

This place does not cover:

| Special surface textures or texturization methods | H01L 31/0236 |
| Luminescent layers for solar cells | H01L 31/055 |

**H01L 31/0224**

**Electrodes**

**Definition statement**

This place covers:

Electrodes and manufacturing methods thereof.

References

**Limiting references**

This place does not cover:

| Electrodes for organic photosensitive devices | H01L 51/441 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Methods for making electrodes are in | H01L 31/0224 |
| Methods for making a transparent electrode | H01L 31/1884 |
**H01L 31/022408**

{for devices characterised by at least one potential jump barrier or surface barrier}

**Definition statement**

*This place covers:*

Electrodes or electrode structures for photodiodes, phototransistors and photoconductor devices, and the fabrication thereof.

**H01L 31/022425**

{for solar cells}

**Definition statement**

*This place covers:*

Electrode structures for solar cells and fabrication methods.

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Electrode structures</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transparent electrodes (including for solar cells)</td>
<td>H01L 31/022466</td>
</tr>
<tr>
<td>Interconnections between cells within a module when the cells are not integrated on the same substrate</td>
<td>H01L 31/05</td>
</tr>
<tr>
<td>Method for forming transparent electrode</td>
<td>H01L 31/1884</td>
</tr>
<tr>
<td>Electrodes for photo electrochemical cells (DSSC, Grätzel type) for counter electrode</td>
<td>H01G 9/2022</td>
</tr>
</tbody>
</table>

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Interconnection structures of thin film solar cells in a module | H01L 31/046 |

**Special rules of classification**

Methods for forming solar cell electrodes are classified here and not in H01L 31/18, except the method for forming transparent electrode, which is classified in H01L 31/1884.

For electrodes of thin film solar cells, double classification is made in H01L 31/022425 and H01L 31/046, but not for the series interconnection structures of thin film solar cells in a module, which is covered by H01L 31/046.

**H01L 31/022433**

{Particular geometry of the grid contacts}

**Definition statement**

*This place covers:*

Specific patterns of front electrodes.
Special rules of classification
Specific transversal sections of electrodes or back electrodes are covered by H01L 31/022425.

H01L 31/022466
{made of transparent conductive layers, e.g. TCO, ITO layers}

Definition statement
This place covers:
Transparent electrodes for photodetectors and/or solar cells.

References
Limiting references
This place does not cover:

| Method for manufacturing a transparent electrode | H01L 31/1884 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Transparent electrodes for light emitting devices | H01L 33/42 |
| Transparent electrodes for organic light sensitive devices | H01L 51/442 |
| Material composition, e.g. conductive oxides | H01B 1/08 |

Special rules of classification
If both method and material are relevant, then both H01L 31/022466 and H01L 31/1884.
Give this group symbol if some absorption curves or other optical properties of the TCO layers are disclosed.

H01L 31/0232
Optical elements or arrangements associated with the device (H01L 31/0236 takes precedence; for photovoltaic cells H01L 31/054; for photovoltaic modules H02S 40/20)

Definition statement
This place covers:
Optical elements used for focusing, reflecting or diffracting light and associated with the photosensitive device.

References
Limiting references
This place does not cover:

| Surface textures for light trapping effects | H01L 31/0236 |
| Optical elements for photovoltaic cells | H01L 31/054 |
Light-reflecting or light-concentrating means specially adapted for PV modules

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

- Imager structures, e.g. microlenses for CCDs

**Special rules of classification**

Plasmonic structures: if part of Schottky junctions, then see H01L 31/1085 (MSM). If purely optical, then here (or H01L 31/0232)

H01L 31/0232

{comprising luminescent members, e.g. fluorescent sheets upon the device}

**Definition statement**

*This place covers:*

Luminescent element meant for converting incident wavelengths into different wavelengths, better suited to the spectral absorption of the device (so called "up-conversion" or "down-conversion").

**References**

**Limiting references**

*This place does not cover:*

- Luminescent element for solar cells

H01L 31/0236

**Special surface textures**

**Definition statement**

*This place covers:*

- Surface textures specially adapted for light trapping effects, for both photodetectors and solar cell devices
- Texturization methods

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

- Chemical or electrical treatment, e.g. etching, of semiconductors
- Light emitting devices with a roughened surface

**Special rules of classification**

Texturization methods are covered by this group, and not in H01L 31/18.
Synonyms and Keywords
Corrugated surface; protrusions; projections; roughened surface; pyramidal structures (for silicon); light trapping.

H01L 31/024
Arrangements for cooling, heating, ventilating or temperature compensation (for photovoltaic devices H01L 31/052)

Definition statement
This place covers:
Cooling arrangements for photodetectors

References

Limiting references
This place does not cover:

| Cooling arrangements for photovoltaic devices | H01L 31/052 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Cooling apparatuses in general, e.g. arrangement or mounting of refrigeration units | F25D 19/00 |

H01L 31/0248
characterised by their semiconductor bodies

Definition statement
This place covers:
Photodetectors and solar cells having a particular semiconductor body

The "particularity" can be:
- the nature of the material (specific composition, special doping species)
- material shapes or dimensions
- the crystalline structure

Special rules of classification
This group and subgroups thereof are only used for classifying invention information, e.g. not every document dealing with group IV materials is classified H01L 31/028

H01L 31/0256
characterised by the material

Definition statement
This place covers:
Device characterized by the material used as active layer having a specific composition, i.e. the light absorbing semiconductor material
References

Limiting references
This place does not cover:

| Materials which are not active materials | H01L 31/0216 |
| Manufacturing methods                  | H01L 31/18   |
| Organic semiconductor materials         | H01L 51/42   |

H01L 31/0264
Inorganic materials

Definition statement
This place covers:
Inorganic semiconductor materials forming the active part of photosensitive devices, photodetectors and photovoltaic devices

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Organic semiconductor materials | H01L 51/0032 |

H01L 31/028
including, apart from doping material or other impurities, only elements of Group IV of the Periodic System

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Documents relating to the Staebler-Wronski effect | H01L 31/03767 |
| Deposition methods of group IV materials         | H01L 31/1804, H01L 21/02104 |

Special rules of classification
This group covers only devices with specificity in the group IV material. This group symbol is not given as an index code to all documents referring to a photoelectric structure comprising group IV elements.
H01L 31/0284
{comprising porous silicon as part of the active layer(s) (porous silicon as antireflective layer for photodiodes H01L 31/0216; for solar cells H01L 31/02168)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Porous silicon as antireflective layer for photodiodes</td>
<td>H01L 31/0216</td>
</tr>
<tr>
<td>Porous silicon as antireflective layer for solar cells</td>
<td>H01L 31/02168</td>
</tr>
</tbody>
</table>

H01L 31/02966
{including ternary compounds, e.g. HgCdTe}

Definition statement
This place covers:
HgCdTe compounds having a low bandgap, e.g. for IR photodetector

H01L 31/03046
{including ternary or quaternary compounds, e.g. GaAlAs, InGaAs, InGaAsP}

Definition statement
This place covers:
Ternary or quaternary compounds having a specific stoichiometry, absorption spectrum or band gap

H01L 31/0321
{characterised by the doping material (H01L 31/0323, H01L 31/0325 take precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chalcopyrite compounds characterised by the doping material</td>
<td>H01L 31/0323</td>
</tr>
<tr>
<td>Chalcogenide compounds characterised by the doping material</td>
<td>H01L 31/0325</td>
</tr>
</tbody>
</table>
H01L 31/0322
{comprising only A_{III}B_{II}C_{VI} chalcopyrite compounds, e.g. Cu In Se$_2$, Cu Ga Se$_2$, Cu In Ga Se$_2$}

**Definition statement**

*This place covers:*

CIS and CIGS materials and deposition methods.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forming chalcogenide semiconducting materials not being oxides on a substrate</td>
<td>H01L 21/02568</td>
</tr>
<tr>
<td>Heterojunction solar cells including a I-III-VI active layer</td>
<td>H01L 31/0749</td>
</tr>
<tr>
<td>Coating by vacuum evaporation, by sputtering or by ion implantation of sulphides, selenides or tellurides</td>
<td>C23C 14/0623</td>
</tr>
<tr>
<td>Reactive treatment with sulphur or selenium after deposition</td>
<td>C23C 14/5866</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Methods for forming CIS or CIGS are classified here, not in H01L 31/18.

H01L 31/03365
{comprising only Cu$_2$X / CdX heterojunctions, X being an element of Group VI of the Periodic System}

**Definition statement**

*This place covers:*

Cu$_2$O/CdS and Cu$_2$S/CdS heterojunction devices

H01L 31/0352

characterised by their shape or by the shapes, relative sizes or disposition of the semiconductor regions

**Definition statement**

*This place covers:*

Photoelectric devices in which the active layer is characterized by some geometrical aspects.

The substrate or body of the device on which the active layer is formed

Devices comprising nanodots, quantum dots, quantum wires, as active material

Active layers involving quantum effects, e.g. quantum dots and intermediate band solar cells

Photoactive nanotubes or nanowires
Relationships with other classification places

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Geometrical aspects of other parts of the device than active layer and body</td>
<td>H01L 31/0224</td>
</tr>
<tr>
<td>are classified with said other parts, e.g. electrodes</td>
<td></td>
</tr>
<tr>
<td>Semiconductor particles embedded in insulating material</td>
<td>H01L 31/0384</td>
</tr>
<tr>
<td>Nanotubes or nanowires forming an heterojunction with an organic</td>
<td>H01L 51/4266</td>
</tr>
<tr>
<td>semiconductor material</td>
<td></td>
</tr>
</tbody>
</table>

**H01L 31/035236**

**{Superlattices; Multiple quantum well structures}**

**Definition statement**

*This place covers:*

Photodetectors and photovoltaic cells involving superlattices or multiple quantum wells.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor nanoparticles within a matrix</td>
<td>H01L 31/0384</td>
</tr>
</tbody>
</table>

**Synonyms and Keywords**

Superlattices, quantum wells, MQW (multiple quantum wells), quantum dots, quantum wires, quantum boxes, nanodots, nanorods.

**H01L 31/035272**

**{characterised by at least one potential jump barrier or surface barrier}**

**Definition statement**

*This place covers:*

Photodetectors and also solar cells having at least one potential jump barrier.
**H01L 31/035281**

{Shape of the body}

**Definition statement**

*This place covers:*

Devices having special shapes of the device body, e.g. cylindrical or spherical bodies:

![Fig 6 of EP1253649](image)

**H01L 31/03529**

{Shape of the potential jump barrier or surface barrier}

**Definition statement**

*This place covers:*

Sawteeth, interdigitated junctions

![P1005095](image)

**H01L 31/036**

characterised by their crystalline structure or particular orientation of the crystalline planes

**Definition statement**

*This place covers:*

- Polycrystalline semiconductors
- Amorphous materials
- Crystalline particles in an amorphous matrix
- Metallic or insulating substrates used for thin film deposition
Particular orientation of the crystalline planes of e.g. substrates or body in the device:

Figure 1 of EP1302976

Semiconducting whiskers

References

Limiting references

This place does not cover:

| Porous silicon as active material | H01L 31/0284 |

H01L 31/0368

including polycrystalline semiconductors (H01L 31/0392 takes precedence)

References

Limiting references

This place does not cover:

| Thin films deposited on metallic or insulating substrates | H01L 31/0392 |

H01L 31/03682

{including only elements of Group IV of the Periodic System}

Definition statement

This place covers:

Polysilicon devices
H01L 31/0376
including amorphous semiconductors (H01L 31/0392 takes precedence)

References

Limiting references
This place does not cover:

Thin films deposited on metallic or insulating substrates

H01L 31/03762
{including only elements of Group IV of the Periodic System}

Definition statement
This place covers:
Amorphous silicon devices

References

Informative references
Attention is drawn to the following places, which may be of interest for search:

Deposition methods of amorphous silicon

H01L 31/0202, H01L 21/02365, C23G

Special rules of classification
This group symbol is given, if specific aspects of amorphous material are disclosed.

H01L 31/03767
{presenting light-induced characteristic variations, e.g. Staebler-Wronski effect}

Definition statement
This place covers:
Subject-matter which describes the Staebler-Wronski effect or aims at solving problems and drawbacks related to this effect.

H01L 31/0384
including other non-monocrystalline materials, e.g. semiconductor particles embedded in an insulating material (H01L 31/0392 takes precedence)

Definition statement
This place covers:
Semiconductor particles, e.g. nanoparticles, in a dielectric matrix
Semiconductor particles, e.g. nanoparticles, in an inorganic semiconductor matrix
References

Limiting references
This place does not cover:

| Semiconductor devices including thin films | H01L 31/0392 |

Glossary of terms
In this place, the following terms or expressions are used with the meaning indicated:

| MGL | Monograin layer also called monograin membrane, i.e. powder particles embedded within a polymer membrane |

H01L 31/0392
including thin films deposited on metallic or insulating substrates {; characterised by specific substrate materials or substrate features or by the presence of intermediate layers, e.g. barrier layers, on the substrate (textured substrates H01L 31/02366)}

Definition statement
This place covers:
Thin films deposited on "cheap" substrates, e.g. glass, metal, ceramic substrates
Barrier layers used to avoid out-diffusion of impurities from said "cheap" substrates

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| I-III-VI (chalcopyrite) compounds deposited on a flexible substrate | H01L 31/03923 |
| II-VI materials deposition on non-semiconductor substrates | H01L 31/1836 |
| III-V materials deposition on non-semiconductor substrates | H01L 31/1852 |
| Flexible substrates for photoelectrochemical solar cells | H01G 9/2095 |

Special rules of classification
Classification is given with this symbol whenever a detailed substrate is described.

H01L 31/03921
{including only elements of Group IV of the Periodic System}

Definition statement
This place covers:
Non semiconductor substrates on which only group IV thin film devices are deposited, e.g. amorphous silicon devices on metallic or insulating substrates.
H01L 31/04

adapted as photovoltaic [PV] conversion devices (testing thereof during manufacture \{H01L 22/00\}; testing thereof after manufacture \textbf{H02S 50/10}\)

Definition statement

This place covers:

Semiconductor devices sensitive to light and adapted for the direct conversion of the light into electrical energy for the purpose of providing electrical energy (not for light detection purposes).

Relationships with other classification places

This group and subgroups do not cover organic light sensitive devices, which are covered by \textbf{H01L 51/42} as expressed by the limiting reference after \textbf{H01L 31/00}.

This group and subgroups also do not cover electrolytic light sensitive devices, e.g. dye sensitized solar cells, which are covered by \textbf{H01G 9/20}, as expressed by the limiting reference to \textbf{H01G 9/00} after the sub class title of \textbf{H01L}.

References

Limiting references

This place does not cover:

| Testing of PV devices during manufacture | H01L 22/00 |
| Organic solar cells | H01L 51/42 |
| Electrolytic light sensitive devices, e.g. dye sensitized solar cells | H01G 9/20 |
| Testing of PV devices after manufacture | H02S 50/10 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Imager structures consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate | H01L 27/146 |
| Electrodes at the cell level | H01L 31/0224 |
| Devices in which radiation controls flow of current through the device, e.g. photodetectors | H01L 31/08 |
| Production of heat using solar radiation | F24S |
| Measurement of X-radiation, gamma radiation, corpuscular radiation or cosmic radiation with semiconductor detectors | G01T 1/24 |
| Measurement of X-radiation, gamma radiation, corpuscular radiation or cosmic radiation with resistance detectors | G01T 1/26 |
| Measurement of neutron radiation with semiconductor detectors | G01T 3/08 |
| Couplings of light guides with optoelectronic elements | G02B 6/42 |
| Arrangement for obtaining electrical energy from radioactive sources | G21H 1/12 |
| Electrochemical current or voltage generators | \textbf{H01M 6/00 - H01M 16/00} |
Special rules of classification

- The group **H01L 31/04** itself only includes subject-matter where the nature of the light converting material is not clear.
- Devices including photovoltaic cells as power source, wherein the document does not disclose any structural details regarding said photovoltaic devices, should be classified in the relevant groups for said device as such.

Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homojunction</td>
<td>pn junction involving both p and n regions made out of the same material, with the same composition and the same structure (only the doping species change).</td>
</tr>
<tr>
<td>Heterojunction</td>
<td>pn junction involving two different materials, the difference lying in the crystal structure and/or the composition (example: p-type amorphous silicon / n-type crystalline silicon).</td>
</tr>
<tr>
<td>P-i-n structure</td>
<td>P-N junction with thick intrinsic layer in between, whereby the intrinsic interlayer is the major part of the absorbing layer, i.e. not Heterojunction with Intrinsic Thin-layer solar cells.</td>
</tr>
<tr>
<td>Heterojunction with Intrinsic Thin-layer solar cells</td>
<td>P-N structures including a very thin intrinsic inter-layer, which is not the absorbing layer of the structure.</td>
</tr>
<tr>
<td>Tandem solar cell</td>
<td>a plurality of junctions are monolithically stacked on one another (for lateral integration, see <strong>H01L 27/142</strong>).</td>
</tr>
<tr>
<td>Schottky contact</td>
<td>rectifying (non-ohmic) metal/semiconductor contact.</td>
</tr>
<tr>
<td>Group 14 elements</td>
<td>formerly known as Group IVA elements (C, Si, Ge, Sn, Pb).</td>
</tr>
<tr>
<td>Conversion devices</td>
<td>light sensitive devices specially adapted for conversion of light into electrical energy, not for the purpose of light detection.</td>
</tr>
<tr>
<td>MIS</td>
<td>Metal Insulator Semiconductor.</td>
</tr>
</tbody>
</table>

Synonyms and Keywords

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si, α-Si</td>
<td>amorphous silicon</td>
</tr>
<tr>
<td>c-Si</td>
<td>crystalline silicon</td>
</tr>
<tr>
<td>mc-Si, muc-Si</td>
<td>microcrystalline silicon</td>
</tr>
<tr>
<td>poly-Si</td>
<td>polycrystalline silicon</td>
</tr>
<tr>
<td>PIN, p-i-n</td>
<td>P-N junction with thick intrinsic layer in between.</td>
</tr>
<tr>
<td>AlBIIIICVI compound</td>
<td>I-III-VI compound, chalcogenides, chalcopyrites</td>
</tr>
<tr>
<td>CIS</td>
<td>CuInSe2</td>
</tr>
<tr>
<td>CIGS</td>
<td>CuInGaSe2</td>
</tr>
<tr>
<td>CIGSS</td>
<td>CuInGaSSe</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent conducting oxide</td>
</tr>
<tr>
<td>ITO</td>
<td>Indium Tin Oxide</td>
</tr>
<tr>
<td>AZO</td>
<td>Aluminium doped Zinc Oxide</td>
</tr>
<tr>
<td>GZO</td>
<td>Gallium doped Zinc Oxide</td>
</tr>
<tr>
<td>QW</td>
<td>Quantum well</td>
</tr>
</tbody>
</table>
MQW | Multiple Quantum Well
---|---
HIT | Heterojunction with Intrinsic Thin-layer
PERL solar cell | Passivated Emitter Rear Locally Diffused solar cell
ARC | Anti-reflective coating
MPPT | Maximum Power Point Tracking
MWT | Metal Wrap Through
FMWT | Front Metal Wrap Through
EWT | Emitter Wrap Through
IBC | Interdigitated Back Contact (solar cells)

In patent documents, the following words/expressions are often used with the meaning indicated:

"solar cells" | "photovoltaic cells"

**H01L 31/041**

Provisions for preventing damage caused by corpuscular radiation, e.g. for space applications

**Definition statement**

This place covers:

- Photovoltaic devices specially adapted for space applications.
- Special features to improve the radiation resistance of the PV cell to avoid radiation damage

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Semiconductor devices sensitive to very short wavelengths, e.g. X-rays, gamma-rays or corpuscular radiation</th>
<th>H01L 31/115</th>
</tr>
</thead>
<tbody>
<tr>
<td>Space applications, e.g. power supply for satellites made of solar cell modules</td>
<td>B64G 1/00</td>
</tr>
</tbody>
</table>

**H01L 31/042**

PV modules or arrays of single PV cells (supporting structures for PV modules [H02S 20/00](#))

**Definition statement**

This place covers:

- PV cell arrays, modules or panels. The PV cells used here are normally of the crystalline-polycrystalline type (bulk cells), e.g. silicon solar cells
- Special configuration of the PV cells array,
- Special electrical connections of the PV cells in a module
- Circuitry integrated with the PV cells
- Specific dispositions or shapes of adjacent cells within the module
- Special configuration or structure of PV modules, adapted for special applications, e.g. solar hats
• Bypass diodes associated to the interconnections between cells of the module.

References

Limiting references

This place does not cover:

| Supporting structures for PV modules | H02S 20/00 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Circuit arrangements for solar cells | H01L 31/02021 |

Synonyms and Keywords

In patent documents, the following words/expressions are often used as synonyms:

- "modules" and "panels"

H01L 31/044

including bypass diodes (bypass diodes in the junction box H02S 40/34)

Definition statement

This place covers:

Bypass diodes in PV modules, e.g. bypass diodes for a string of PV cells in a PV module

Example:
References

Limiting references

This place does not cover:

| bypass diodes in the junction box | H02S 40/34 |

**H01L 31/0443**

comprising bypass diodes integrated or directly associated with the devices, e.g. bypass diodes integrated or formed in or on the same substrate as the photovoltaic cells

**Definition statement**

This place covers:

Bypass diodes in PV modules, e.g. integrated with thin film solar cells.

Example:

![Diagram with labeled parts B, C, B1, B2, B3, C1, C2, C3, 16, 17, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 20, 21, 331](image)

(B: bypass diodes, C: plurality of thin film solar cells)

**H01L 31/0445**

including thin film solar cells, e.g. single thin film a-Si, CIS or CdTe solar cells

**Definition statement**

This place covers:

PV modules or arrays of single PV cells including inorganic thin film solar cells, e.g. single thin film a-Si, CIS or CdTe solar cells.
Example:

**H01L 31/046**

PV modules composed of a plurality of thin film solar cells deposited on the same substrate

**Definition statement**

*This place covers:*

PV modules composed of a plurality of inorganic thin film solar cells deposited on the same substrate and electrically connected together, e.g. thin film a-Si, CIS or CdTe solar cells.

Example:
H01L 31/0463

characterised by special patterning methods to connect the PV cells in a module, e.g. laser cutting of the conductive or active layers

Definition statement

This place covers:

specific patterning methods (like laser trimming, chemical etching) which aims at forming a module from a plurality of (interconnected) adjacent thin film solar cells from initially continuous thin films.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method of deposition of CIS compounds</td>
<td>H01L 31/0322</td>
</tr>
<tr>
<td>Thin films deposited on metallic or insulating substrates</td>
<td>H01L 31/0392</td>
</tr>
<tr>
<td>Method of deposition of amorphous silicon cells</td>
<td>H01L 31/202,</td>
</tr>
<tr>
<td></td>
<td>H01L 31/204</td>
</tr>
<tr>
<td>Roll to roll deposition of amorphous silicon device</td>
<td>H01L 31/206</td>
</tr>
</tbody>
</table>
**H01L 31/0465**

comprising particular structures for the electrical interconnection of adjacent PV cells in the module (H01L 31/0463 takes precedence)

**Definition statement**

This place covers:

specific interconnection structures interconnecting adjacent thin film solar cells, e.g. insulating spacer to avoid short-circuits between cells.

Examples:

(Reference numeral 290: electrical interconnection structure)
References

Limiting references

This place does not cover:

specific patterning methods to interconnect adjacent thin film solar cells in a thin film PV module

H01L 31/0463

H01L 31/0468

comprising specific means for obtaining partial light transmission through the module, e.g. partially transparent thin film solar modules for windows

Definition statement

This place covers:

Example:

H01L 31/047

PV cell arrays including PV cells having multiple vertical junctions or multiple V-groove junctions formed in a semiconductor substrate

Definition statement

This place covers:

Solar cells formed in a semiconductor substrate (bulk type) and being separated by V-grooves or having a plurality of vertical junctions.
**H01L 31/0475**

PV cell arrays made by cells in a planar, e.g. repetitive, configuration on a single semiconductor substrate; PV cell microarrays (PV modules composed of a plurality of thin film solar cells deposited on the same substrate [**H01L 31/046**])

**Definition statement**

*This place covers:*

Photovoltaic cell arrays made by cells in a planar, e.g. repetitive, configuration on a single semiconductor substrate; PV cell microarrays.
Examples:

(Reference numerals 5: N-doping, 3: P-doping)
References

Limiting references

This place does not cover:

Photovoltaic modules composed of a plurality of thin film solar cells deposited on the same substrate

H01L 31/046

H01L 31/048

Encapsulation of modules

Definition statement

This place covers:

- PV devices comprising encapsulation layers specially adapted for protecting the photovoltaic module, e.g. details of laminations, materials in-between; methods for obtaining them:

- Housings for PV cells:
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Encapsulation of photodetectors or photodiodes</td>
<td>H01L 31/0203</td>
</tr>
<tr>
<td>Coatings at the cell level, e.g., for passivation or antireflection</td>
<td>H01L 31/02167</td>
</tr>
<tr>
<td>Back side reflectors for PV cells</td>
<td>H01L 31/056</td>
</tr>
<tr>
<td>Processes or apparatus peculiar to the manufacture or treatment of these devices or of parts thereof</td>
<td>H01L 31/18</td>
</tr>
<tr>
<td>Encapsulation of organic solar cells</td>
<td>H01L 51/448</td>
</tr>
<tr>
<td>Layered products essentially comprising sheet glass, or glass</td>
<td>B32B 17/00</td>
</tr>
<tr>
<td>Synthetic resin laminates</td>
<td>B32B 27/00</td>
</tr>
<tr>
<td>Adhesives per se</td>
<td>C09J</td>
</tr>
<tr>
<td>Materials for sealing or packing joints or covers</td>
<td>C09K 3/10</td>
</tr>
</tbody>
</table>

H01L 31/049

Protective back sheets

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layered sheets per se</td>
<td>B32B</td>
</tr>
</tbody>
</table>
H01L 31/05

Electrical interconnection means between PV cells inside the PV module, e.g. series connection of PV cells (electrodes H01L 31/0224; electrical interconnection of thin film solar cells formed on a common substrate H01L 31/046; particular structures for electrical interconnecting of adjacent thin film solar cells in the module H01L 31/0465; electrical interconnection means specially adapted for electrically connecting two or more PV modules H02S 40/36)

Definition statement

This place covers:

- The serial interconnection of PV cells (10) inside a PV module (100), e.g.:

- Specific interconnection materials for electrically interconnecting PV cells
- Wiring substrates for serial connection of back contacted solar cells
- Methods for interconnecting PV cells

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Electrodes for PV cells</th>
<th>H01L 31/022425</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical interconnection of thin film solar cells formed on a common substrate</td>
<td>H01L 31/046</td>
</tr>
<tr>
<td>Particular structures for electrical interconnecting of adjacent thin film solar cells in the module</td>
<td>H01L 31/0465</td>
</tr>
<tr>
<td>Electrical interconnection means specially adapted for electrically connecting two or more PV modules</td>
<td>H02S 40/36</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Soldering in general</th>
<th>B23K</th>
</tr>
</thead>
</table>
Conductive pastes as such
Materials used as interconnection in printed circuits

**H01L 31/052**

Cooling means directly associated or integrated with the PV cell, e.g. integrated Peltier elements for active cooling or heat sinks directly associated with the PV cells (cooling means in combination with the PV module H02S 40/42)

**Definition statement**

*This place covers:*
- PV cells comprising active cooling means, e.g. peltier elements, a liquid or gaseous coolant, directly associated or integrated with the cell
- PV cells comprising passive cooling means, e.g. heat sinks, directly associated or integrated with the cell

**References**

**Limiting references**

*This place does not cover:*

Cooling means in combination with the PV module H02S 40/42

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

- Cooling means using Peltier elements for semiconductor devices in general H01L 23/38
- Cooling means for photodetectors or photodiodes H01L 31/024
- Optical elements directly associated or integrated with the PV cell, e.g. light reflecting and light concentrating means H01L 31/054
- Thermoelectric devices operating with Peltier or Seebeck-effect only H01L 35/28

**H01L 31/0525**

including means to utilise heat energy directly associated with the PV cell, e.g. integrated Seebeck elements

**Definition statement**

*This place covers:*

Hybrid solar devices, i.e. PV cells including means for utilising thermal energy, e.g. by using Seebeck elements

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

- Using solar heat per se F24S 20/00
Means to utilise heat energy directly associated with the PV module \[ H02S\ 40/44 \]

**H01L 31/053**

Energy storage means directly associated or integrated with the PV cell, e.g. a capacitor integrated with a PV cell (energy storage means associated with the PV module \[ H02S\ 40/38 \])

**Definition statement**

This place covers:
Photovoltaic devices including a battery to store electrical energy

**References**

**Limiting references**

This place does not cover:

Energy storage means associated with the PV module \[ H02S\ 40/38 \]

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accumulators structurally combined with charging apparatus</td>
<td>[ H01M\ 10/465 ]</td>
</tr>
<tr>
<td>Circuit arrangements for charging batteries with solar cells</td>
<td>[ H02J\ 7/35 ]</td>
</tr>
</tbody>
</table>

**H01L 31/054**

Optical elements directly associated or integrated with the PV cell, e.g. light-reflecting means or light-concentrating means

**Definition statement**

This place covers:
PV cells comprising solar concentrators, lenses and reflectors, e.g. Fresnel lenses:

![Figure 2A](image-url)
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Antireflective coatings for light sensitive devices | H01L 31/0216 |
| Concentrating means for semiconductor photodetectors | H01L 31/0232 |
| Concentrators for solar heat collectors | F24S 23/00 |
| Optical elements per se | G02B |

H01L 31/055

where light is absorbed and re-emitted at a different wavelength by the optical element directly associated or integrated with the PV cell, e.g. by using luminescent material, fluorescent concentrators or up-conversion arrangements

Definition statement

This place covers:

PV cells comprising coatings or separate members, which change the wavelengths of the incident light, making it more suitable for absorption by the associated PV cell, e.g. fluorescent concentrators:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Luminescent member for photodetectors, e.g. for X-ray detectors | H01L 31/0232 |
| Luminescent, e.g. electroluminescent, chemiluminescent materials | C09K 11/00 |

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| Up conversion / down conversion | Incident photons are converted into photons of higher/respectively lower energies (shorter, respectively longer wavelengths). |
Synonyms and Keywords

In patent documents, the following words/expressions are often used as synonyms:

• "photoluminescent materials", "luminescent materials" and "phosphorescent materials"

H01L 31/056

the light-reflecting means being of the back surface reflector [BSR] type

Definition statement

This place covers:

PV cells comprising light-reflecting means sending back the light that already went through the PV cell, e.g. an Ag electrode in order to reflect the light on the back of the PV cell.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Electrodes for PV cells | H01L 31/022425 |

Special rules of classification

When an electrode has a specific structure/composition specially adapted for acting as back surface reflector, the document should be classified in H01L 31/056 and additionally in H01L 31/022425.

H01L 31/06

characterised by at least one potential-jump barrier or surface barrier

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Photovoltaic cell arrays including PV cells having multiple vertical junctions or multiple V-groove junctions formed in a semiconductor substrate | H01L 31/047 |
**H01L 31/061**

the potential barriers being of the point-contact type (**H01L 31/07** takes precedence)

**Definition statement**

This place covers:

Point contact solar cells:

See for instance EP2120269.

**References**

**Limiting references**

This place does not cover:

| Devices having potential barriers being of the Schottky type | **H01L 31/07** |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Electrodes for light sensitive devices as such and manufacturing methods | **H01L 31/022425** |

**Figure 1.** A cross-section of a texturized, point-contact solar cell, with front and back surface diffusions.
Special rules of classification
Concerning the meaning of "point contact": the point contact in this group must be ohmic.

H01L 31/062
the potential barriers being only of the metal-insulator-semiconductor type

Definition statement
This place covers:
Photovoltaic devices where the potential barrier consists in a metal-insulator-semiconductor (MIS) structure:

(US2006102972)

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

Photodetectors being of the conductor-insulator- semiconductor type, e.g. having a MIS structure

Synonyms and Keywords
MIS: Metal - Insulator - Semiconductor; Tunnel (contact, oxide, structure,...)
Inversion layers; Field effect.
**H01L 31/065**

the potential barriers being only of the graded gap type

**Definition statement**

This place covers:
Photovoltaic devices where the absorbing part of the device involves a layer with a graded bandgap:

![Bandgap Diagram](image)

**Special rules of classification**

When classifying in H01L 31/065 (graded bandgap), subject matter related to the junction type is additionally classified in the corresponding other subgroups provided for under H01L 31/06.

Example: Solar cells having a p-i-n structure with a graded band gap intrinsic region, are classified in H01L 31/065 and additionally in H01L 31/075.

**H01L 31/068**

the potential barriers being only of the PN homojunction type, e.g. bulk silicon PN homojunction solar cells or thin film polycrystalline silicon PN homojunction solar cells

**Definition statement**

This place covers:
Photovoltaic devices where the potential barrier is a p-n junction involving one single material (same composition and same crystal structure) with different dopants (so called "homojunction"), e.g. silicon homojunction p-n solar cells.
Example of bulk silicon solar cell:

(Fig 1 of EP2341549)

Example of thin film solar cell:

(Figure 2c from document US2002/036011)

Classification of specific technical subjects

Amorphous silicon is not considered to be the same material as crystalline silicon, because a-Si and c-Si have a different crystal structure, and a different band gap. An a-Si / c-Si structure is, therefore, considered a heterojunction, which are covered by H01L 31/072.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Multiple homojunctions</th>
<th>H01L 31/0687</th>
</tr>
</thead>
<tbody>
<tr>
<td>III - V homo junctions</td>
<td>H01L 31/0693</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Devices with potential barriers being only of the PN heterojunction type, e.g. a-Si / c-Si solar cell</th>
<th>H01L 31/072</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photodetectors with p-n-homojunction structure</td>
<td>H01L 31/103</td>
</tr>
<tr>
<td>Methods for manufacturing homojunction solar cells</td>
<td>H01L 31/18</td>
</tr>
</tbody>
</table>
Special rules of classification

All homojunction solar cells are classified in H01L 31/068 and additionally in H01L 31/0236, H01L 31/0224, H01L 31/02167, and H01L 31/02168, whenever appropriate.

Multiple homojunctions are covered by H01L 31/0687 unless one of the junctions is of special interest as such. In that case, the subject matter is additionally classified in H01L 31/068.

H01L 31/0687

Multiple junction or tandem solar cells

Definition statement

This place covers:

Tandem homojunction solar cells, i.e. a plurality of homojunction cells deposited on one another so as to form a single integrated photovoltaic structure, each cell having a different bandgap and thus a different spectral sensitivity. Tunnel junctions between cells usually ensure the electrical connection and the current flow between the cells.

(Fig 1 of EP1469528)

Relationships with other classification places

- stacked solar cells, meaning different solar cells mechanically stacked on one another, not integrated as a single structure: H01L 31/043, see figure below)
References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stacked solar cells (see figure above), i.e. different solar cells</td>
<td>H01L 31/0687</td>
</tr>
<tr>
<td>mechanically stacked on one another, not integrated as a single structure.</td>
<td></td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solar cells laterally integrated on a common substrate</td>
<td>H01L 31/0475</td>
</tr>
<tr>
<td>Heterojunctions tandem solar cells</td>
<td>H01L 31/0725</td>
</tr>
<tr>
<td>p-i-n tandem solar cells</td>
<td>H01L 31/076</td>
</tr>
<tr>
<td>Tandem solar cells comprising sub-cells each having a different kind of</td>
<td>H01L 31/078</td>
</tr>
<tr>
<td>potential barrier</td>
<td></td>
</tr>
</tbody>
</table>

Special rules of classification

III-V (homojunction) tandem solar cells are classified both in H01L 31/0687 and additionally in H01L 31/0693, if all the cells of the tandem structure are III-V homojunction cells.

**H01L 31/0693**

the devices including, apart from doping material or other impurities, only A\textsubscript{III}B\textsubscript{V} compounds, e.g. GaAs or InP solar cells

Definition statement

This place covers:

Photovoltaic PN homojunction devices including, apart from doping material or other impurities, only A\textsubscript{III}B\textsubscript{V} compounds, e.g. n-GaAs / p- GaAs.
Space solar cells, concentrator solar cells

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| III - V heterojunctions solar cells, i.e. solar cells involving two different III-V materials within one junction | H01L 31/0735 |

Special rules of classification

III-V (homojunction) tandem solar cells are classified both in H01L 31/0687 and additionally in H01L 31/0693, if all the cells of the tandem structure are III-V homojunction cells.

**H01L 31/07**

the potential barriers being only of the Schottky type

Definition statement

This place covers:
Photovoltaic devices where the junction consists in a Schottky barrier (rectifying metal-semiconductor junction).

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Photodetectors with Schottky structure | H01L 31/108 |

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| Schottky contact | metal-semiconductor structure involving a potential barrier (that is, not ohmic). The Schottky metal is both a part of the junction and an electrode. |

**H01L 31/072**

the potential barriers being only of the PN heterojunction type

Definition statement

This place covers:
Photovoltaic devices where the junction consists in a p-n structure involving two different materials (compositionally and/or structurally), thereby forming a so called heterojunction.

Relationships with other classification places

The different heterojunctions types are dispatched in the subgroups H01L 31/072 and subgroups and H01L 31/0336 and subgroups.
References

Limiting references
This place does not cover:

- P-i-n solar cell structures

Informative references
Attention is drawn to the following places, which may be of interest for search:

- Materials of the semiconductor bodies
- Heterojunction photodetectors

H01L 31/0725
Multiple junction or tandem solar cells

Definition statement
This place covers:

Tandem heterojunction solar cells, i.e. photovoltaic structures consisting of a plurality of heterojunctions cells (and only heterojunction solar cells) deposited on one another so as to form a single integrated photovoltaic structure, each cell having normally a different bandgap and a different spectral sensitivity.

References

Limiting references
This place does not cover:

- Stacked solar cells, i.e. different solar cells mechanically stacked on one another, not integrated as a single structure

Informative references
Attention is drawn to the following places, which may be of interest for search:

- Solar cells laterally integrated on a common substrate
- Tandem homojunction solar cells
- P-i-n tandem solar cells
- Tandem solar cells comprising sub-cells each having a different kind of potential barrier

H01L 31/073
comprising only A\textsubscript{II}B\textsubscript{VI} compound semiconductors, e.g. CdS/CdTe solar cells

Definition statement
This place covers:

Heterojunction photovoltaic device wherein the heterojunction barrier consists in two different II-VI compound materials.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>II-VI heterojunction photodetectors</td>
<td>H01L 31/109</td>
</tr>
</tbody>
</table>

H01L 31/0735

comprising only $A_{III}B_{V}$ compound semiconductors, e.g. GaAs/AlGaAs or InP/GaInAs solar cells

Definition statement

This place covers:

Heterojunction photovoltaic devices wherein the heterojunction consists in two different III-V compound materials.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>III-V heterojunction photodetectors</td>
<td>H01L 31/109</td>
</tr>
</tbody>
</table>

H01L 31/074

comprising a heterojunction with an element of Group IV of the Periodic System, e.g. ITO/Si, GaAs/Si or CdTe/Si solar cells

Definition statement

This place covers:

Heterojunction photovoltaic devices wherein the heterojunction consists in two different materials, only one of them being silicon or another Group IV element or alloy.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heterojunction comprising only Group IV materials</td>
<td>H01L 31/0745, H01L 31/0747</td>
</tr>
<tr>
<td>III-V heterojunction photodetectors</td>
<td>H01L 31/109</td>
</tr>
</tbody>
</table>

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

Group IVA is also referred to as Group 14 (new nomenclature).
**H01L 31/0745**

comprising a $A_{IV}B_{IV}$ heterojunction, e.g. Si/Ge, SiGe/Si or Si/SiC solar cells

**Definition statement**

*This place covers:*

Heterojunction photovoltaic devices wherein the heterojunction barrier consists in two different group IV materials (elements or alloys).

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| AIV/BIV heterojunction photodetectors | H01L 31/109 |

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

Group IVA is also referred to as group 14 (new nomenclature).

**H01L 31/0747**

comprising a heterojunction of crystalline and amorphous materials, e.g. heterojunction with intrinsic thin layer or HIT® solar cells; solar cells

**Definition statement**

*This place covers:*

Heterojunction photovoltaic devices wherein the heterojunction barrier consists in two different group IV materials with different crystalline structures (with or without a thin intrinsic interlayer in-between).

Example: HIT® solar cell:
Limiting references

This place does not cover:

- P-i-n solar cells with the intrinsic part composed of one amorphous sublayer and one microcrystalline sublayer, both being absorption layers (meaning of similar thicknesses)

Informative references

Attention is drawn to the following places, which may be of interest for search:

- AIV/BIV heterojunction photodetectors

H01L 31/0749

including a A\text{II}B\text{III}C\text{VI} compound, e.g. CdS/CulnSe$_2$ [CIS] heterojunction solar cells

Definition statement

This place covers:
- Heterojunction photovoltaic devices wherein the heterojunction barrier includes at least one I-III-VI compound

H01L 31/075

the potential barriers being only of the PIN type

Definition statement

This place covers:
- Photovoltaic devices wherein the potential barrier consists of a p-i-n structure, the intrinsic layer being the light absorbing layer.
NB: most solar cells having p-i-n structure are made of a-Si with a thicker i layer between thinner p and n layers.

Classification of specific technical subjects

p-n structures including an very thin intrinsic inter-layer, which is not the absorbing layer of the structure, e.g. HIT® solar cells, are considered to be PN heterojunctions, which are covered by group H01L 31/0747.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Photodetectors with p-i-n structure | H01L 31/105 |

Special rules of classification

If all p, i and n layers are crystalline, i.e. poly- or monocrystalline, not microcrystalline, then H01L 31/077.

H01L 31/076

Multiple junction or tandem solar cells

Definition statement

This place covers:

- Tandem p-i-n solar cells, i.e. a plurality of p-i-n structures deposited on one another so as to form a single integrated photovoltaic structure, each cell having normally a different bandgap and therefore different spectral sensitivity.

References

Limiting references

This place does not cover:

| Stacked solar cells (see figure below), i.e. different solar cells mechanically stacked on one another, not integrated as a single structure. | H01L 31/046 |
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Solar cells laterally integrated on a common substrate | H01L 31/0475 |
| Tandem solar cells comprising sub-cells each having a different kind of potential barrier | H01L 31/078 |
| Multiple wavelength photodetectors | H01L 31/101 |
| P-i-n photodetectors | H01L 31/105 |

**H01L 31/077**

the devices comprising monocrystalline or polycrystalline materials

**Definition statement**

This place covers:
Photovoltaic p-i-n structures wherein at least one of the active layers is crystalline.

**References**

**Limiting references**

This place does not cover:

| P-n structure with very thin intrinsic interlayer which does not act as the absorbing region of the structures, e.g. in HIT® solar cells | H01L 31/0747 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Mechanically stacked on one another | H01L 31/046 |
| Photodetectors with p-i-n structure | H01L 31/105 |

**H01L 31/078**

including different types of potential barriers provided for in two or more of groups **H01L 31/062 - H01L 31/075**

**Definition statement**

This place covers:
Tandem solar cells with different junction types, e.g. one p-i-n sub-cell and one heterojunction sub-cell integrated on one another. Normally, all type of tandem solar cells which are not classified in H01L 31/0687, H01L 31/0725 or H01L 31/076).

Normally, all types of tandem solar cells which are not classified in H01L 31/0687, H01L 31/0725 or H01L 31/076 are classified here.
**H01L 31/08**

In which radiation controls flow of current through the device, e.g. photoresistors

**Definition statement**

*This place covers:*

Photosensitive devices specially adapted for detection of photons.

Photoconductors devices not having a potential barrier Photodetection devices involving one or more potential barriers, e.g. photodiodes, phototransistors

All wavelengths, i.e. terahertz (far IR), IR, visible, UV, X rays, gamma, corpuscular radiation is covered.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Integrated photosensitive devices ( imagers ) | H01L 27/146 |
| Pyrometry (infrared radiation measurements) | G01J 5/20, G01J 5/28 |
| Photometry | G01N 1/00 |
| Sensors for corpuscular radiation, X-rays or gamma rays as a whole (including circuitry) | G01T 1/00 |

**Glossary of terms**

*In this place, the following terms or expressions are used with the meaning indicated:*

| Photoconductive | the electrical conductivity of the material changes when light is absorbed by said material |

**H01L 31/085**

{the device being sensitive to very short wavelength, e.g. X-ray, Gamma-rays}

**Definition statement**

*This place covers:*

Photoconductive devices, involving no junction, sensitive to very short wavelengths.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Photodiode arrays sensitive to short wavelength | H01L 27/14658 |
| Photoconductor arrays sensitive to short wavelengths | H01L 27/14676 |
| Solar cells | H01L 31/04 |
| Devices sensitive to infrared, visible or UV light | H01L 31/09 |
Measuring radiation intensity of very short wavelengths radiations with semiconductor devices

H01L 31/09

Devices sensitive to infra-red, visible or ultraviolet radiation (H01L 31/101 takes precedence)

Definition statement
This place covers:
Photoconductive devices, involving no junction, sensitive to infrared, visible and UV light.

References

Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Devices comprising at least one potential jump barrier, e.g. photodiodes</th>
<th>H01L 31/101</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bipolar phototransistors</td>
<td>H01L 31/11</td>
</tr>
<tr>
<td>Phototyristors</td>
<td>H01L 31/111</td>
</tr>
<tr>
<td>Field effect phototransistors</td>
<td>H01L 31/112</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Solar cells</th>
<th>H01L 31/04</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photoconductive devices sensitive to wavelengths not being IR, visible or UV, i.e. being very short wavelength and corpuscular radiations</td>
<td>H01L 31/085</td>
</tr>
<tr>
<td>Photodiodes sensitive to wavelengths not being IR, visible or UV, i.e. being very short wavelength and corpuscular radiations</td>
<td>H01L 31/115</td>
</tr>
<tr>
<td>Radiation pyrometer using semiconductor devices</td>
<td>G01J 5/20</td>
</tr>
</tbody>
</table>

H01L 31/10

characterised by at least one potential-jump barrier or surface barrier, e.g. phototransistors

Definition statement
This place covers:
Photodetecting devices for IR, visible and UV and very short wavelength or particles, comprising at least one potential barrier, e.g. p-n homojunction, heterojunction, Schottky junction, p-i-n structure

Photodiodes (one barrier)
Bipolar photo transistors (two barriers)
Photo thyristors (three barriers)
Field effect photo transistors (junction or MIS transistors).
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Integrated devices, e.g. imagers</th>
<th>H01L 27/146</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photoconductors</td>
<td>H01L 31/08, H01L 31/09</td>
</tr>
<tr>
<td>Photometry using radiation detectors</td>
<td>G01J 1/42</td>
</tr>
<tr>
<td>Radiation pyrometer using semiconductor devices</td>
<td>G01J 5/20</td>
</tr>
<tr>
<td>Photometry (not just the photosensitive semiconducting part, but also circuitry and other aspects of sensors)</td>
<td>G01N 1/00</td>
</tr>
<tr>
<td>Radiation sensors (not just the photosensitive semiconducting part, but also circuitry and other aspects of sensors)</td>
<td>G01T 1/00, G01T 3/00</td>
</tr>
<tr>
<td>Semiconductor radiation intensity detectors, e.g. for very short wavelengths</td>
<td>G01T 1/24</td>
</tr>
<tr>
<td>Measuring spatial distribution of X-rays or nuclear radiations with semiconductor detectors</td>
<td>G01T 1/366</td>
</tr>
<tr>
<td>Semiconductor neutron detector</td>
<td>G01T 3/08</td>
</tr>
</tbody>
</table>

H01L 31/101

Devices sensitive to infra-red, visible or ultra-violet radiation

Definition statement

This place covers:
Multijunction photodetectors, eg. multispectral photodiodes

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Multicolour (multispectral) imagers with stacked pixels | H01L 27/14647, H01L 27/14652 |

H01L 31/103

the potential barrier being of the PN homojunction type

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Photodiode integrated with other components (for instance the transistor in a pixel) | H01L 27/146 |
| P-n homojunction solar cells | H01L 31/068 |
Special rules of classification

In case the photosensing part (pixel) of an integrated device (imager) is described and considered to contain important features, the document is also classified in H01L 31/10 and subgroups.

H01L 31/12

structurally associated with, e.g. formed in or on a common substrate with, one or more electric light sources, e.g. electroluminescent light sources, and electrically or optically coupled thereto (semiconductor devices with at least one potential barrier or surface barrier adapted for light emission H01L 33/00; amplifiers using electroluminescent element and photocell H03F 17/00; electroluminescent light sources per se H05B 33/00)

Definition statement

This place covers:
Devices including light emitting source(s) as well as photodetector(s) on a common substrate. This specific code is used when it is unclear which device controls the other (emitting device controls photosensitive device or the other way round).

References

Limiting references

This place does not cover:
Combination of organic light sensitive components with organic light emitting components, e.g. optocoupler H01L 27/288

Informative references

Attention is drawn to the following places, which may be of interest for search:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Assemblies of opto-electronic devices (not integrated on the same substrate, only juxtaposed, and not electrically nor optically coupled)</td>
<td>H01L 25/167</td>
</tr>
<tr>
<td>Semiconductor devices with at least one potential barrier or surface barrier adapted for light emission</td>
<td>H01L 33/00</td>
</tr>
<tr>
<td>Coupling light guides with opto-electronic elements</td>
<td>G02B 6/42</td>
</tr>
<tr>
<td>Amplifiers using electroluminescent element and photocell</td>
<td>H03F 17/00</td>
</tr>
<tr>
<td>Electronic switching using opto-electronic devices</td>
<td>H03K 17/968</td>
</tr>
<tr>
<td>Optical interconnects</td>
<td>H04B 10/801</td>
</tr>
<tr>
<td>Electroluminescent light sources per se</td>
<td>H05B 33/00</td>
</tr>
</tbody>
</table>

H01L 31/125

{Composite devices with photosensitive elements and electroluminescent elements within one single body}

Definition statement

This place covers:
Devices wherein the light source is an electroluminescent element, e.g. a LED device.
H01L 31/14

the light source or sources being controlled by the semiconductor device sensitive to radiation, e.g. image converters, image amplifiers or image storage devices

**Definition statement**

*This place covers:*

Devices wherein the signal from the photodetector is used for controlling the emission of light from the light source.

**Special rules of classification**

Details of containers and/or encapsulation for these devices (including light source(s) and photodetector(s) are only classified here, not in H01L 31/0203).

H01L 31/147

the light sources and the devices sensitive to radiation all being semiconductor devices characterised by at least one potential or surface barrier

**Definition statement**

*This place covers:*

Combinations of LED and photodiode, both devices optically coupled, when the signal from the photodiode controls the light emission from the LED.

H01L 31/153

formed in, or on, a common substrate

**Definition statement**

*This place covers:*

Integrated combinations of LED and photodiode in/on the same substrate, both devices optically coupled, when the signal from the photodiode controls the light emission from the LED.

H01L 31/16

the semiconductor device sensitive to radiation being controlled by the light source or sources

**Definition statement**

*This place covers:*

Devices, wherein the light from the light source is sent to the photodetector which gives an electrical signal.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Assemblies of opto-electronic devices, not being integrated on the same substrate, only juxtaposed | H01L 25/16 |
Proximity sensors
Coupling light guides with opto-electronic elements
Electronic switching or gating using opto-electronic devices

Special rules of classification
Details of containers and/or encapsulation for these devices (including light source(s) and photodetector(s) are only classified here, not in H01L 31/0203).

H01L 31/18
Processes or apparatus peculiar to the manufacture or treatment of these devices or of parts thereof (not peculiar thereto H01L 21/00)

References
Informative references
Attention is drawn to the following places, which may be of interest for search:
Testing of photovoltaic devices, e.g. of PV modules or single PV cells

H01L 31/1804
{comprising only elements of Group IV of the Periodic System}

Definition statement
This place covers:
Deposition, etching, patterning, doping of group IVA (group 14) elements or alloys as parts of photosensitive devices.

References
Limiting references
This place does not cover:
Heat treatments, e.g. dopant activation, crystallization

Informative references
Attention is drawn to the following places, which may be of interest for search:
Etching, cleaning, patterning of semiconductors outside the specific context of photosensitive devices
Deposition of semiconductors outside the specific context of photosensitive devices

Special rules of classification
If the device obtained by the method is of particular interest, then the document is additionally classified in the relevant device groups H01L 31/06, H01L 27/142, or H01L 31/08.
**H01L 31/1828**

{the active layers comprising only A\textsubscript{II}B\textsubscript{VI} compounds, e.g. CdS, ZnS, CdTe}

**Definition statement**

This place covers:
Deposition, etching, patterning, doping of group II-VI compounds as parts of photosensitive devices

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Processes relating to semiconductor devices per se | H01L 21/00 |

**H01L 31/184**

{the active layers comprising only A\textsubscript{III}B\textsubscript{V} compounds, e.g. GaAs, InP}

**Definition statement**

This place covers:
Deposition, etching, patterning, doping of group III-V compounds as parts of photosensitive devices.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Processes relating to semiconductor devices per se | H01L 21/00 |

**H01L 31/186**

{Particular post-treatment for the devices, e.g. annealing, impurity gettering, short-circuit elimination, recrystallisation}

**Definition statement**

This place covers:
Post-treatment of (non-amorphous) photosensitive devices or of materials within photosensitive devices (possibly before final completion of the device).

**References**

**Limiting references**

This place does not cover:

| Post-treatment specific to amorphous semiconductors, wherein the final film is still amorphous after the treatment | H01L 31/208 |
Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Heat treatments of the deposited layers or of the devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystallisation or recrystallisation of non-monocrystalline semiconductor materials per se</td>
</tr>
<tr>
<td>Thermal treatment for modifying the properties of semiconductor bodies per se</td>
</tr>
</tbody>
</table>

H01L 31/1864

{Annealing}

Definition statement

This place covers:

Heat treatments of the deposited layers or of the devices

References

Limiting references

This place does not cover:

Recrystallization | H01L 31/1872

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Thermal treatment for modifying the properties of semiconductor bodies per se | H01L 21/324 |
| Selenization in I-III-VI chalcopyrite semiconductor layer formation | H01L 31/0322 |

Special rules of classification

If the treatment is done during the formation of the semiconductor layers, the annealing is not considered to be a "post treatment" and these processes details are classified in groups dealing with the formation of the semiconductor layers.

H01L 31/1868

{Passivation}

Definition statement

This place covers:

After-treatments for passivation

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Coating deposition | H01L 31/0216 |
**H01L 31/1872**

**{Recrystallisation}**

**Definition statement**

This place covers:

Crystallization processes and recrystallisation processes: the starting layer being in polycrystalline or amorphous state, after the treatment being then in mono- or polycrystalline state, e.g. crystallization of amorphous layers.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Film crystallization as such (not specific to photosensitive devices)</td>
<td>H01L 21/02667</td>
</tr>
<tr>
<td>Particular post-treatment of the devices, wherein the layers after the treatment are still amorphous</td>
<td>H01L 31/208</td>
</tr>
</tbody>
</table>

**H01L 31/1876**

**{Particular processes or apparatus for batch treatment of the devices}**

**Definition statement**

This place covers:

Apparatus and processes in which a plurality of substrates or devices are simultaneously processed.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apparatuses not specific to the fabrication of solar cells or photodetecting devices</td>
<td>H01L 21/67</td>
</tr>
</tbody>
</table>

**H01L 31/188**

**{Apparatus specially adapted for automatic interconnection of solar cells in a module}**

**Definition statement**

This place covers:

Stringer devices, for automatic soldering of interconnecting tabs to solar cells (of bulk type) for series connections
H01L 31/1884
{Manufacture of transparent electrodes, e.g. TCO, ITO}

Definition statement
This place covers:
Methods for manufacturing transparent electrodes.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Electrode material or optical/electrical properties of transparent electrodes</th>
<th>H01L 31/022466</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transparent electrodes for semiconductor light emitting devices LEDs</td>
<td>H01L 33/42</td>
</tr>
<tr>
<td>Transparent electrodes for organic devices</td>
<td>H01L 51/442</td>
</tr>
<tr>
<td>Conductive materials, e.g. oxides</td>
<td>H01B 1/08</td>
</tr>
</tbody>
</table>

H01L 31/20
such devices or parts thereof comprising amorphous semiconductor materials

Definition statement
This place covers:
Apparatuses and methods specific to amorphous semiconductor materials

References
Limiting references
This place does not cover:

| Apparatuses and methods relating to microcrystalline silicon                | H01L 31/1824    |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Crystallization of amorphous layers                                         | H01L 31/1872    |

Special rules of classification
Microcrystalline is not considered amorphous for purposes of classification.

H01L 31/202
{including only elements of Group IV of the Periodic System}

Definition statement
This place covers:
Methods for depositing elements of the fourth group of the Periodic System, e.g. amorphous silicon.
Special rules of classification
For methods aimed at decreasing the Staebler-Wronski effect, classification is additionally made in H01L 31/03767.

H01L 31/206

{Particular processes or apparatus for continuous treatment of the devices, e.g. roll-to roll processes, multi-chamber deposition}

Definition statement
This place covers:
Methods or specific apparatuses for processing a plurality of devices on a substrate, e.g. multi-chamber deposition of p-i-n amorphous silicon solar modules and roll to roll processes.

H01L 31/208

{Particular post-treatment of the devices, e.g. annealing, short-circuit elimination}

Definition statement
This place covers:
Methods to recover short-circuit defects in amorphous silicon solar cell modules.

H01L 33/00

Semiconductor devices with at least one potential-jump barrier or surface barrier specially adapted for light emission; Processes or apparatus specially adapted for the manufacture or treatment thereof or of parts thereof; Details thereof (H01L 51/50 takes precedence; devices consisting of a plurality of semiconductor components formed in or on a common substrate and including semiconductor components with at least one potential-jump barrier or surface barrier, specially adapted for light emission H01L 27/15; semiconductor lasers H01S 5/00)

Definition statement
This place covers:
Light emitting diodes [LEDs] or superluminescent diodes [SLDs], including LEDs or SLDs emitting infra-red [IR] light or ultra-violet [UV] light.

The subgroup H01L 33/48 covers elements in intimate contact with the semiconductor body or integrated with the package.

References

Limiting references
This place does not cover:

| Hybrid assemblies of a plurality of individual LED devices | H01L 25/075 |
| Hybrid assemblies of LED devices with other semiconductor devices | H01L 25/167 |
Devices consisting of a plurality of monolithically integrated LED components or of LED components monolithically integrated with other semiconductor components | H01L 27/15

Organic light emitting diodes [OLEDs] or polymer light emitting diodes [PLEDs] | H01L 51/50

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Compositions of polymers for encapsulating LEDs | C08L |
| Photoluminescent materials per se | C09K 11/00 |
| Light sources using semiconductor devices as light-generating elements, e.g. using light-emitting diodes [LED] or lasers | F21K 9/00 |
| Couplings of planar or plate-like light guides with LEDs | G02B 6/0073 |
| Couplings of light guides with optoelectronic elements | G02B 6/42 |
| Liquid crystal display backlights using LEDs | G02F1/13357 |
| Semiconductor lasers | H01S 5/00 |
| Electroluminescent light sources per se | H05B 33/00 |
| Circuit arrangements for LEDs | H05B 33/0803 |

**Special rules of classification**

In this group, at each hierarchical level, in the absence of an indication to the contrary, classification is made in the first appropriate place.

When classifying in the subgroup H01L 33/18 or H01L 33/40, classification is also made in group H01L 33/26 or one of its subgroups in order to identify the chemical composition of the light emitting region.

**Synonyms and Keywords**

In patent documents, the following abbreviations are often used:

| LED | Light Emitting Diode |
| SLD | Super Luminescent Diode |
| IR | Infra-Red |
| UV | Ultra-Violet |
| LCD | Liquid Crystal Display |
| PCB | Printed Circuit Board |
**H01L 35/00**

Thermoelectric devices comprising a junction of dissimilar materials, i.e. exhibiting Seebeck or Peltier effect with or without other thermoelectric effects or thermomagnetic effects; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof; Details thereof (devices consisting of a plurality of solid state components formed in or on a common substrate **H01L 27/00**; refrigerating machines using electric or magnetic effects **F25B 21/00**; thermometers using thermoelectric or thermomagnetic elements **G01K 7/00**; obtaining energy from radioactive sources **G21H**)

**References**

**Limiting references**

This place does not cover:

| Thermophotovoltaic systems | H02S 10/30 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Details of semiconductor or other solid state devices Cooling arrangements using the Peltier effect | H01L 23/38 |
| Devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate | H01L 27/16 |
| Soldering or welding | B23K |
| Selenium; Tellurium; Compounds thereof | C01B 19/00 |
| Oxides of metals | C01G |
| Alloys | C22C |
| Exhaust or silencing apparatus combined or associated with devices profiting by exhaust energy | F01N 5/00 |
| Refrigeration - Machines, plant, or systems, using electric or magnetic effects | F25B 21/00 |
| Heat-Exchange apparatus, not provided for in another subclass, in which the heat-exchange media do not come into direct contact | F28D |
| Details of heat-exchange and heat-transfer apparatus | F28F |
| Radiation pyrometer | G01J 5/12 |
| Measuring temperature based on the use of electric or magnetic elements directly sensitive to heat | G01K 7/00 |
| Arrangements for obtaining electrical energy from radioactive sources | G21H 1/00 |
| Generators or motors not provided for elsewhere | H02N 11/00 |

**Special rules of classification**

Devices or aspects which are not provided for in lower groups but still contain technical details of thermoelectrics are classified in the head group.
Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEG</td>
<td>thermoelectric generator</td>
</tr>
<tr>
<td>TEC</td>
<td>thermoelectric cooler</td>
</tr>
<tr>
<td>TEM</td>
<td>thermoelectric module</td>
</tr>
<tr>
<td>ZT</td>
<td>dimensionless figure of merit</td>
</tr>
</tbody>
</table>

H01L 35/04

Structural details of the junction; Connections of leads

Definition statement

This place covers:
Structural details of the junction between the thermoelectric legs which are not covered by the subgroups H01L 35/06 or H01L 35/08.

References

Limiting references

This place does not cover:
Thermo-electric devices operating with Peltier or Seebeck effect only characterised by the structure or configuration of the cell or thermo-couple forming the device, e.g. electrical details

H01L 35/06

detachable, e.g. using a spring

Definition statement

This place covers:
Detachable connections between the thermoelectric material and the junction, for example a spring connection for compensating for thermal expansion or for avoiding use of a solder connection.

H01L 35/08

non-detachable, e.g. cemented, sintered, soldered {, e.g. thin films}

Definition statement

This place covers:
Non-detachable junctions such as soldered or sintered connections to the thermoelectric material.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:
Soldering or welding

B23K
**H01L 35/10**

Connections of leads

*Definition statement*

This place covers:

Connection of terminal leads only, namely the external electrodes for supplying or receiving power for connecting to the thermoelectric device as a whole and details of their arrangement or structure.

**H01L 35/12**

Selection of the material for the legs of the junction

*Definition statement*

This place covers:

Materials specially adapted for the legs of the junction of thermo-electric devices.

**H01L 35/16**

comprising tellurium or selenium or sulfur

*Definition statement*

This place covers:

Thermoelectric compositions comprising tellurium such as bismuth telluride or alloys thereof, including nanomaterials.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Tellurium compounds per se | C01B 19/00 |

**H01L 35/18**

comprising arsenic or antimony or bismuth (*H01L 35/16* takes precedence), {e.g. $\text{A}_{\text{III}}\text{B}_\text{V}$ compounds}

*Definition statement*

This place covers:

Thermoelectric compositions comprising antimony, for example skutterudites, cobalt antimonide, or compositions comprising bismuth.

**References**

*Limiting references*

This place does not cover:

| Bismuth telluride | H01L 35/16 |
**H01L 35/20**

comprising metals only (H01L 35/16, H01L 35/18 take precedence)

**Definition statement**

This place covers:
Thermoelectric compositions comprising metals only, such as alloys, for example constantan.

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Composition</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Selenium, Tellurium</td>
<td>H01L 35/16</td>
</tr>
<tr>
<td>Arsenic, Antimony, Bismuth</td>
<td>H01L 35/18</td>
</tr>
</tbody>
</table>

**H01L 35/22**

comprising compounds containing boron, carbon, oxygen or nitrogen {or germanium or silicon, e.g. superconductors}

**Definition statement**

This place covers:
Thermoelectric compositions comprising compounds containing boron, carbon, oxygen (high temperature oxide thermoelectric materials) or nitrogen, germanium or silicon, for example silicon germanide.

**References**

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Composition</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Organic compositions</td>
<td>H01L 35/24</td>
</tr>
</tbody>
</table>

**H01L 35/24**

using organic compositions

**Definition statement**

This place covers:
Organic thermoelectric compositions.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Composition</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Organic semiconductors</td>
<td>H01L 51/00</td>
</tr>
</tbody>
</table>
**H01L 35/26**

using compositions changing continuously or discontinuously inside the material

**Definition statement**

*This place covers:*

Thermoelectric compositions changing continuously or discontinuously inside the material, for example superlattices of different thermoelectric materials, or composite or nanocomposite materials with a matrix containing particles of thermoelectric material, for example to reduce thermal conductivity and increase figure of merit.

**H01L 35/30**

characterised by the heat-exchanging means at the junction

**Definition statement**

*This place covers:*

Details of the thermal properties of the device or module, for example the heat transfer arrangement, or details of the interface to the heat source, for example coupling to a source of exhaust heat from an internal combustion engine or to a solar heat source or a source of refrigeration.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Exhaust or silencing apparatus combined or associated with devices profiting by exhaust energy | F01N 5/00 |
| Refrigeration - Machines, plant, or systems, using electric or magnetic effects | F25B 21/00 |
| Heat-exchange apparatus, not provided for in another subclass, in which the heat-exchange media do not come into direct contact | F28D |
| Details of heat-exchange and heat-transfer apparatus, of general application | F28F |

**H01L 35/32**

characterised by the structure or configuration of the cell or thermo-couple forming the device {including details about, e.g., housing, insulation, geometry, module}

**Definition statement**

*This place covers:*

Details of the design of the thermocouple or module; details about the housing, such as the materials used for the substrate or the packaging; insulation - details of the thermal design of the module itself (heat exchanging means H01L 35/30); geometry - details of the layout or symmetry of the device or module - details of how to arrange multiple thermocouples into a module, such as the electrical arrangement in series or variations thereof.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Details of semiconductor or other solid state devices - Cooling arrangements using the Peltier effect | H01L 23/38 |
| Devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate | H01L 27/16 |
| Generators or motors not provided for elsewhere | H02N 11/00 |

H01L 35/325

{Cascades of thermo-couples}

Definition statement

This place covers:

Cascades of thermocouples, for example multi-stage devices in which each stage provides a cooling effect within a certain temperature regime.

H01L 35/34

Processes or apparatus peculiar to the manufacture or treatment of these devices or of parts thereof (not peculiar thereto H01L 21/00)

Definition statement

This place covers:


References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Manufacture of semiconductor devices per se | H01L 21/00 |
**H01L 37/00**

Thermoelectric devices without a junction of dissimilar materials; Thermomagnetic devices, e.g. using Nernst-Ettinghausen effect; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof (devices consisting of a plurality of solid state components formed in or on a common substrate H01L 27/00; radiation pyrometers using pyroelectric detectors G01J 5/34) thermometers using thermo-electric or thermomagnetic elements G01K 7/00; selection of materials for magnetography, e.g. for Curie-point writing G03G 5/00)

**Definition statement**

This place covers:

Devices directly converting thermal energy to electrical or magnetic quantities or vice versa using thermoelectric or thermomagnetic effects of solid state bulk materials, the related materials and fabrication of such devices.

Particularly important are devices based on

- Pyroelectric effect (change of dielectric polarisation under thermal influence) and its inverse effect, the electrocaloric effect (temperature change under an applied electrical field);
- Pyromagnetic effect (change of magnetisation under thermal influence) and its inverse effect, the magnetocaloric effect (temperature change under an applied magnetic field);
- Nernst-Ettingshausen effect (generation of an electrical field orthogonal to a magnetic field which is perpendicular to a thermal gradient) and its inverse effect (generation of a transversal thermal gradient by a magnetic field orthogonal to an electrical current);
- Bolometric effect (change of electrical resistance under thermal influence).

**References**

**Limiting references**

This place does not cover:

| Heating or cooling arrangements, e.g. heat pumps, using electric or magnetic effects | F25B 21/00 |
| Thermistors | H01C 7/008, H01C 7/02, H01C 7/04 |
| Devices using ballistic electron transport across a (vacuum) gap, e.g. thermotunnel diodes | H01J 45/00 |
| Devices based on simple Joule heating (heat generated by current flow through a resistive material) | H05B 3/00 |

**Application-oriented references**

Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

| Devices consisting of plural semiconductor or other solid state components on a common substrate including thermoelectric or thermomagnetic components, e.g. integrated arrays | H01L 27/16 |
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Classifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor infrared radiation sensitive devices - Photoresistors - Phototransistors</td>
<td>H01L 31/09, H01L 31/101</td>
</tr>
<tr>
<td>Thermoelectric devices with junctions of different materials, e.g. based on Peltier or Seebeck effects</td>
<td>H01L 35/00</td>
</tr>
<tr>
<td>Measuring thermal radiation; Pyrometers</td>
<td>G01J 5/20</td>
</tr>
<tr>
<td>Measuring temperature based on thermoelectric or thermomagnetic elements; Thermometers</td>
<td>G01K 7/00</td>
</tr>
<tr>
<td>Magnetography and selection of materials thereof, e.g. Curie-point writing</td>
<td>G03G 5/00, G03G 5/16, G03G 19/005</td>
</tr>
</tbody>
</table>

**Special rules of classification**

In this group, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

**Synonyms and Keywords**

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEG</td>
<td>Thermoelectric generator</td>
</tr>
<tr>
<td>TMG</td>
<td>Thermomagnetic generator</td>
</tr>
</tbody>
</table>

**H01L 37/02**

using thermal change of dielectric constant, e.g. working above and below Curie point {, e.g. pyroelectric devices}

**Definition statement**

This place covers:

Pyroelectric or electrocaloric devices, mainly TEGs.

**H01L 37/025**

{Selection of materials}

**Definition statement**

This place covers:

Pyroelectric or electrocaloric materials.

**H01L 37/04**

using thermal change of magnetic permeability, e.g. working above and below the Curie point {, e.g. pyromagnetic devices}

**Definition statement**

This place covers:

Pyromagnetic or magnetocaloric devices, mainly TMGs.
H01L 39/00

Devices using superconductivity; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof (devices consisting of a plurality of solid state components formed in or on a common substrate  

H01L 27/00; {light detection G01J, G02F 2/00; application to memories G11C 11/44, G11C 15/00, G11C 19/32} ; superconducting conductors cables or transmission lines H01B 12/00; {microwaves H01P 7/00, H01P 11/00} ; superconductive coils or windings H01F; amplifiers using superconductivity H03F 19/00; {impulse generators and logic circuits H03K 3/38, H03K 17/92, H03K 19/195; lasers H01S 3/00, H01S 5/00})

Definition statement

This place covers:

- Devices based on materials having essentially zero electrical resistance below a characteristic temperature Tc, current density Jc, and magnetic field Hc, e.g. Josephson devices, switches;
- Intermediate products used in specially adapted arrangements, e.g. tape or wire like parts for cables or coils, basic conductor elements like films etc., and fabrication thereof until superconductive material is obtained;
- Details and fabrication thereof.

Relationships with other classification places

Superconductive (ceramic, crystalline) materials in devices are classified in this group.

Bulk permanent magnets solely characterised by their materials are classified both in this group and in H01F 6/00.

References

Limiting references

This place does not cover:

| Thermoelectric junction, e.g. Peltier or Seebeck devices comprising superconductors | H01L 35/225 |
| Superconductive materials characterised by the ceramic-forming technique or the ceramic composition in general, and precursor materials thereof | C04B 35/00 |
| Superconductive (single) crystals and fabrication thereof including epitaxy | C30B |
| Superconductive conductors such as cables or transmission lines composed of superconductive filaments or tapes covered by this group- Manufacturing thereof | H01B 12/00, H01B 13/00 |
| Superconductive inductors such as magnets or coils composed of superconductive filaments or tapes covered by this group- Coils- Transformers- Manufacturing- of coils | H01F 6/00, H01F 6/06, H01F 36/00, H01F 41/00, H01F 41/048 |
| Waveguide type devices, e.g. for microwaves- Filters- Transmission lines- Resonators- Manufacturing | H01P, H01P 1/00, H01P 3/00, H01P 7/00, H01P 11/00 |
| Antennas | H01Q 1/364 |
| Current leads | H01R 4/68 |
| Lasers | H01S 3/1683 |
**Application-oriented references**

Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

| Devices consisting of plural semiconductor or other solid state components on a common substrate including superconducting components, e.g. integrated circuit arrangements with Josephson junctions | H01L 27/18 |
| Superconductive magnetometers, e.g. SQUIDs- using magnetic resonance | G01R 33/035, G01R 33/3815 |
| High power arc switches | H01H 33/004 |
| Superconductive magnetic energy storage systems | H02J 15/00 |
| Dynamo-electric machines, e.g. electric motors or generators, with superconductive windings | H02K 55/00 |
| Magnetic holding or levitation devices using superconductivity- for trains | H02N 15/04, B60L 13/00 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Manufacture or treatment of semiconductor or solid state devices in general | H01L 21/00 |
| Superconductive parts in semiconductor or other solid state devices, e.g. integrated circuit electrodes or interconnects; Fabrication thereof | H01L 21/32058, H01L 21/76891, H01L 23/49888, H01L 23/53285, H01L 29/437 |
| Magnetic separation - of superconductive material- using superconducting coils | B03C 1/00, B03C 1/021, B03C 1/0337, B03C 1/0355 |
| Forming coating layers comprising copper oxides - by physical vapour deposition, e.g. sputtering- by chemical vapour deposition | C23C 14/087, C23C 16/408 |
| Cryostats | F17C 13/007 |
| Measuring level of liquids or fluent solid materials; Level sensors | G01F 23/246 |
| Measuring radiation - Photometers, e.g. single photon detectors- Pyrometers | G01J, G01J 1/42, G01J 5/20 |
| Measuring temperature using superconductive elements; Thermometers | G01K 7/006 |
| Measuring superconductive properties | G01R 33/1238 |
| Measuring X-ray or corpuscular radiation; particle detectors | G01T 1/1606 |
| Quantum computers | G06N 10/00 |
| Magnetic recording - Heads - Positioning thereof | G11B 5/00, G11B 5/3126, G11B 5/3159, G11B 5/583 |
| Digital memories - content addressed- using shift registers | G11C 11/44, G11C 15/06, G11C 19/32 |
| Protective circuits for superconducting apparatus such as coils, lines, machines | H02H 7/001 |
| Current limiting circuits using superconducting devices, e.g. FCL circuits | H02H 9/023 |
### Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abrikosov vortex</td>
<td>Vortex of supercurrent in a superconductor circulating around the normal conducting core of the vortex</td>
</tr>
<tr>
<td>Cryotron</td>
<td>Device that uses externally induced switching of a current carrying element between superconductive and normal states by electric, magnetic or heating means, e.g. using a gate conductor, coil, resistive heater</td>
</tr>
<tr>
<td>Tc</td>
<td>Critical temperature</td>
</tr>
<tr>
<td>High Tc</td>
<td>Tc above 30 K; more frequently Tc above 90 K, may be cooled by liquid nitrogen</td>
</tr>
</tbody>
</table>

### Synonyms and Keywords

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>B(P)SCCO</td>
<td>Bismuth (lead) strontium calcium copper oxide; Bi(Pb)SrCaCuO</td>
</tr>
<tr>
<td>Bi–22(n-1)nBi–2223</td>
<td>Bi2Sr2Can-1CunO4+2n+x series (n=1, 2, 3) Bi2Sr2Ca2Cu3O10+x</td>
</tr>
<tr>
<td>Coated conductor</td>
<td>Coated conductor; a superconducting film on a tape like substrate</td>
</tr>
<tr>
<td>FCL</td>
<td>Fault current limiter</td>
</tr>
<tr>
<td>HBCCO</td>
<td>Mercury barium calcium copper oxide</td>
</tr>
<tr>
<td>Hc</td>
<td>Critical magnetic field</td>
</tr>
<tr>
<td>HTC</td>
<td>High Tc</td>
</tr>
<tr>
<td>HTSHTSC</td>
<td>High Tc superconductor</td>
</tr>
<tr>
<td>IBAD</td>
<td>Ion beam assisted deposition</td>
</tr>
<tr>
<td>Ic</td>
<td>Critical current</td>
</tr>
<tr>
<td>Jc</td>
<td>Critical current density</td>
</tr>
<tr>
<td>LHe</td>
<td>Liquid helium</td>
</tr>
<tr>
<td>LN LN2</td>
<td>Liquid nitrogen</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>--------------</td>
<td>---------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Low Tc</td>
<td>Not high Tc; more frequently Tc of only a few K, needs cooling by liquid helium</td>
</tr>
<tr>
<td>LTC</td>
<td>Low Tc</td>
</tr>
<tr>
<td>LTS</td>
<td>Low Tc superconductor</td>
</tr>
<tr>
<td>PCS</td>
<td>Persistent current switch</td>
</tr>
<tr>
<td>(O)PIT</td>
<td>(Oxide) powder-in-tube; method for forming superconductive filaments</td>
</tr>
<tr>
<td>RABITS</td>
<td>Rolling assisted biaxially textured substrate</td>
</tr>
<tr>
<td>RE</td>
<td>Rare earth</td>
</tr>
<tr>
<td>RE–123</td>
<td>REBa2Cu3O7-x</td>
</tr>
<tr>
<td>RBC RBOCBO</td>
<td>Rare earth barium copper oxide</td>
</tr>
<tr>
<td>RSFQ</td>
<td>Rapid single flux quantum</td>
</tr>
<tr>
<td>SIS</td>
<td>Superconductor-insulator-superconductor (stacked layers in junctions)</td>
</tr>
<tr>
<td>SNS</td>
<td>Superconductor-normal conductor-superconductor (stacked layers in junctions)</td>
</tr>
<tr>
<td>SQUID</td>
<td>Superconducting quantum interference device</td>
</tr>
<tr>
<td>TES</td>
<td>Transition edge sensor</td>
</tr>
<tr>
<td>TBCCO</td>
<td>Thallium barium calcium copper oxide</td>
</tr>
<tr>
<td>YBC YBCO BYCBYCO</td>
<td>Yttrium barium copper oxide</td>
</tr>
<tr>
<td>Y–123</td>
<td>YBa2Cu3O7-x</td>
</tr>
</tbody>
</table>

**H01L 39/02**

**Details**

**Definition statement**

This place covers:

Direct connections, e.g. splices, between superconducting filaments or wires and manufacture thereof

**H01L 39/10**

characterised by the means for switching {between superconductive and normal states}

**Definition statement**

This place covers:

Devices having special means for inducing or modifying superconductive to normal state transition, e.g. electrical, optical, thermal

**References**

**Limiting references**

This place does not cover:

Devices without or with simple electromagnetic or heating means for switching, e.g. coils, heater wires
**H01L 39/12**

**characterised by the material**

**Definition statement**

*This place covers:*

Only superconductive materials of the devices.

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Material</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper oxide compounds</td>
<td>C01G 3/006</td>
</tr>
<tr>
<td>Superconductive ceramic materials and precursor materials based on</td>
<td>C04B 35/45</td>
</tr>
<tr>
<td>copper oxides</td>
<td></td>
</tr>
<tr>
<td>Ceramics based on magnesium boride</td>
<td>C04B 35/58057</td>
</tr>
<tr>
<td>Crystals based on rare earth copper oxides</td>
<td>C30B 29/225</td>
</tr>
</tbody>
</table>

**H01L 39/128**

{Multi-layered structures, e.g. super lattices}

**Definition statement**

*This place covers:*

Superconductive materials consisting of copper oxide superconductors stacked in alternating fashion with other materials, wherein the latter may be different copper oxide superconductors.

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Material</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Materials formed by stacking atomic monolayers of copper, oxygen, and</td>
<td>H01L 39/126</td>
</tr>
<tr>
<td>other elements which in combination form a single copper oxide</td>
<td></td>
</tr>
<tr>
<td>superconductor</td>
<td></td>
</tr>
</tbody>
</table>

**H01L 39/16**

Devices switchable between superconductive and normal states {, e.g. switches, current limiters (circuits for current limitation using superconductor elements H02H 9/023)}

**Definition statement**

*This place covers:*

Resistive FCL devices, including such with non-inductive windings.
References

Limiting references

This place does not cover:

FCL devices based on inductive windings, e.g. rings, coils, transformers [H01F 6/06, H01F 36/00]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Current limiting circuits using superconducting devices, e.g. FCL circuits [H02H 9/023]

H01L 39/20

Power cryotrons

Definition statement

This place covers:

FCL devices as described under H01L 39/16 with further external, e.g. thermal, magnetic, electric, switching means;

Persistent current switch (PCS) devices for high power applications.

H01L 39/2403

{Processes peculiar to the manufacture or treatment of composite superconductor filaments (comprising copper oxide H01L 39/2419)}

Definition statement

This place covers:

Manufacturing composites of either plural filaments of different superconductive materials covered by H01L 39/2406 - H01L 39/2419 or filaments whose superconductive material is irrelevant embedded in other, mostly metallic materials, e.g. aspects such as claddings for shunting, insulation or mechanical reinforcement.

H01L 39/2451

{Precursor deposition followed by after-treatment, e.g. oxidation}

Definition statement

This place covers:

Methods for treating precursor layers to establish superconductive state, e.g. heating or oxygenation treatments of layers formed by methods covered by groups H01L 39/2422 - H01L 39/2448.

H01L 39/2477

{Processes including the use of precursors}

Definition statement

This place covers:

Methods for preparing, treating or selecting precursors such as powders used in the (O)PIT method.
H01L 39/248  
{Processes peculiar to the manufacture or treatment of filaments or composite wires}

Definition statement

This place covers:
Fabrication of (multi-)filamentary wires or tapes by e.g. (O)PIT or CC methods.

Special rules of classification

Classification of relevant details concerning substrate, buffer, or superconductive layer deposition is mandatory in groups H01L 39/2422 - H01L 39/2461, by allocating at least Indexing Code symbols thereof.

H01L 41/00

Piezo-electric devices in general; Electrostrictive devices in general; Magnetostrictive devices in general; Processes or apparatus specially adapted for the manufacture or treatment thereof or of parts thereof; Details thereof (devices consisting of a plurality of solid-state components formed in or on a common substrate H01L 27/00)

Definition statement

This place covers:
• Devices which exhibit or change a dielectric polarisation of a solid state body when subjected to mechanical stress (piezoelectric effect) or which exhibit a mechanical deformation when subjecting such body to an electrical field (inverse piezoelectric effect; electrostrictive effect);
• Devices which exhibit or change an electrical field across an elastic dielectric solid state body by mechanical deformation or which exhibit a mechanical deformation when subjecting such body to an electrical field (quasi-electrostrictive effect), e.g. dielectric electroactive polymer devices;Devices of the above types are collectively termed PE devices.
• Devices which exhibit or change a magnetisation of a solid state body when subjected to mechanical stress (piezomagnetic effect; inverse magnetostrictive effect; Villari effect) or which exhibit a mechanical deformation when subjecting such body to a magnetic field (magnetostrictive effect; magnetic shape memory effect);Such devices are collectively termed MS devices.

Relationships with other classification places

This main group covers PE or MS devices which are pertinent to several technical fields like primary motion producing or electricity generating elements (actuators, sensors, transducers) usable in a multitude of application areas, or which are not limited to a particular application, i.e. PE or MS devices in general. Aspects such as their function, structure, details, materials used, fabrication etc. are classified here.

The group H01L 41/00 itself covers devices with cooperating PE and MS parts or combined PE and MS effects, e.g. magneto-electric converters. Relevant details of the respective PE or MS parts should be classified using Indexing Code symbols under H01L 41/08 and H01L 41/12.

Electrical machines based on PE or MS effects, i.e. motors or generators using PE or MS devices as primary motion producing or electricity generating parts, are covered by H02N 2/00. Aspects such as the mechanical construction built around said PE or MS devices, driving or control circuits and methods are classified there, i.e. the PE or MS devices covered by H01L 41/00 are seen as black boxes and could in principle be replaced by any device of equal electromechanical conversion functionality.
If no relevant details of the PE or MS elements themselves are given, classification is done only in H02N 2/00. If particular details of the PE or MS elements are concerned, classification in H01L 41/00 is required.

Piezoresistivity (change of electrical resistance of a (semi)conducting material under mechanical stress) is not a piezoelectric effect. Piezoresistive devices are thus excluded from this group. Frequently they concern force or pressure sensors covered by G01L 1/18 or G01L 9/06.

References

**Limiting references**

This place does not cover:

<table>
<thead>
<tr>
<th>Devices consisting of plural semiconductor or other solid state components on a common substrate, e.g. integrated circuit arrangements, including PE components</th>
<th>H01L 27/20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor devices wherein carrier transport therein is modulated through stress generated by PE parts, e.g. strained channel FET</td>
<td>H01L 29/68</td>
</tr>
<tr>
<td>Semiconductor devices controlled by applied mechanical force or pressure, e.g. piezoresistive devices</td>
<td>H01L 29/84</td>
</tr>
<tr>
<td>Surgical cutting instruments</td>
<td>A61B 17/320068</td>
</tr>
<tr>
<td>Dental cleaning, e.g. tooth brushes</td>
<td>A61C 17/20</td>
</tr>
<tr>
<td>Inhalers</td>
<td>A61M 15/0085</td>
</tr>
<tr>
<td>Atomisers for liquids; Nebulisers</td>
<td>B05B 17/0607</td>
</tr>
<tr>
<td>PE mechanical vibration generators, e.g. (ultra)sonic probes - in medical diagnosis - for analysing material</td>
<td>B06B 1/06, A61B 8/00, G01N 29/2437</td>
</tr>
<tr>
<td>Ultrasonic cleaning</td>
<td>B08B 3/12</td>
</tr>
<tr>
<td>Hair clippers; Shavers</td>
<td>B26B 19/28</td>
</tr>
<tr>
<td>Ink jet printers - Control methods or devices - Print head structures - Production thereof</td>
<td>B41J 2/04581, B41J 2/14201, B41J 2/1607</td>
</tr>
<tr>
<td>Typewriters</td>
<td>B41J 2/295</td>
</tr>
<tr>
<td>PE generators - in tyre sensors - in firing or trigger mechanisms of weapons - in photographic flash ignition</td>
<td>B60C 23/0411, F41A 19/62, G03B 15/0463</td>
</tr>
<tr>
<td>Fuel injection in combustion engines - Control circuits or methods for injectors - Injectors - Injection valves</td>
<td>F02D 41/2096, F02M 51/0603, F02M 59/468, F02M 63/0026</td>
</tr>
<tr>
<td>Fuel ignition - in combustion engines - in lighters</td>
<td>F02P 3/12, F23Q 2/287, F23Q 3/002</td>
</tr>
<tr>
<td>Devices comprising (ion) conductive EAPs (ionic EAPs; IPMCs) (based on electrochemical effects in these EAPs)</td>
<td>F03G 7/005</td>
</tr>
<tr>
<td>Pumps - Diaphragma type micropumps - Tube type - Oscillatory type, e.g. fans</td>
<td>F04B 17/003, F04B 43/046, F04B 43/095, F04D 33/00</td>
</tr>
<tr>
<td>Brakes</td>
<td>F16D 2121/28, F16D 2129/12</td>
</tr>
<tr>
<td>Suppression of vibrations, i.e. active cancellation</td>
<td>F16F 15/005</td>
</tr>
<tr>
<td>Topic</td>
<td>CPC Code</td>
</tr>
<tr>
<td>----------------------------------------------------------------------</td>
<td>---------------------------------------------------</td>
</tr>
<tr>
<td>Valves</td>
<td>F16K 31/004</td>
</tr>
<tr>
<td>PE arrangements for measuring length, width or thickness</td>
<td>G01B 7/063</td>
</tr>
<tr>
<td>Gyrosopes</td>
<td>G01C 19/56</td>
</tr>
<tr>
<td>Sensors for measuring level of liquids or fluent solid materials</td>
<td>G01F 23/296</td>
</tr>
<tr>
<td>PE strain gauges</td>
<td>G01L 1/16</td>
</tr>
<tr>
<td>PE pressure gauges</td>
<td>G01L 9/0022, G01L 9/008, G01L 9/08, G01L 23/10, G01L 23/222</td>
</tr>
<tr>
<td>PE fluid microsensors, e.g. quartz crystal microbalance, SAW devices</td>
<td>G01N 29/022</td>
</tr>
<tr>
<td>PE accelerometers</td>
<td>G01P 15/09</td>
</tr>
<tr>
<td>PE probes for scanning probe microscopy (SPM)</td>
<td>G01Q 10/045, G01Q 20/04</td>
</tr>
<tr>
<td>Adjustable mountings for optical elements, e.g. PE motorised lenses, objectives</td>
<td>G02B 7/02, G02B 7/10</td>
</tr>
<tr>
<td>PE MEMS optical mirror devices</td>
<td>G02B 26/0858</td>
</tr>
<tr>
<td>PE sound producing horns, buzzers</td>
<td>G10K 9/122</td>
</tr>
<tr>
<td>MS relays</td>
<td>H01H 55/00</td>
</tr>
<tr>
<td>PE relays</td>
<td>H01H 57/00</td>
</tr>
<tr>
<td>PE or MS release mechanisms in circuit breaker switches</td>
<td>H01H 71/127</td>
</tr>
<tr>
<td>Electrostatic devices not based on deformation of a solid state body by electrical fields or mechanical forces (dielectric EAPs), e.g. based on relative motion of spaced conductors</td>
<td>H02N 1/00</td>
</tr>
<tr>
<td>Impedance networks, frequency selective elements or circuits, e.g. resonators, filters, delay lines using BAW or SAW- Manufacturing</td>
<td>H03H 9/00, H03H 3/00</td>
</tr>
<tr>
<td>PE touch switches; Keyboards</td>
<td>H03K 17/964</td>
</tr>
<tr>
<td>MS acoustic transducers, e.g. microphones, speakers</td>
<td>H04R 15/00</td>
</tr>
<tr>
<td>PE acoustic transducers, e.g. microphones, speakers</td>
<td>H04R 17/00</td>
</tr>
</tbody>
</table>

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacture or treatment of semiconductor or solid state devices in general</td>
<td>H01L 21/00</td>
</tr>
<tr>
<td>MEMS devices with electromechanical transducers</td>
<td>B81B 3/0021</td>
</tr>
<tr>
<td>Forming coating layers of metal oxides - Alkali, alkaline earth or lead based perovskites - by physical vapour deposition, e.g. sputtering - by chemical vapour deposition- by solution deposition, e.g. sol-gel</td>
<td>C23C 14/088, C23C 16/409, C23C 18/1216</td>
</tr>
<tr>
<td>Electrochemical actuators</td>
<td>F03G 7/005</td>
</tr>
<tr>
<td>Thermal actuators</td>
<td>F03G 7/06</td>
</tr>
<tr>
<td>Weighing</td>
<td>G01G 3/13</td>
</tr>
<tr>
<td>Measuring mechanical vibrations</td>
<td>G01H 11/08</td>
</tr>
<tr>
<td>Analysing fluids by acoustic waves</td>
<td>G01N 29/036</td>
</tr>
<tr>
<td>Measuring PE properties</td>
<td>G01R 29/22</td>
</tr>
</tbody>
</table>
Measuring time - Clocks or watches- Timing standards G04C 3/12, G04F 5/06
Structure or manufacture of flux-sensitive heads using magneto-resistive devices G11B 5/39
Fine positioning of magnetic recording heads - on discs- on tapes G11B 5/5552, G11B 5/592
Digital memories, e.g. FRAMs G11C 11/22
Electromagnetic actuators, e.g. solenoids H01F 7/06
Stack capacitors H01G 4/30
Adjustable capacitors using variation of electrode distance H01G 5/16
Ferroelectric capacitors- for integrated circuit arrangements H01G 7/06, H01L 28/55
Electrostatic actuators H02N 1/002
PE or MS motors or generators H02N 2/00
Actuators not provided for elsewhere H02N 11/006
Frequency generators H03B 5/32

Special rules of classification
In this group, in the absence of an indication to the contrary, an invention is classified in the last appropriate place. Additional information concerning devices, materials or manufacturing methods is indicated by Indexing Code symbols, e.g. in case the invention concerns a device Indexing Code symbols for details or manufacturing should be allocated.

Glossary of terms
In this place, the following terms or expressions are used with the meaning indicated:

| Stacked or multilayer(ed) structure | PE parts, e.g. PE layers, and electrodes alternating in one, i.e. stacking direction |

Synonyms and Keywords
In patent documents, the following abbreviations are often used:

| BAW | Bulk acoustic wave |
| DEA | Dielectric elastomeric actuator |
| EAP | Electroactive polymer |
| EPAM | Electroactive polymer artificial muscle |
| MEMS | Microelectromechanical system |
| MS | Magnetostrictive |
| MSM | Magnetic shape memory (effect) |
| PE | Piezoelectric or electrostrictive |
| PEG | PE generator |
| PMN | Lead magnesium niobate |
| PT | Lead titanate |
| PZ | Piezoelectric; Lead zirconate |
| PZN | Lead zinc niobate |
PZT Piezoelectric transducer; Lead zirconate titanate
SAW Surface acoustic wave

H01L 41/04
of piezoelectric or electrostrictive devices

Definition statement
This place covers:
Special structures of or auxiliary parts associated with the PE device, e.g. of mechanical, electrical or thermal nature, such as circuit, sensing or cooling means.

H01L 41/06
of magnetostrictive devices

Definition statement
This place covers:
Special structures of or auxiliary parts associated with the MS device, e.g. of mechanical, electrical or thermal nature, such as mounting, sensing or cooling means.

H01L 41/16
Selection of materials

Definition statement
This place covers:
Only active materials comprising combined PE and MS constituents, e.g. magneto-electric composites, or exhibiting PE and MS effects, e.g. multi-ferroic materials.

H01L 41/18
for piezoelectric or electrostrictive devices {, e.g. bulk piezoelectric crystals}

Definition statement
This place covers:
Only PE materials.

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Ceramic materials and precursor materials - based on perovskite barium titanates - based on lead zirconate titanates - based on niobates, tantalates | C04B 35/4682, C04B 35/491, C04B 35/495 |
| Crystals of complex oxides - Niobates; Tantalates; Titanates | C30B 29/22, C30B 29/30, C30B 29/32 |
H01L 41/183
{Composite materials, e.g. having 1-3 or 2-2 type connectivity}

Definition statement

This place covers:
Only materials of multi-phase structure, not all phases needing to be PE themselves, which together form the PE material, e.g. ceramic rods, fibres or particles in a polymer matrix.

Further information:

H01L 41/20
for magnetostrictive devices

Definition statement

This place covers:
Only MS or MSM materials.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Magnetic shape memory alloys

H01L 41/22
Processes or apparatus specially adapted for the assembly, manufacture or treatment of piezo-electric or electrostrictive devices or of parts thereof

Definition statement

This place covers:
Processes or apparatus for manufacturing a material, product or device which exhibits or changes an electrostatic polarisation when subjected to mechanical stress or which exhibits a mechanical deformation, e.g. tending to produce a deflection, when subjected to electric stress;

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Processes or apparatus specially adapted for manufacture or treatment of semiconductor or solid state devices or of parts thereof in general
H01L 41/23
Forming enclosures or casings

Definition statement

This place covers:
Processes or apparatus for forming enclosures or casings with encapsulants as illustrated in the figures.
H01L 41/27

Manufacturing multilayered piezo-electric or electrostrictive devices or parts thereof, e.g. by stacking piezo-electric bodies and electrodes

Definition statement

This place covers:
Processes or apparatus for manufacturing multilayered piezo-electric or electrostrictive [PE] parts of the type illustrated.

H01L 41/29

Forming electrodes, leads or terminal arrangements

Definition statement

This place covers:
Generic processes, or apparatus, for forming electrodes, leads or terminal arrangements for piezo-electric or electrostrictive [PE] devices or parts thereof.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Processes or apparatus adapted for the manufacture or treatment of semiconductor or solid state devices or of parts thereof</th>
<th>H01L 21/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apparatus or processes specially adapted for manufacturing conductors or cables</td>
<td>H01B 13/00</td>
</tr>
<tr>
<td>Fixed capacitors; Processes of their manufacture</td>
<td>H01G 4/00</td>
</tr>
<tr>
<td>Processes or means, e.g. batteries, for the direct conversion of chemical into electrical energy, Constructional details or processes of manufacture of the non-active parts, Current conducting connections for cells</td>
<td>H01M 2/00</td>
</tr>
<tr>
<td>Processes or means, e.g. batteries, for the direct conversion of chemical into electrical energy, electrodes</td>
<td>H01M 4/00</td>
</tr>
<tr>
<td>Electrically-conductive connections: Structural associations of a plurality of mutually-insulated electrical connecting elements; Coupling devices; Current collectors</td>
<td>H01R</td>
</tr>
</tbody>
</table>
**H01L 41/293**

Connection electrodes of multilayered piezo-electric or electrostrictive parts

**Definition statement**

*This place covers:*

Processes or apparatus for manufacturing connection electrodes of multilayered piezo-electric or electrostrictive [PE] parts, including lead-in or terminal arrangements of the type illustrated.

**Special rules of classification**

Arrangements of an integral individual layer electrode in combination with connection electrode are classified in both H01L 41/293 and H01L 41/297.
**H01L 41/297**

**Individual layer electrodes of multilayered piezo-electric or electrostrictive parts**

**Definition statement**

*This place covers:*

Processes or apparatus for manufacturing individual layer electrodes of multilayered piezo-electric or electrostrictive [PE] of the type illustrated.

**Special rules of classification**

Arrangements of an integral individual layer electrode in combination with connection electrode are classified in both H01L 41/293 and H01L 41/297.

**H01L 41/31**

**Applying piezo-electric or electrostrictive parts or bodies onto an electrical element or another base**

**Definition statement**

*This place covers:*

Processes or apparatus for applying piezo-electric or electrostrictive [PE] parts or bodies onto an electrical element or another base of the types illustrated are included in this group.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference Description</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in or on a common substrate or of specific parts thereof; Manufacture of integrated circuit devices or of specific parts thereof</td>
<td>H01L 21/70</td>
</tr>
<tr>
<td>Assembly of devices consisting of solid state components formed in or on a common substrate; Assembly of integrated circuit devices</td>
<td>H01L21/98</td>
</tr>
<tr>
<td>Apparatus or processes for manufacturing printed circuits</td>
<td>H05K 3/00</td>
</tr>
<tr>
<td>Manufacture of assemblies consisting of preformed electrical components</td>
<td>H05K 13/00</td>
</tr>
</tbody>
</table>

H01L 41/311

Mounting of piezo-electric or electrostrictive parts together with semiconductor elements, or other circuit elements, on a common substrate

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference Description</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in or on a common substrate or of specific parts thereof; Manufacture of integrated circuit devices or of specific parts thereof</td>
<td>H01L 21/70</td>
</tr>
<tr>
<td>Assembly of devices consisting of solid state components formed in or on a common substrate. Assembly of integrated circuit devices</td>
<td>H01L21/98</td>
</tr>
<tr>
<td>Apparatus or processes for manufacturing printed circuits</td>
<td>H05K 3/00</td>
</tr>
<tr>
<td>Manufacture of assemblies consisting of preformed electrical components</td>
<td>H05K 13/00</td>
</tr>
</tbody>
</table>

H01L 41/39

Inorganic materials

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference Description</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic compositions (i.e., for piezo-electric, electrostrictive, or magnetostrictive elements)</td>
<td>H01L 41/187</td>
</tr>
<tr>
<td>Shaped ceramic products characterised by their composition; Ceramic compositions; Processing powders of inorganic compounds preparatory to the manufacturing of ceramic products</td>
<td>C04B 35/00</td>
</tr>
<tr>
<td>Ceramic compositions containing free metal bonded to carbides, diamond, oxides, borides, nitrides, silicides, e.g. cermets, or other metal compounds, e.g. oxynitrides or sulfides, other than as macroscopic reinforcing agents</td>
<td>C22C</td>
</tr>
</tbody>
</table>
**H01L 41/47**

Processes or apparatus specially adapted for the assembly, manufacture or treatment of magnetostrictive devices or of parts thereof

**Definition statement**

*This place covers:*

Processes or apparatus for manufacturing a material, product or device, which exhibits or changes a magnetization when subjected to mechanical stress or which exhibits a mechanical deformation when subjected to a magnetic field.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| For the manufacture or treatment of semiconductor or solid-state devices or of parts thereof in general | H01L 21/00 |

**H01L 43/00**

Devices using galvano-magnetic or similar magnetic effects; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof (devices consisting of a plurality of solid state components formed in or on a common substrate **H01L 27/00**; devices with potential-jump barrier, or surface barrier controllable by variation of a magnetic field **H01L 29/82**)

**Definition statement**

*This place covers:*

Devices wherein an electrical current flow, e.g. amplitude, direction, electronic spin, within a solid state body is directly influenced by an external magnetic field, the related materials, and fabrication of such devices.

Particularly relevant are devices based on:

- Hall effect (generation of a potential difference (Hall voltage) across an electrical conductor, transverse to an electrical current therein and a magnetic field perpendicular to the current);
- Magnetoresistance effects (change of electrical resistance under magnetic field influence), in particular tunnel magnetoresistance or giant magnetoresistance, so-called spin valves.
- This group covers galvano-magnetic devices which are pertinent to several technical fields or which are not limited to a particular application, i.e. galvano-magnetic devices in general. Aspects such as their structure, materials used, fabrication etc. are classified here.

**References**

**Limiting references**

*This place does not cover:*

| Semiconductor devices using spin-polarised carriers, e.g. Spin-FET | H01L 29/66984 |
| Semiconductor devices with at least one potential barrier, e.g. diodes or transistors, controllable by a magnetic field | H01L 29/82 |
Application-oriented references
Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

<table>
<thead>
<tr>
<th>Devices consisting of plural semiconductor or other solid state components on a common substrate, e.g. integrated circuit arrangements, including galvano-magnetic components, e.g. MRAM arrangements</th>
<th>H01L 27/22</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical quantity converters in sensors, e.g. magnetic encoders</td>
<td>G01D 5/142</td>
</tr>
<tr>
<td>Isolation couplers in electrical sensors</td>
<td>G01R 15/20</td>
</tr>
<tr>
<td>Arrangements for measuring electrical power or power factor</td>
<td>G01R 21/08</td>
</tr>
<tr>
<td>Magnetometers- Manufacturing</td>
<td>G01R 33/06, G01R 33/0052</td>
</tr>
<tr>
<td>Magnetic recording heads - using Hall devices- using MR devices</td>
<td>G11B 5/37, G11B 5/39</td>
</tr>
</tbody>
</table>

Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Manufacture or treatment of semiconductor or solid state devices in general</th>
<th>H01L 21/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage or current regulators</td>
<td>G05F 1/635</td>
</tr>
<tr>
<td>Analogue computers</td>
<td>G06G 7/162</td>
</tr>
<tr>
<td>Frequency generators</td>
<td>H03B 15/00</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>H03F 15/00</td>
</tr>
<tr>
<td>Switching circuits - Pulse generators - Electronic switching circuits - Proximity switches- Logic circuits</td>
<td>H03K 3/59, H03K 17/90, H03K 17/9517, H03K 19/18</td>
</tr>
</tbody>
</table>

Special rules of classification
In this group, in the absence of an indication to the contrary, an invention is classified in the last appropriate place. Additional information concerning devices, materials or manufacturing methods is indicated by Indexing Code symbols, e.g. in case the invention concerns a device Indexing Code symbols for details or manufacturing should be allocated.

Synonyms and Keywords

<table>
<thead>
<tr>
<th>AMR</th>
<th>Anisotropic magnetoresistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMR</td>
<td>Colossal magnetoresistance</td>
</tr>
<tr>
<td>EMR</td>
<td>Extraordinary magnetoresistance</td>
</tr>
<tr>
<td>GMR</td>
<td>Giant magnetoresistance</td>
</tr>
<tr>
<td>MR</td>
<td>Magnetoresistance</td>
</tr>
<tr>
<td>MRAM</td>
<td>Magnetoresistive RAM</td>
</tr>
<tr>
<td>MTJ</td>
<td>Magnetic tunnel junctionMR tunnel junction</td>
</tr>
<tr>
<td>Spin-FET</td>
<td>FET using spin-polarised carrier transport</td>
</tr>
</tbody>
</table>
H01L 43/00 (continued)

<table>
<thead>
<tr>
<th>STJ</th>
<th>Spin tunnel junction</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR</td>
<td>Tunnel magnetoresistance</td>
</tr>
<tr>
<td>XMR</td>
<td>Any one of AMR to TMR</td>
</tr>
</tbody>
</table>

H01L 43/02

Details

Definition statement

This place covers:
Special structures of or auxiliary parts associated with the galvano-magnetic devices, e.g. of mechanical or electrical nature, such as mounting or wiring means.

H01L 43/10

Selection of materials

Definition statement

This place covers:
Only materials of the active galvano-magnetic parts of the devices, e.g. pinning, pinned or free magnetic layers, non-magnetic or tunnel barriers of MR devices.

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Magnetic thin film materials | H01F 10/08 |
| Magnetic thin films comprising spin-exchange-coupled multilayers-Manufacturing | H01F 10/32, H01F 41/302 |

H01L 45/00

Solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier, e.g. dielectric triodes; Ovshinsky-effect devices; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof (devices consisting of a plurality of solid state components formed in or on a common substrate H01L 27/00; devices using superconductivity H01L 39/00; piezo-electric devices H01L 41/00; bulk negative resistance effect devices H01L 47/00; {memories G11C 11/34; G11C 13/0002; amplifying circuits H03F 11/00; pulse generation H03K 3/02; electronic switching circuits H03K 17/00; logic circuits H03K 19/00})

Definition statement

This place covers:
Devices wherein the electrical conductivity within a bulk solid state body is directly influenced by an electrical current flowing through or an electrical field applied to the body, the related materials, and fabrication of such devices.

Particularly relevant are devices based on
• Electrically switchable resistance, which in analogy to devices based on magnetoresistance may be called electroresistance devices;
• Electron tunnelling through insulators, e.g. MIM diodes;
• Charge density travelling waves.

The group H01L 45/00 itself covers conductor-insulator-conductor devices, e.g. MIM diodes, having one branch in their current-voltage characteristics only; the insulator (I) may comprise multiple different insulator layers. It extends also to transistor like MIMIM devices.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superconductive devices- MIM type</td>
<td>H01L 39/00, H01L 39/22</td>
</tr>
<tr>
<td>Piezoelectric devices</td>
<td>H01L 41/00</td>
</tr>
<tr>
<td>Bulk negative differential resistance devices, e.g. Gunn diodes</td>
<td>H01L 47/00</td>
</tr>
</tbody>
</table>

Application-oriented references

Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Devices consisting of plural semiconductor or other solid state components on a common substrate, e.g. integrated circuit arrangements, including electroresistance components, e.g. PRAM arrays</td>
<td>H01L 27/24</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active matrix liquid crystal displays</td>
<td>G02F 1/1365</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>H03F 11/00</td>
</tr>
</tbody>
</table>

Special rules of classification

In this group, in the absence of an indication to the contrary, an invention is classified in the last appropriate place. Additional information concerning devices, materials or manufacturing methods is indicated by Indexing Code symbols, e.g. in case the invention concerns a device Indexing Code symbols for details or manufacturing should be allocated.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIM</td>
<td>Metal-insulator-metal</td>
</tr>
</tbody>
</table>
H01L 45/04

{Bistable or multistable switching devices, e.g. for resistance switching non-volatile memory}

Definition statement

This place covers:

Devices having at least two stable branches in their current-voltage characteristics, wherein transition between these branches is obtained at certain switching voltages or currents; the states may be persistent after voltage or current application, e.g. non-volatile or memory type devices (OUM), or non-persistent, e.g. threshold switching devices (OTS).

These devices, showing an electrically switchable resistance, may be called electroresistance devices or RRAM devices. Particularly relevant are devices based on:

- Solid state phase change between amorphous and crystalline states (Ovshinsky effect) or between different crystalline states, e.g. PRAM devices;
- Formation and dissolution of conductive filaments via migration or redistribution of metal cations (CBRAM or PMC devices), anions or crystal vacancies (e.g. OXRAM devices);
- Trapping and detrapping of bulk electronic defects.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Dielectric breakdown anti-fuses - Integrated arrangements thereof - with junction diodes- with transistors</th>
<th>H01L 23/5252, H01L 27/101, H01L 27/1021, H01L 27/112</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical phase change recording</td>
<td>G11B 7/00454, G11B 7/00557, G11B 7/0062</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Devices consisting of plural semiconductor or other solid state components on a common substrate, e.g. integrated circuit arrangements, including resistors or capacitors only | H01L 27/101 |
|________________________________________________________________________________________________|---------------|
| Bistable switching devices with at least one potential barrier, e.g. Hi-Lo semiconductor diodes or transistors | H01L 29/685, H01L 29/8615 |
| Optical phase change recording layers                                                             | G11B 7/243    |
| RRAM digital memories                                                                             | G11C 13/0002  |
| Digital memories with dielectric breakdown anti-fuses                                            | G11C 17/16    |

Special rules of classification

In this group, classes are allocated according to the physical working principle of the device.

Additional classes concerning relevant device details, materials or manufacturing methods should be allocated as well.
Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

RRAM, RERAM, resistive RAM = electrical resistance changing non-volatile devices

**Synonyms and Keywords**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBRAM</td>
<td>Conductive bridging RAM</td>
</tr>
<tr>
<td>CER</td>
<td>Colossal electroresistance</td>
</tr>
<tr>
<td>CRAM</td>
<td>Chalcogenide based RRAM; Carbon based RRAM</td>
</tr>
<tr>
<td>EPIREPVPR</td>
<td>Electrical pulse induced resistance (change)</td>
</tr>
<tr>
<td></td>
<td>Electrical pulse variable resistance</td>
</tr>
<tr>
<td>GST IGST; I-GST NGST; N-GSTOGST; O-GST</td>
<td>GeSbTe, a common chalcogenide PCM GST containing indium</td>
</tr>
<tr>
<td></td>
<td>GST containing nitrogen</td>
</tr>
<tr>
<td></td>
<td>GST containing oxygen</td>
</tr>
<tr>
<td>Memristor</td>
<td>Memory resistor</td>
</tr>
<tr>
<td>OTS</td>
<td>Ovonic threshold switch</td>
</tr>
<tr>
<td>OUM</td>
<td>Ovonic unified memory</td>
</tr>
<tr>
<td>Ovonic</td>
<td>Ovshinsky effect</td>
</tr>
<tr>
<td>OXRAM</td>
<td>RRAM based on oxide switching material</td>
</tr>
<tr>
<td>PCM</td>
<td>Phase change material</td>
</tr>
<tr>
<td>PCMO</td>
<td>PrCaMnO3, a common CER material</td>
</tr>
<tr>
<td>PMC</td>
<td>Programmable metallisation cell; synonym to CBRAM</td>
</tr>
<tr>
<td>PRAMPCRAM</td>
<td>Phase change RAM</td>
</tr>
<tr>
<td>RRAMRERAM</td>
<td>Resistive RAM</td>
</tr>
</tbody>
</table>

*In patent documents the following expressions/words are often used as synonyms:*

CER = EPIR, EVPR

**H01L 47/00**

Bulk negative resistance effect devices, e.g. Gunn-effect devices; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof (devices consisting of a plurality of solid state components formed in or on a common substrate [H01L 27/00](#))

**Definition statement**

*This place covers:*

Devices based on NDR in bulk solid state materials and fabrication of such devices.

The NDR mostly originates from transferred electron effects in semiconductors (electrons are transferred from a conduction band region of high mobility to one of higher energy and lower mobility on the application of an appropriate electric field strength), the Gunn effect being the most prominent one.

Devices of this type are mainly used as primary voltage or current oscillation generating elements in high frequency generators.
References

Application-oriented references

Examples of places where the subject matter of this place is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

| Devices consisting of plural semiconductor or other solid state components on a common substrate, e.g. integrated circuit arrangements, including NDR components | H01L 27/26 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| NDR devices having potential barriers, e.g. resonant tunnel diodes, Esaki diodes | H01L 29/88 |
| Bistable or multistable bulk switching devices | H01L 45/04 |
| Digital memories | G11C 11/39 |
| Frequency generators | H03B 9/12 |
| Amplifiers | H03F 3/10 |
| Pulse generators | H03K 3/357 |
| Electronic switching circuits | H03K 17/70 |

Special rules of classification

In this group, in the absence of an indication to the contrary, an invention is classified in the last appropriate place. Additional information concerning devices or manufacturing methods is indicated by Indexing Code symbols, e.g. in case the invention concerns a device Indexing Code symbols for manufacturing should be allocated.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

| NDR | Negative differential resistance; a negative slope region in the current-voltage characteristics |
| TED | Transferred electron device; Transferred electron diode |

H01L 49/00

Solid state devices not provided for in groups H01L 27/00 - H01L 47/00 and H01L 51/00 and not provided for in any other subclass; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof

Definition statement

This place covers:

Solid state devices which are neither based on semiconductor, thermoelectric, superconductive, piezoelectric/electrostrictive/magnetostrictive, galvano-magnetic, bulk negative differential resistance materials nor bulk switching effects without potential barriers, i.e. using other, potentially unknown, solid state effects for rectifying, amplifying, oscillating or switching, and fabrication of such devices.

Particularly relevant are such devices based on:
• Metal-insulator transition, e.g. Mott effect;
• Quantum effects, e.g. metal single electron devices, Plasmon devices.
• Other thin-film or thick-film devices and fabrication of such devices.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Semiconductor or other solid state devices</th>
<th>H01L 27/00 - H01L 47/00, H01L 51/00 or any other subclass, e.g. B81B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passive two-terminal devices adapted for integrated circuit arrangements</td>
<td>H01L 28/00</td>
</tr>
<tr>
<td>Passive two-terminal devices not adapted for integrated circuit arrangements - Resistors - of thick-film type - Manufacturing thereof - of thin-film type - Manufacturing thereof - Inductors - of printed circuit type - Manufacturing thereof - Capacitors - of thin-film or thick-film type</td>
<td>H01C, H01C 7/003, H01C 17/065, H01C 7/006, H01C 17/075, H01F, H01F 5/003, H01F 17/0006, H01F 41/041, H01G, H01G 4/33</td>
</tr>
</tbody>
</table>

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Semiconductor SETs- Manufacturing</th>
<th>H01L 29/7613, H01L 29/66439, H01L 29/66469</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superconductive transistors- FET type</td>
<td>H01L 39/228, H01L 39/146</td>
</tr>
<tr>
<td>Printed circuits - incorporating printed electric components- Manufacturing</td>
<td>H05K 1/00, H05K 1/16, H05K 3/00</td>
</tr>
</tbody>
</table>

Special rules of classification

In this group, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIT</td>
<td>Metal-insulator transition</td>
</tr>
<tr>
<td>SET</td>
<td>Single electron transistor</td>
</tr>
</tbody>
</table>
H01L 51/00
Solid state devices using organic materials as the active part, or using a combination of organic materials with other materials as the active part; Processes or apparatus specially adapted for the manufacture or treatment of such devices, or of parts thereof (devices consisting of a plurality of components formed in or on a common substrate H01L 27/28; thermoelectric devices using organic material H01L 35/00, H01L 37/00; piezoelectric, electrostrictive or magnetostrictive elements using organic material H01L 41/00)

Definition statement
This place covers:
• Organic materials used as active material in the solid state devices
• Molecular electronic devices
• Devices specially adapted for rectifying, amplifying, oscillating or switching, or capacitors or resistors with at least one potential-jump barrier or surface barrier
• Devices specially adapted for sensing infra-red radiation, light, electro-magnetic radiation of shorter wavelength or corpuscular radiation and adapted for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation using organic materials as the active part, or using a combination of organic materials with other material as the active part;
• Devices specially adapted for light emission, e.g. organic light emitting diodes (OLED) or polymer light emitting devices (PLED)

References

Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Devices consisting of a plurality of components formed in or on a common substrate</th>
<th>H01L 27/00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermoelectric devices using organic material</td>
<td>H01L 35/00, H01L 37/00</td>
</tr>
<tr>
<td>Organic superconductors</td>
<td>H01L 39/00</td>
</tr>
<tr>
<td>Piezoelectric, electrostrictive or magnetostrictive elements using organic material</td>
<td>H01L 41/00</td>
</tr>
<tr>
<td>Devices using galvano-magnetic or similar magnetic effects; Processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof</td>
<td>H01L 43/00</td>
</tr>
<tr>
<td>Solid state devices adapted for rectifying, amplifying, oscillating or switching without a potential-jump barrier or surface barrier</td>
<td>H01L 45/00</td>
</tr>
<tr>
<td>Bulk negative resistance effect devices, e.g. Gunn-effect devices</td>
<td>H01L 47/00</td>
</tr>
<tr>
<td>Typewriters or selective printing mechanisms characterised by the printing or marking process for which they are designed; e.g. ink jet printers</td>
<td>B41J 2/00</td>
</tr>
<tr>
<td>Conductors or conductive bodies characterized by the conductive materials</td>
<td>H01B 1/00</td>
</tr>
<tr>
<td>Insulators or insulating bodies characterised by the insulating materials</td>
<td>H01B 3/00</td>
</tr>
<tr>
<td>Organic capacitors</td>
<td>H01G 4/00</td>
</tr>
<tr>
<td>Semiconductor lasers; e.g. organic semiconductor laser</td>
<td>H01S 5/00</td>
</tr>
</tbody>
</table>
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Invention Description</th>
<th>Indexing Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processes for applying liquids or other fluent materials</td>
<td>B05D 1/00</td>
</tr>
<tr>
<td>Printing processes to produce particular kinds of printed work</td>
<td>B41M 3/00</td>
</tr>
<tr>
<td>Etching, surface-brightening or pickling compositions</td>
<td>C09K 13/00</td>
</tr>
<tr>
<td>Light sources using luminescence; e.g. lamps based on OLEDs</td>
<td>F21K 2/00</td>
</tr>
<tr>
<td>Devices or arrangements for the control of the intensity, colour, phase, polarisation or direction of light arriving from an independent light source, e.g. LCD</td>
<td>G01F 1/00</td>
</tr>
<tr>
<td>Systems using the reflection or re-radiation of radio waves; e.g. RFID tags</td>
<td>Q01S 13/00</td>
</tr>
<tr>
<td>Light guides, e.g. photonic crystals</td>
<td>G02B 6/00</td>
</tr>
<tr>
<td>Digital computers in general; Data processing equipment in general, e.g. molecular computers</td>
<td>G06F 15/00</td>
</tr>
<tr>
<td>Control arrangements or circuits, of interest only in connection with visual indicators other than cathode-ray tubes; e.g. control arrangements for OLED displays</td>
<td>G09G 3/00</td>
</tr>
<tr>
<td>Digital stores characterised by the use of particular electric or magnetic storage elements</td>
<td>G11C 11/00</td>
</tr>
<tr>
<td>Digital stores using elements whose operation depends upon chemical change</td>
<td>G11C 13/02</td>
</tr>
<tr>
<td>Details of electrodes, of magnetic control means, of screens, or of the mounting or spacing thereof, common to two or more basic types of discharge tubes or lamps; e.g. field emission displays</td>
<td>H01J 1/00</td>
</tr>
<tr>
<td>Tagging code for “dye sensitized solar cells”</td>
<td>Y02E 10/541</td>
</tr>
</tbody>
</table>

**Special rules of classification**

The invention is classified using EC classes and Indexing Codes. Additional information is classified using Indexing Codes and Key Words (KW).

If the invention concerns a device, the device is classified in the appropriate sub groups H01L 51/05, H01L 51/42, or H01L 51/50. The materials used in the specific embodiments are then classified using Indexing Codes in the sub groups of H01L 51/0032. Methods used in the specific embodiments are then classified using Indexing Codes in the sub groups of H01L 51/0001.

If the invention concerns a material (as the active part in a device), then the material is classified in the appropriate subgroup H01L 51/0032. Devices of the specific embodiments are then classified using Indexing Codes in the sub groups of H01L 51/05, H01L 51/42, or H01L 51/50. Methods used in the specific embodiments are then classified using Indexing Codes in the sub groups of H01L 51/0001.

If the invention concerns a specially adapted method for producing a device, then the method is classified in H01L 51/0001. Devices of the specific embodiments are then classified using Indexing Codes in the sub groups of H01L 51/05, H01L 51/42, or H01L 51/50. The materials used in the specific embodiments are then classified using Indexing Codes in the sub groups of H01L 51/0032.

Materials are classified only insofar as they are disclosed in a specific embodiment, e.g. a concrete device, or a synthesis method.
Synonyms and Keywords

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTFT</td>
<td>Organic Thin Film Transistor</td>
</tr>
<tr>
<td>OLED</td>
<td>Organic Light Emitting Diode</td>
</tr>
<tr>
<td>PLED</td>
<td>Polymer Light Emitting Diode</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent conductive oxide</td>
</tr>
<tr>
<td>ITO</td>
<td>Indium tin oxide</td>
</tr>
<tr>
<td>FTO</td>
<td>Fluorine doped tin oxide</td>
</tr>
<tr>
<td>LEC</td>
<td>Light emitting electrochemical cell</td>
</tr>
<tr>
<td>RGB</td>
<td>Red Green Blue</td>
</tr>
<tr>
<td>RGBW</td>
<td>Red Green Blue White</td>
</tr>
<tr>
<td>CCM</td>
<td>Colour Changing Material</td>
</tr>
<tr>
<td>HOMO</td>
<td>Highest Occupied Molecular Orbital</td>
</tr>
<tr>
<td>LUMO</td>
<td>Lowest Unoccupied Molecular Orbital</td>
</tr>
</tbody>
</table>

H01L 51/0001

{Processes specially adapted for the manufacture or treatment of devices or of parts thereof (multistep processes H01L 51/0098, H01L 51/05, H01L 51/42, H01L 51/50)}

Definition statement

This place covers:

Processes specially adapted for the formation of organic semiconductor devices, including the formation and patterning of active layers

References

Limiting references

This place does not cover:

Multistep processes for manufacturing devices, see device groups

Informative references

Attention is drawn to the following places, which may be of interest for search:

Etching, surface-brightening or pickling compositions
**H01L 51/0004**

(using printing techniques, e.g. ink-jet printing, screen printing)

**Definition statement**

This place covers:

Printing techniques, such as screen printing, specially adapted for the formation of patterned or non-patterned layers of organic material forming the active part of the device.

**References**

**Limiting references**

This place does not cover:

| Printing of conductive materials for devices covered by H01L 51/00 | H01L 51/0022 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Printing processes to produce particular kinds of printed work | B41M 3/00 |

---

**H01L 51/0005**

(ink-jet printing)

**Definition statement**

This place covers:

Ink jet printing techniques, specially adapted for the formation of patterned or non-patterned layers of organic material forming the active part of the device.

**References**

**Limiting references**

This place does not cover:

| Ink jet printers | B41J 2/005 |

---

**H01L 51/0006**

(Electrolytic deposition using an external electrical current, e.g. in-situ electropolymerisation)

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Polymerisation initiated by direct application of electric current | C08F 2/58 |
H01L 51/0008
(using physical deposition, e.g. sublimation, sputtering)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Coating by vacuum evaporation, by sputtering or by ion implantation of the coating forming material

H01L 51/0009
(using laser ablation)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Vacuum evaporation by wave energy or particle radiation

H01L 51/0011
(selective deposition, e.g. using a mask)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Coating on selected surface areas using masks

H01L 51/0013
(using non liquid printing techniques, e.g. thermal transfer printing from a donor sheet)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Contact thermal transfer or sublimation processes
### H01L 51/0018

{using photolithographic techniques}

#### References

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Photomechanical, e.g. photolithographic, production of textured or patterned surfaces | G03F 7/00 |

### H01L 51/002

{Making n- or p-doped regions}

#### Definition statement

This place covers:

Doping of organic semiconductive material in order to change the electrical properties of the material

#### References

**Limiting references**

This place does not cover:

| Doping of a host material with a light emitting material | H01L 51/5012 |

### H01L 51/0022

{using printing techniques, e.g. ink jet printing}

#### References

**Limiting references**

This place does not cover:

| Ink jet printer | B41J 2/005 |

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Apparatus or processes for manufacturing printed circuits in which conductive material is applied to the insulating support in such a manner as to form the desired conductive pattern by ink-jet printing | H05K 3/125 |
**H01L 51/0024**

{for forming devices by joining two substrates together, e.g. lamination technique}

**Definition statement**

*This place covers:*

Processes where parts of the devices are first formed on each of the two substrates, and the final device is formed by joining the two substrates, e.g.:

![Diagram of process](image.png)

**H01L 51/0027**

{using coherent electromagnetic radiation, e.g. laser annealing}

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Working by laser beam</th>
<th>B23K 26/00</th>
</tr>
</thead>
</table>


H01L 51/0029
{Special provisions for controlling the atmosphere during processing
(H01L 51/0026 takes precedence)}

References
Limiting references
This place does not cover:

<table>
<thead>
<tr>
<th>Thermal treatment of the active layer, e.g. annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 51/0026</td>
</tr>
</tbody>
</table>

H01L 51/003
{using a temporary substrate}

Definition statement
This place covers:
Example:

H01L 51/0032
{Selection of organic semiconducting materials, e.g. organic light sensitive or organic light emitting materials}

Definition statement
This place covers:
organic materials for their electrical or other properties insofar as they are specific for their use in devices covered by the group H01L 51/00.
# References

## Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carbon; Compounds thereof; e.g. Fullerenes</td>
<td>C01B 32/00</td>
</tr>
<tr>
<td>Cyclic hydrocarbons containing rings other than, or in addition to, six-membered aromatic rings</td>
<td>C07C 13/00</td>
</tr>
<tr>
<td>Cyclic hydrocarbons containing only six-membered aromatic rings as cyclic parts</td>
<td>C07C 15/00</td>
</tr>
<tr>
<td>Ketones; Ketenes;</td>
<td>C07C 49/00</td>
</tr>
<tr>
<td>Quinones</td>
<td>C07C 50/00</td>
</tr>
<tr>
<td>Compounds containing amino groups bound to a carbon skeleton</td>
<td>C07C 211/00</td>
</tr>
<tr>
<td>Heterocyclic compounds</td>
<td>C07D</td>
</tr>
<tr>
<td>Macromolecular compounds obtained by reactions forming a carbon-to-carbon link in the main chain of the macromolecule</td>
<td>C08G 61/00</td>
</tr>
<tr>
<td>Macromolecular compounds obtained by reactions forming a linkage containing nitrogen with or without oxygen or carbon in the main chain of the macromolecule</td>
<td>C08G 73/00</td>
</tr>
<tr>
<td>Dyes with anthracene nucleus not condensed with any other ring</td>
<td>C09B 1/00</td>
</tr>
<tr>
<td>Dyes with an anthracene nucleus condensed with one or more carbocyclic rings</td>
<td>C09B 3/00</td>
</tr>
<tr>
<td>Dyes with an anthracene nucleus condensed with one or more heterocyclic rings with or without carbocyclic rings</td>
<td>C09B 5/00</td>
</tr>
<tr>
<td>Acridine dyes</td>
<td>C09B 15/00</td>
</tr>
<tr>
<td>Methine or polymethine dyes, e.g. cyanine dyes</td>
<td>C09B 23/00</td>
</tr>
<tr>
<td>Porphines; Azaporphines</td>
<td>C09B 47/00</td>
</tr>
<tr>
<td>Quinacridones</td>
<td>C09B 48/00</td>
</tr>
<tr>
<td>Dyes of natural origin prepared from natural sources, e.g. vegetable sources</td>
<td>C09B 61/00</td>
</tr>
<tr>
<td>Luminescent, e.g. electroluminescent, chemoluminescent materials</td>
<td>C09K 11/00</td>
</tr>
<tr>
<td>Etching, surface-brightening or pickling compositions</td>
<td>C09K 13/00</td>
</tr>
<tr>
<td>Liquid crystal materials</td>
<td>C09K 19/00</td>
</tr>
</tbody>
</table>

## Special rules of classification

Special rules for classifying chemical compounds

Markush formulae or generic formulae are not classified, only concrete embodiments or examples are classified. Simple lists of known compounds (without application in an example or embodiment) are not classified.

Fullerenes and carbon nanotubes are considered to be organic material. Graphene is considered to be inorganic.

Side-chains of aromatic or aliphatic polymers are classified using the appropriate Indexing Code-codes (sub codes of H01L 51/005, H01L 51/0075, H01L 51/0076, H01L 51/0077, H01L 51/0093).
Aromatic or aliphatic polymers comprising a metal complex in their main chain are classified both in subgroups of H01L 51/0034 and in subgroups of H01L 51/0077.

Compounds comprising silicon are always classified in H01L 51/0094 and, where appropriate, additionally with an Indexing Code of H01L 51/0034, H01L 51/0045, H01L 51/005, H01L 51/0075, H01L 51/0076, H01L 51/0095.

Ligands of metal complexes are not classified in H01L 51/005 and subgroups.

Molecules that comprise hetero aromatic ring systems and condensed (non-hetero) ring systems are classified both in H01L 51/0062 (and subgroups) and H01L 51/0052 (and subgroups).

Cyanine dyes are not classified in H01L 51/0065, H01L 51/0067, H01L 51/0068, H01L 51/0069, H01L 51/0071.

Phthalocyanines

H01L 51/0078 takes precedence over H01L 51/0079, H01L 51/0083, H01L 51/0089, H01L 51/0091, H01L 51/0092.

Transition metal complexes:

H01L 51/0084 takes precedence over H01L 51/0078.

Complexes with more than one metal centre:

H01L 51/009 is given in addition to H01L 51/0078, H01L 51/0079, H01L 51/0083, H01L 51/0084, H01L 51/0089, H01L 51/0091, H01L 51/0092.

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

**Frequently Used Chemical Compounds**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD</td>
<td>N,N,N',N'-Tetrakis(phenyl)benzidine</td>
</tr>
<tr>
<td>TDATA</td>
<td>4,4',4''-Tris(3-alkylphenyl phenylamino)triphenyl-amine</td>
</tr>
<tr>
<td>Compound</td>
<td>Chemical Structure</td>
</tr>
<tr>
<td>-------------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>M-TDATA</td>
<td><img src="image1" alt="M-TDATA Chemical Structure" /></td>
</tr>
<tr>
<td>NaphDATA</td>
<td><img src="image2" alt="NaphDATA Chemical Structure" /></td>
</tr>
<tr>
<td>2-TNATA</td>
<td><img src="image3" alt="2-TNATA Chemical Structure" /></td>
</tr>
<tr>
<td>NPB or α-NPD</td>
<td><img src="image4" alt="NPB or α-NPD Chemical Structure" /></td>
</tr>
<tr>
<td>β-NPD</td>
<td><img src="image5" alt="β-NPD Chemical Structure" /></td>
</tr>
</tbody>
</table>

**Chemical Structures:**

- **M-TDATA:** 4,4',4''-Tris(3-methylphenyl phenylamino)triphenyl-amine
- **NaphDATA:** 4,4',4''-Tris(N-(3-naphthylphenyl)-N-phenyl amino)-triphenyl-amine
- **2-TNATA:** 4,4',4''-Tris(N-(2-naphthyl)-N-phenyl-amino) -triphenylamine
- **NPB or α-NPD:** N,N'-Di(napththalen-2-yl)-N,N'-diphenyl-benzidine; 4,4'-bis[N-(1-naphthyl)-N-phenylamino]biphenyl
- **β-NPD:** ![β-NPD Chemical Structure](image5)
<table>
<thead>
<tr>
<th><strong>TMADN</strong></th>
<th><img src="image" alt="Tetramethyl-9,10-dinaphthyl anthracene" /></th>
</tr>
</thead>
<tbody>
<tr>
<td>TBADN</td>
<td><img src="image" alt="2-(Phenyl)-5-(4-Biphenyl)-1,3,4-oxadiazole" /></td>
</tr>
<tr>
<td><strong>PBD</strong></td>
<td><img src="image" alt="2-(Phenyl)-5-(4-Biphenyl)-1,3,4-oxadiazole" /></td>
</tr>
<tr>
<td>MCP</td>
<td><img src="image" alt="4,4'-di(N-carbazolo) diphenyl" /></td>
</tr>
<tr>
<td>CBP</td>
<td><img src="image" alt="4,4'-di(N-carbazolo) diphenyl" /></td>
</tr>
<tr>
<td><strong>BCP</strong></td>
<td><img src="image" alt="2,9-Dimethyl-4,7-diphenyl-1,10-phenanthroline" /></td>
</tr>
<tr>
<td>BPhen</td>
<td>4,7-Diphenyl-1,10-phenanthroline</td>
</tr>
<tr>
<td>-----------------</td>
<td>----------------------------------</td>
</tr>
</tbody>
</table>
| TPBi            | 2,2',2''(1,3,5-Benzene
triyl)tris-(1-phenyl-1H-benzimida
dole) |
<p>|                 | <img src="image" alt="TPBi Diagram" /> |
| DPVBi           | <img src="image" alt="DPVBi Diagram" /> |
| BCZVBi          | <img src="image" alt="BCZVBi Diagram" /> |
| DPAVBi          | <img src="image" alt="DPAVBi Diagram" /> |
| Spiro-TAD       | <img src="image" alt="Spiro-TAD Diagram" /> |</p>
<table>
<thead>
<tr>
<th>Compound</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCTA</td>
<td>4,4',4&quot;-Tris(N-Carbazoyl) triphenylamin</td>
</tr>
<tr>
<td>TAZ</td>
<td><img src="image" alt="TAZ structure" /></td>
</tr>
<tr>
<td>TCNQ</td>
<td>7,7,8,8-Tetracyano chinodimethan</td>
</tr>
<tr>
<td>DCM2</td>
<td>2-Methyl-6-[2-(2,3,6,7-tetrahydro-1H,5H-benzo[i,j]quinolizin-9-yl)ethenyl]-4H-pyran-4-ylidene porpane dinitrile</td>
</tr>
<tr>
<td>DCJTB</td>
<td><img src="image" alt="DCJTB structure" /></td>
</tr>
<tr>
<td>C545T</td>
<td><img src="image" alt="C545T structure" /></td>
</tr>
<tr>
<td>Pc</td>
<td>Phthalocyanine</td>
</tr>
<tr>
<td>CuPc</td>
<td>Copper Phthalocyanine</td>
</tr>
<tr>
<td>Alq3</td>
<td>Tris-(8-hydroxyquinone) aluminium</td>
</tr>
<tr>
<td>------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>BAlq3</td>
<td><img src="image" alt="BAIq3" /></td>
</tr>
<tr>
<td>Ir(PPy)3</td>
<td><img src="image" alt="Ir(PPy)3" /></td>
</tr>
<tr>
<td>Ir(piq)3</td>
<td><img src="image" alt="Ir(piq)3" /></td>
</tr>
<tr>
<td>FlrPic</td>
<td><img src="image" alt="FlrPic" /></td>
</tr>
<tr>
<td>PtOEP</td>
<td><img src="image" alt="PtOEP" /></td>
</tr>
<tr>
<td>Polymer</td>
<td>Chemical Structure</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------</td>
</tr>
<tr>
<td>PPV</td>
<td><img src="image" alt="Polyphenylenevinylene" /></td>
</tr>
<tr>
<td>P3HT</td>
<td><img src="image" alt="Poly (3-hexyl thiophene)" /></td>
</tr>
<tr>
<td>MDMO-PPV</td>
<td>Poly[2-methoxy-5-(3,7-dimethyloctyloxy)-1,4-phenylenevinylene]</td>
</tr>
<tr>
<td>MEH-PPV</td>
<td>Poly[2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene]</td>
</tr>
<tr>
<td>PCDTBT</td>
<td>Poly[N-9'-heptadecanyl-2,7-carbazole-alt-5,5-(4'-7'-di-2'-1',3'-benzothiadiazole)]</td>
</tr>
<tr>
<td>PCPDTBT</td>
<td>Poly[2,6-(4,4-bis(2-ethylhexyl)-4H-cyclopenta[2,1-b:3,4-b]dithiophene)alt-4,7-(2,1,3-benzo thiadiazole)]</td>
</tr>
<tr>
<td>PVK</td>
<td><img src="image" alt="Polyvinylcarbazol" /></td>
</tr>
<tr>
<td>PFO</td>
<td><img src="image" alt="Polyfluorene" /></td>
</tr>
<tr>
<td>APFO Green 1</td>
<td><img src="image" alt="APFO Green 1" /></td>
</tr>
<tr>
<td>F8BT</td>
<td><img src="image" alt="F8BT" /></td>
</tr>
</tbody>
</table>
PCBM  (6,6)-phenyl-C61-butyric acid methyl ester

H01L 51/0035
{comprising aromatic, heteroaromatic, or aryllic chains, e.g. polyaniline (per se C08G 73/026), polyphenylene (per se C08G 61/10), polyphenylene vinylene (per se C08G 61/02)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Macromolecular compounds containing only carbon atoms in the main chain of the macromolecule, e.g. polyphenylene vinylene | C08G 61/02 |
| Macromolecular compounds containing only aromatic carbon atoms in the main chain of the macromolecule, e.g. polyphenylenes | C08G 61/10 |
| Polyamines | C08G 73/02 |

H01L 51/0036
{Heteroaromatic compounds comprising sulfur or selene, e.g. polythiophene (per se C08G 61/126)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Macromolecular compounds containing atoms other than carbon in the main chain of the macromolecule, derived from five-membered heterocyclic compounds, with a five-membered ring containing one sulfur atom in the ring, e.g. polythiophene | C08G 61/126 |

H01L 51/0038
{Poly-phenylenevinylene and derivatives (per se C08G 61/10)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Macromolecular compounds containing only aromatic carbon atoms in the main chain of the macromolecule, e.g. polyphenylenes | C08G 61/10 |
H01L 51/0041

{Poly acetylene (per se C08G 61/04, C08F 38/02, C08F 138/02, C08F 238/02) or derivatives}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Homopolymers or copolymers of acetylene | C08F 38/02 |
| Homopolymers of acetylene | C08F 138/02 |
| Copolymers of acetylene | C08F 238/02 |
| Macromolecular compounds containing only aliphatic carbon atoms in the main chain of the macromolecule | C08G 61/04 |

H01L 51/0045

{Carbon containing materials, e.g. carbon nanotubes, fullerenes (per se C01B 32/15)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Nanosized carbon materials | C01B 32/15 |

H01L 51/0047

{comprising substituents, e.g. PCBM}

Definition statement

This place covers:

Example:

![Diagram of PCBM, TPA-PCBM, MF-PCBM](image)

US2011132439
H01L 51/005

{Macromolecular systems with low molecular weight, e.g. cyanine dyes, coumarine dyes, tetrathiafulvalene (H01L 51/0045, H01L 51/0077, H01L 51/0093, H01L 51/0094) take precedence}

Definition statement

This place covers:
- Aliphatic compounds
- Styrene and derivatives
- Oligophenylene

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Organic semiconductor materials based on carbon containing materials</td>
<td>H01L 51/0045</td>
</tr>
<tr>
<td>Organic semiconductor materials based on coordination compounds, e.g.</td>
<td>H01L 51/0077</td>
</tr>
<tr>
<td>metal complexes</td>
<td></td>
</tr>
<tr>
<td>Organic semiconductor materials based on biomolecules or bio-macromolecules, e.g. proteins, ATP, chlorophyl, beta-carotene, lipids, enzymes</td>
<td>H01L 51/0093</td>
</tr>
<tr>
<td>Organic semiconductor materials based on silicon-containing organic</td>
<td>H01L 51/0094</td>
</tr>
<tr>
<td>semiconductors</td>
<td></td>
</tr>
<tr>
<td>Organic semiconductor materials based on starburst compounds</td>
<td>H01L 51/0095</td>
</tr>
</tbody>
</table>

H01L 51/0059

{Amine compounds having at least two aryl rest on at least one amine-nitrogen atom, e.g. triphenylamine (per se C07C 211/00)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compounds containing amino groups bound to a carbon skeleton</td>
<td>C07C 211/00</td>
</tr>
</tbody>
</table>

Special rules of classification

Aromatic amine compounds having both a polycondensed non-hetero-aromatic ring system and a heteroaromatic ring system are classified in H01L 51/006 and additionally in H01L 51/0061.

The ring systems are classified using the appropriate Indexing Codes H01L 51/0052, H01L 51/0062.
H01L 51/0062
{aromatic compounds comprising a hetero atom, e.g.: N,P,S}

References
Limiting references
This place does not cover:

| Amine compounds having at least two aryl rest on at least one amine-nitrogen atom | H01L 51/0059 |

Special rules of classification
Compounds having both a non-condensed heteroaromatic ring system and a condensed heteroaromatic ring systems are classified both in H01L 51/0071 and H01L 51/0065 - H01L 51/0069.

H01L 51/0064
{Cyanine Dyes}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Methine or polymethine dyes, e.g. cyanine dyes | C09B 23/00 |

H01L 51/0067
{comprising only nitrogen as heteroatom (H01L 51/0064 takes precedence)}

References
Limiting references
This place does not cover:

| Organic semiconductor materials based on cyanine Dyes | H01L 51/0064 |

H01L 51/0069
{comprising two or more different heteroatoms per ring, e.g. S and N (H01L 51/0064 takes precedence)}

References
Limiting references
This place does not cover:

| Organic semiconductor materials based on cyanine Dyes | H01L 51/0064 |
H01L 51/0075
{Langmuir Blodgett films (per se B05D 1/202)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Langmuir Blodgett films | B05D 1/202 |

H01L 51/0076
{Liquid crystalline materials (per se C09K 19/00)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Liquid crystal materials | C09K 19/00 |

H01L 51/0078
{Phthalocyanine (per se C09B 47/04)}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Phthalocyanine | C09B 47/04 |

H01L 51/009
{Polynuclear complexes, i.e. complexes having two or more metal centers}

Special rules of classification
Metal complexes having more than one metal centre are classified in this group and additionally in groups H01L 51/0079, H01L 51/0089, H01L 51/0091, and H01L 51/0092.

H01L 51/0094
{Silicon-containing organic semiconductors}

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

| Silicon compounds having one or more C-Si linkages | C07F 7/08 |
**H01L 51/0096**

{Substrates}

**Definition statement**

*This place covers:*

Substrates specially adapted for being used in organic semiconductor devices.

**H01L 51/05**

specially adapted for rectifying, amplifying, oscillating or switching, or capacitors or resistors with at least one potential-jump barrier or surface barrier {multistep processes for their manufacture}

**Definition statement**

*This place covers:*

- Organic diodes
- Organic transistors
- Organic thin film transistors

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate including components using organic materials as the active part, or using a combination of organic materials with other materials as the active part | H01L 27/28 |
| Processes specially adapted for forming the device | H01L 51/0001 |
| Organic semiconducting material forming the active part of the device | H01L 51/0032 |
| Organic light emitting transistors | H01L 51/5296 |
**H01L 51/0541**

{Lateral single gate single channel transistors with non inverted structure, i.e. the organic semiconductor layer is formed before the gate electrode}

**Definition statement**

*This place covers:*

Organic thin film transistors with top gate structure:

![Diagram of organic thin film transistor with top gate structure](image-url)
H01L 51/0545

{Lateral single gate single channel transistors with inverted structure, i.e. the organic semiconductor layer is formed after the gate electrode}

Definition statement

*This place covers:*

Organic thin film transistors with bottom gate structure:

![Diagram of organic thin film transistors with bottom gate structure](image)

EP1291932
**H01L 51/0554**

{the transistor having two or more gate electrodes}

**Definition statement**

This place covers:

OTFTS with two gate electrodes:

![Diagram of a transistor with two gate electrodes](image1)

**H01L 51/057**

{having a vertical structure, e.g. vertical carbon nanotube field effect transistors [CNT-FETs]}

**Definition statement**

This place covers:

vertical OTFTs: (S = source; D = drain; G = gate)

![Diagram of a vertical CNT-FET](image2)
H01L 51/0591
{Bi-stable switching devices}

Definition statement

This place covers:

Devices whose resistivity can be switched between two states:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Digital stores using elements whose operation depends upon chemical change</th>
<th>G11C 13/02</th>
</tr>
</thead>
</table>

H01L 51/0595

{molecular electronic devices (molecular computers G06F 15/80; molecular memories G11C 11/00, G11C 13/02)}

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Digital computers in general, e.g. molecular computers</th>
<th>G06F 15/80</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor</td>
<td>G11C 11/00</td>
</tr>
<tr>
<td>Digital stores using elements whose operation depends upon chemical change</td>
<td>G11C 13/02</td>
</tr>
</tbody>
</table>
**H01L 51/10**

Details of devices

**Definition statement**

*This place covers:*

- Electrodes
- Passivation
- Encapsulation

**H01L 51/42**

specially adapted for sensing infra-red radiation, light, electro-magnetic radiation of shorter wavelength or corpuscular radiation and adapted for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation {using organic materials as the active part, or using a combination of organic materials with other material as the active part; Multistep processes for their manufacture}

**Definition statement**

*This place covers:*

- Organic solar cells
- Organic Photodiodes
- Organic light sensitive transistors
- Organic light sensitive resistors

**References**

**Limiting references**

*This place does not cover:*

| Inorganic light sensitive devices | H01L 31/00 |
| Electrolytic light-sensitive devices | H01G 9/20 |

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Devices consisting of a plurality of semiconductor or other solid state components formed in or on a common substrate including components using organic materials as the active part, or using a combination of organic materials with other materials as the active part | H01L 27/30 |
| Processes specially adapted for forming the device | H01L 51/0001 |
| Organic semiconducting material forming the active part of the device | H01L 51/0032 |
**H01L 51/4206**

{Metal-organic semiconductor-metal devices}

**Definition statement**

*This place covers:*

Example:

![Diagram of a metal-organic semiconductor-metal device with labels 8b, 6, 8a, Ag, Me-PTC (Crystal), and 480 nm. The diagram includes a reference to EP1608028.]*
**H01L 51/4213**

{Comprising organic semiconductor-inorganic semiconductor hetero-junctions (H01L 51/4253 takes precedence)}

**Definition statement**

*This place covers:*

Light sensitive devices having a junction between an organic semiconductor and silicon, II-VI semiconductors (e.g. CdSe), III-V semiconductors (GaAs), or chalcogenide semiconductors (CIS, CIGS)

---

**References**

**Limiting references**

*This place does not cover:*

| Light sensitive devices comprising a bulk hetero junction | H01L 51/4253 |
H01L 51/422

{Majority carrier devices using sensitisation of widebandgap semiconductors, e.g. TiO$_2$ (photoelectrochemical devices with a liquid or solid electrolyte \textit{H01G 9/20})}

References

\textit{Limiting references}

\textit{This place does not cover:}

| Electrolytic light sensitive devices based on oxide semiconductors, e.g. dye sensitized solar cells | \textit{H01G 9/2027} |

\textbf{Glossary of terms}

\textit{In this place, the following terms or expressions are used with the meaning indicated:}

widebandgap semiconductors are semiconductors having a bandgap $>$ 2.7 eV.
H01L 51/4226
{the wideband gap semiconductor comprising titanium oxide, e.g. TiO$_2$}

**Definition statement**

*This place covers:*
Solid state dye sensitized solar cells

---

**Figure 1** - Schematic diagram of a solid state dye sensitised solar cell formed with a mesoporous TiO$_2$ n-type semiconductor material.
H01L 51/424

{comprising organic semiconductor-organic semiconductor hetero-junctions (H01L 51/4253 takes precedence)}

Definition statement

This place covers:

Example:

References

Limiting references

This place does not cover:

Bulk hetero-junction devices  H01L 51/4253
H01L 51/4246
{comprising multi-junctions, e.g. double hetero-junctions}

Definition statement

This place covers:

Example:

devices having an exciton blocking layer (composed of BCP):

![Diagram of multi-junction device](image1)

H01L 51/4253
{comprising bulk hetero-junctions, e.g. interpenetrating networks}

Definition statement

This place covers:

Example:

![Diagram of bulk hetero-junction](image2)
H01L 51/4273
{comprising blocking layers, e.g. exciton blocking layers}

Definition statement

This place covers:

Example:

![Graph showing current density vs bias voltage](image)


H01L 51/428
{light sensitive field effect devices}

Special rules of classification

Light sensitive field effect devices are additionally classified in groups H01L 51/4206 - H01L 51/4253. Structural details of the field effect device are classified by Indexing Codes of H01L 51/0508.
**H01L 51/445**

{comprising arrangements for extracting the current from the cell, e.g. metal finger grid systems to reduce the serial resistance of transparent electrodes}

**Definition statement**

*This place covers:*

E.g. metal finger grid electrodes:

---

![Diagram](image1)

**H01L 51/447**

{Light trapping means}

**Definition statement**

*This place covers:*

optical elements that improve the light absorption in the active layer

---

![Diagram](image2)
**H01L 51/448**

{Passivation, containers, encapsulations}

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Passivation, containers, encapsulations for OLEDs | H01L 51/5237 |

**H01L 51/50**

specially adapted for light emission, e.g. organic light emitting diodes [OLED] or polymer light emitting devices [PLED]; (organic semiconductor lasers H01S 5/36; {circuit arrangements for OLED or PLED H05B 33/0896; control arrangements for organic electroluminescent displays G09G 3/3208})

**Definition statement**

This place covers:

Solid state devices specially adapted for light emission using organic materials as the active part e.g. OLED, PLED

The headgroup H01L 51/50 is given if the active part of the OLED contains a layer with a function different from those given in the subgroups thereof. Preferably, a short description of the function of the special layer is given in free text, example:

US2008318084:

![Diagram](image)

Colour stabilizing layer (CSL) between EL and HBL

**References**

**Limiting references**

This place does not cover:

| Inorganic light emitting diodes | H01L 33/00 |
| Control arrangements for organic electroluminescent displays | G09G 3/3208 |
| Organic semiconductor lasers | H01S 5/36 |
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Indexing Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assemblies of OLEDs</td>
<td>H01L 25/048</td>
</tr>
<tr>
<td>Devices consisting of a plurality of organic light emitting devices formed in or on a common substrate, e.g. integrated devices with OLEDs</td>
<td>H01L 27/32</td>
</tr>
<tr>
<td>Single-step processes for the manufacture or treatment of the device or of parts thereof</td>
<td>H01L 51/0001</td>
</tr>
<tr>
<td>Organic semiconducting materials</td>
<td>H01L 51/0032</td>
</tr>
<tr>
<td>Lighting devices for vehicle interior</td>
<td>B60Q 3/00</td>
</tr>
<tr>
<td>Luminescent e.g. electroluminescent materials</td>
<td>C09K 11/00</td>
</tr>
<tr>
<td>Light sources using semiconductor devices as light-generating elements, e.g. using light-emitting diodes [LED] or lasers</td>
<td>F21K 9/00</td>
</tr>
<tr>
<td>Lighting devices intended for fixed installation</td>
<td>F21S 8/00</td>
</tr>
<tr>
<td>Details of lighting devices, of general application</td>
<td>F21V</td>
</tr>
<tr>
<td>Planar light sources using OLEDs</td>
<td>F21Y 2107/60 and F21Y 2115/10</td>
</tr>
<tr>
<td>Illumination devices for LCD</td>
<td>G02F1/13357</td>
</tr>
<tr>
<td>Indicating arrangements making use of semiconductor devices</td>
<td>G09F 9/33</td>
</tr>
<tr>
<td>Illuminated signs</td>
<td>G09F 13/00</td>
</tr>
<tr>
<td>Electroluminescent light sources</td>
<td>H05B 33/00</td>
</tr>
</tbody>
</table>

**Special rules of classification**

Layers characterized by the material are classified in a subgroup of H01L 51/0032 and additionally receive the Indexing Code-code H01L 51/5012-H01L 51/5096, corresponding to the nature of the layer. E.g. a hole-transporting layer characterized by a specific material is classified in H01L 51/0032 and H01L 51/5056.

**Synonyms and Keywords**

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL</td>
<td>Electroluminescent, electroluminescent layer</td>
</tr>
<tr>
<td>OEL</td>
<td>Organic electroluminescent layer</td>
</tr>
<tr>
<td>EIL</td>
<td>Electron injection layer</td>
</tr>
<tr>
<td>HIL</td>
<td>Hole injection layer</td>
</tr>
<tr>
<td>ETL</td>
<td>Electron transporting layer</td>
</tr>
<tr>
<td>HTL</td>
<td>Hole transporting layer</td>
</tr>
<tr>
<td>EBL</td>
<td>Electron blocking layer</td>
</tr>
<tr>
<td>HBL</td>
<td>Hole blocking layer</td>
</tr>
<tr>
<td>LEC</td>
<td>Light emitting electrochemical cells</td>
</tr>
</tbody>
</table>
H01L 51/5004
{characterised by the interrelation between parameters of constituting active layers, e.g. HOMO-LUMO relation}

Definition statement
This place covers:
OLEDs characterized by comparing parameters of constituting active (sub)layers e.g. HOMO, LUMO comparison of adjacent layers

Example:
EP2247163:

References

Limiting references
This place does not cover:

Subject matter relating to a specific layer characterized by parameters independently of adjacent layers. This is classified in the corresponding group covering this layer in addition to the Indexing Code-code H01L 2251/55, e.g. a doped hole transporting layer characterised by a certain thickness is classified in H01L 51/506 in combination with H01L 2251/558

H01L 51/5008
{Intermediate layers comprising a mixture of materials of the adjoining active layers}

Definition statement
This place covers:
Intermediate layers comprising a mixture of materials of the adjoining active layers or structures in which the materials of adjoining layers are completely mixed with concentration gradients to avoid sharp interfaces.
Examples:
EP1220339:

**H01L 51/5012**

{Electroluminescent [EL] layer}

**Definition statement**

This place covers:

In the headgroup (H01L 51/5012) the fluorescent light emitting layers are classified, i.e. only the formation of singlet excitons results in the emission of useful radiation.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Multiple hosts in the emissive layer | H01L 2251/5384 |

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| Electroluminescent layer | The layer from which the light is emitted, this can be a separate EL layer between a HTL and ETL in a structure anode/HTL/EL/ETL/cathode or it can be e.g. a layer having the dual function of electron transporting and electroluminescence in a structure anode/HTL/ETL(EL)/cathode. |

H01L 51/5016

{Triplet emission}

Definition statement

This place covers:
Phosphorescent emitting layer, i.e. whereby light is generated from both triplet and singlet excitons.

Example:
WO2008147154:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Fluorescent light emitting layer | H01L 51/5012 |
| Stack of electroluminescent layers | H01L 51/5036 |

Synonyms and Keywords

In patent documents, the following abbreviations are often used:

| PHOLED | Phosphorescent organic light emitting diode |
**H01L 51/502**

{comprising active inorganic nanostructures, e.g. luminescent quantum dots}

**Definition statement**

*This place covers:*

Emissive layer comprising inorganic nanostructures (in combination with organic materials in the active part).

**Examples:**

US2008007156:

WO03084292:

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>nanoparticles in whatever layer except emissive layer</td>
<td>H01L 2251/5369</td>
</tr>
<tr>
<td>nanooptics e.g. quantum optics or photonic crystals</td>
<td>B82Y 20/00</td>
</tr>
<tr>
<td>Inorganic luminescent materials</td>
<td>C09K 11/08</td>
</tr>
</tbody>
</table>

**Synonyms and Keywords**

In patent documents, the following abbreviations are often used:

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>QD</td>
<td>quantum dot</td>
</tr>
</tbody>
</table>
**H01L 51/5024**

{having a host comprising an emissive dopant and further additive materials, e.g. for improving the dispersability, for improving the stabilisation, for assisting energy transfer}

**Definition statement**

*This place covers:*

Electroluminescent layers comprising at least three different components: a host material, an emissive dopant (fluorescent or phosphorescent) and a further additive material (not responsible for charge transportation or light emission). The additive helps, e.g. to improve the morphology of the layer, to improve the dispersability of the dopant in the host, to improve the stabilisation (lifetime) of the emissive layers.

Example:

US2007087220:

![Diagram](image)

Fig. 3

S1: first excited singlet energy state; T1, T2: first, second excited triplet energy state; S1*, T1* resp. vibronic levels of the S1 and T1 energy states.

Stabilizing material is capable of accepting energy of higher excited energy states of the emitting material (depopulation avoiding degradation)

**H01L 51/5028**

{for assisting energy transfer, e.g. sensitization}

**Definition statement**

*This place covers:*

Electroluminescent layers comprising a host material, an emissive dopant and additive material used for assisting energy (or exciton) transfer between the host material and the emissive dopant. The purpose of the additive is to help increase the light emission from the dopant. The additive is normally not emissive, however some residual light emission might also result from the additive.
Example:

Singlet and triplet excitons in the host material are transferred to the phosphorescent sensitizer or, with a lower probability, are directly transferred to the fluorescent dye. Singlet excitons in the phosphor are transferred to the triplet state (intersystem crossing) from where they can couple with the singlet state of the fluorescent dye.

X: loss mechanisms

Ideally all excitons are transferred to the singlet state of the fluorescent dye.

**Synonyms and Keywords**

*In patent documents, the following abbreviations are often used:*

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISC</td>
<td>intersystem crossing agent</td>
</tr>
</tbody>
</table>

**H01L 51/5032**

{Light emitting electrochemical cells [LEC], i.e. with mobile ions in the active layer}

**Definition statement**

*This place covers:*

Organic electroluminescent devices having mobile ions in the active layer,
Example:

![Diagram](image)

References

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Electroluminescent light sources | H05B 33/00 |

**H01L 51/5036**

{Multi-colour light emission, e.g. colour tuning, polymer blend, stack of electroluminescent layers}

**Definition statement**

This place covers:

Electroluminescent layer containing a stack of emissive sublayers, e.g. R, G, B emissive sublayers, combination of emissive host and emissive dopant, different dopants in the emissive layer, OLED in combination with filter or colour changing media (CCM). Frequently used for white light emission.
Example:

WO2009/36718

1: OLED; 3: Wavelength conversion layer; 4: filter layer

References

Limiting references

This place does not cover:

- Stacked OLEDs for multi-colour emission
- OLED displays using colour filters or colour changing media for generation of RGB sub-pixels
- Integration of OLED and light modulating element e.g. electrochromic element
- Repetitive electroluminescent units between one set of electrodes

Informative references

Attention is drawn to the following places, which may be of interest for search:

- Optical filters in general

H01L 51/504

{Stack of electroluminescent layers}

Definition statement

This place covers:

Electroluminescent layer containing a stack of emissive sublayers for multi-colour light emission
Example:

US2008318084: Stack of emissive sublayers (R,B,G) in contact, for the emission of white light

**H01L 51/5044**

*{with spacer layers between the emissive layers}*

**Definition statement**

*This place covers:*
Electroluminescent layer containing a stack of emissive sublayers with at least one spacer layer between two adjacent emissive sublayers, often between a fluorescent and phosphorescent emissive sublayer

Example:

US2007278937
Stack of fluorescent and phosphorescent emitting layers with spacer in between

EP2503617:

14a: red and green emissive layer comprising a host having hole transportability and red and green phosphorescent dopant

14c: blue emissive layer comprising a host having electron transportability and blue fluorescent dopant

14b: spacer layer consists of hole transport material which prevents energy transfer from the blue emissive layer to the red and green emissive layer

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| combination of fluorescent and phosphorescent emission | H01L 2251/5376 |

H01L 51/5048

{Carrier transporting layer}

Special rules of classification

This group is no longer used for classification of new documents, see sub groups H01L 51/5056 and H01L 51/5072.

H01L 51/5052

{Doped transporting layer}

Special rules of classification

This group is no longer used for classification of new documents, see sub groups H01L 51/506 and H01L 51/5076.
**H01L 51/5056**

*{Hole transporting layer}*  

**Definition statement**  

*This place covers:*  

Organic layer having a function of transporting holes. Normally, this layer is positioned between the anode (or hole injection layer) and the emissive layer.

**References**  

**Limiting references**  

*This place does not cover:*  

| Emissive hole transporting layer | H01L 51/5012 |

**Special rules of classification**  

Hole transporting layers characterized by the material are classified in a subgroup of H01L 51/0032 and additionally receive the Indexing Code-code H01L 51/5056.

**H01L 51/506**

*{comprising a dopant}*  

**Definition statement**  

*This place covers:*  

Doped hole transporting layer. This allows the use of a thicker transporting layer and a larger selection of electrode materials.

**H01L 51/5064**

*{having a multilayered structure}*  

**Definition statement**  

*This place covers:*  

Hole transporting layer comprising a stack of hole transporting sublayers e.g. to overcome an energy barrier.
Example:

US2007262703

stack of hole transporting layers (22DPSF and TCTA)

**H01L 51/5068**

{arranged between the light emitting layer and the cathode}

**Definition statement**

*This place covers:*

A hole transporting layer positioned between the light emitting layer and the cathode for whatever reason

Example:

US2011/56029

A transparent conductive layer 104 is positioned between the emissive portion 102 and the cathode 106 to adjust the optical length \( L \) from the emissive layer to the metal cathode and a hole transporting medium 105 is further positioned between the transparent conductive layer 104 and the cathode 106 to avoid electric erosion
### References

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spacer layer between emissive sublayers</td>
<td>H01L 51/5044</td>
</tr>
<tr>
<td>Charge generation layer between emissive units</td>
<td>H01L 51/5278</td>
</tr>
</tbody>
</table>

### H01L 51/5072

{Electron transporting layer}

**Definition statement**

*This place covers:*

Organic layer having a function of transporting electrons. Normally, this layer is positioned between the emissive layer and the cathode.

**References**

**Limiting references**

*This place does not cover:*

<table>
<thead>
<tr>
<th>Description</th>
<th>CPC Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emissive electron transporting layer</td>
<td>H01L 51/5012</td>
</tr>
</tbody>
</table>

### Special rules of classification

Electron transporting layers characterized by the material are classified in a subgroup of H01L 51/0032 and additionally receive the Indexing Code-code H01L 51/5072.

### H01L 51/5076

{comprising a dopant}

**Definition statement**

*This place covers:*

Doped electron transporting layer, This allows the use of a thicker transporting layer and a larger selection of electrode materials.

### H01L 51/508

{having a multilayered structure}

**Definition statement**

*This place covers:*

Electron transporting layer comprising a stack of electron transporting sublayers e.g. to overcome an energy barrier.
Example:

H01L 51/5084
{arranged between the light emitting layer and the anode}

Definition statement
This place covers:
An electron transport layer positioned between the anode and the light emitting layer for whatever reason

Example:

wo2005/093008

H01L 51/5084
{arranged between the light emitting layer and the anode}

References

Limiting references
This place does not cover:
Spacer layer between emissive sublayers

2: anode, 6: ETL, 3: charge generation layer (CGL), 3a:doped ETL, 3b: doped HTL, 4; light emissive layer

EP1978574

2: anode, 6: ETL, 3: charge generation layer (CGL), 3a:doped ETL, 3b: doped HTL, 4; light emissive layer
H01L 51/5088

{Carrier injection layer}

Definition statement

This place covers:
Layers to improve the carrier injection and/or the adhesion between the electrode and the transporting layer

In the headgroup H01L 51/5088, the hole injection layers and buffer layers formed on the anode are classified.

Examples:
EP1892776:

Buffer layer between anode and HTL

EP2372805:

120a, 120b: hole injecting layers; 130: HTL
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

Anode composed of transparent multilayers  H01L 51/5215

H01L 51/5092

{Electron injection layer}

Definition statement

This place covers:

Organic or inorganic layer not being a metal layer between the cathode and the electron transporting layer to improve the electron injection and/or the adhesion e.g. a LiF-layer.

Examples:

![Diagram](image1)

WO2007130047

271,272: EIL

![Diagram](image2)

US2006115673
121, 123: EIL; 122: cathode; 120: ETL; 118: OEL

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Multilayer opaque cathode | H01L 51/5231 |

H01L 51/5096

{Carrier blocking layer}

Definition statement

This place covers:

Hole blocking layer between EL layer and cathode, electron blocking layer between anode and EL layer, exciton blocking layer

Examples:

US2004048101: Carrier blocking layer between emissive and transporting layer:

US2008315753: Exciton blocking layer:
References

Limiting references

This place does not cover:

| Carrier blocking layer between emissive sublayers for multi-colour light emission | H01L 51/5044 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Transporting layers having a carrier blocking property | H01L 51/5048 |

H01L 51/52

Details of devices

Definition statement

This place covers:

Details of organic light emitting devices such as electrodes, encapsulation, optical aspects.

In the headgroup H01L 51/52 details of the OLED are classified which are not provided for in the subgroups e.g. special substrate features specifically adapted for the OLED, special functioning of the OLED.

Examples:

EP2192636: Special functioning

Special substrate features:
EP1798783: OLED layers formed on substrate provided with recesses

References

Limiting references
This place does not cover:

| Light emitting organic transistors | H01L 51/5296 |

Informative references
Attention is drawn to the following places, which may be of interest for search:

| Substrates specially adapted for organic semiconductor devices | H01L 51/0096 |

Special rules of classification
Details of OLED displays (see H01L 27/32) relating to electrodes, encapsulation, light extraction, contrast improvement are classified in the corresponding H01L 51/52 subgroup in combination with an EC/Indexing Code for the relevant display-group

H01L 51/5203

{Electrodes}

Definition statement
This place covers:
In the headgroup H01L 51/5203 details of the OLED electrodes are classified which are not provided for in the subgroups e.g. special disposition of electrodes (anode and cathode not facing each other, anode and cathode on the same plane); external connection to electrodes for non-matrix type displays.

Examples:
EP2317583:

WO9853644:

References

Limiting references

This place does not cover:

| Wiring lines for AMOLED                  | H01L 27/3276 |
| Wiring lines for PMOLED                | H01L 27/3288 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Light emitting logos                  | H01L 27/3239 |
| OLED lamp                             | H01L 2251/5361 |
Special rules of classification

If an electrode can be anode or cathode, both groups (or corresponding Indexing Code) H01L 51/5206 and H01L 51/5221 are given rather than H01L 51/5203.

In an AMOLED, the pixel electrode is considered to be the anode (unless otherwise stated), and thus aspects of the pixel electrode are classified in H01L 51/5206.

H01L 51/5206
{Anodes, i.e. with high work-function material}

Definition statement

This place covers:
Special treatment of anode, special method for depositing anode, special material used for anode (in headgroup H01L 51/5206 only special transparent or semi-transparent materials used for single-layer anode), special disposition of anode

H01L 51/5209
{characterised by the shape}

Definition statement

This place covers:
Special patterning or shape of the anode (comb like, openings or slits formed in anode)

Example:
US2011204343: Comb-like electrode

1,2: comb-shaped sub-electrodes forming one electrode (anode) of the OLED;
7: organic region
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Segment-type displays | H01L 27/3237 |
| Light emitting logo | H01L 27/3239 |

H01L 51/5212

{combined with auxiliary electrode, e.g. ITO layer combined with metal lines}

Definition statement

This place covers:

Arrangements to lower the resistance of the transparent anode, e.g. combining the ITO-anode with a metal line (auxiliary electrode) in the non-emissive portion

Examples:

US2005116629:

2: anode, 3; auxiliary electrode

US2005139821:

electrode, 204: anode

References

Limiting references

This place does not cover:

Multilayer anode composed of ITO and thin or thick metal layer | H01L 51/5215, H01L 51/5218 |
**H01L 51/5215**

{composed of transparent multilayers}

**Definition statement**

*This place covers:*

Anode composed of transparent or semi-transparent multilayer e.g. ITO and thin metal layer

**Example:**

![Stack diagram](image)

US2011133634

ITO-Ag-ITO stack (a) and Ag-ITO-Ag stack (b) forming semi-transparent anode

**References**

**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

| Glass coated with at least two coatings, at least one coating being a metal | C03C 17/36 |

**H01L 51/5218**

{Reflective anodes, e.g. ITO combined with thick metallic layer}

**Definition statement**

*This place covers:*

Reflective anodes, e.g. thick metallic layer possibly combined with transparent conductive oxide (to improve hole injection).
Examples:

14: reflective anode consisting of an adhesive layer (14A e.g. Cr), a reflective layer (14B e.g. Ag alloy) and a barrier layer (also work-function adjustment layer) (14C e.g., ITO)

12: anode metal layer (reflective e.g. thick layer of Ag, Mo, Cr, W, Ni, V)

**H01L 51/5221**

{Cathodes, i.e. with low work-function material}

**Definition statement**

*This place covers:*

Special method for depositing cathode, special material used for cathode (in headgroup **H01L 51/5221** only special opaque materials used for single-layer cathode), special disposition of cathode.

The cathode is normally made with low work-function material. It can eventually be high work-function material e.g. ITO, e.g. if the electron transporting material is doped.

Example:
3: OEL; 4: cathode encapsulating OEL

**H01L 51/5225**

{characterised by the shape}

**Definition statement**

This place covers:

Special patterning or shape of the cathode e.g. comb like, openings or slits formed in the cathode

Example:

5: cathode, 15; openings made in cathode. In this example, openings are made to allow electrical connection of the anode with a contact structure underneath the cathode.

Sometimes openings are made in the cathode to allow light to pass.

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

| Segment-type displays | H01L 27/3237 |
**Definition statement**

This place covers:

Arrangements to lower the resistance of the cathode, usually in case of transparent cathode

Examples:

WO2004086531:

17a: auxiliary electrode, 17: transparent ITO cathode

US2010181557: cathode having composite transparent structure
41: semi-transparent metal layer; 42: mesh structure to enhance current conducting capabilities

Transparent cathode (5) is electrically connected with electrically conductive layer (8) for uniform light emission

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Transparent cathode | H01L 51/5234 |

**H01L 51/5231**

*composed of opaque multilayers*

**Definition statement**

This place covers:

Cathodes composed of opaque conductive multilayers e.g. Ca/Al bilayer

Example:
34: reflective cathode

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Electron injection layer | H01L 51/5092 |

H01L 51/5234

{Transparent, e.g. including thin metal film}

Definition statement

This place covers:
Transparent and semi-transparent cathodes

Example:
US2010181557:

1. Form a first electrode serving as an anode on a substrate by magnetron sputtering, VTE or CVD
2. Form an organic material layer on the substrate after finishing Step 1 by the VTE, spin coating or spray
3. Form a second electrode serving as a cathode on the substrate after finishing Step 2, in which the second electrode is a composite transparent structure layer realizing light emission at a top portion
4. Form a sealing layer on the substrate after finishing Step 3 by the CVD, spin coating or spray coating
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Cathode combined with auxiliary electrode | H01L 51/5228 |

H01L 51/5237

{Passivation; Containers; Encapsulation, e.g. against humidity}

Definition statement

This place covers:

In the headgroup H01L 51/5237 details of the OLED encapsulation or protection are classified, which are not provided for in the subgroups, e.g. bezel, frame, holding unit

Examples:

US2007200497:

![Diagram showing space allocation in the outer regions of OLED](image)

sealing glass: first encapsulation; lower and upper frame: second encapsulation
100: OLED display panel; 120: encapsulating substrate (first encapsulation); 200: frame; 300: bezel (second encapsulation)

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Processes for the manufacture of encapsulations of solid state devices in general</th>
<th>H01L 21/56</th>
</tr>
</thead>
<tbody>
<tr>
<td>Encapsulation of solid state devices in general</td>
<td>H01L 23/28</td>
</tr>
</tbody>
</table>

Special rules of classification

If layers within the device structure are adapted to avoid moisture penetration, the groups for the corresponding layers are given in combination with the Indexing Code-code H01L 51/5237.
Example:

Special disposition of cathode (H01L 51/5221); Special bank formation (H01L 27/3246); Special interlayer insulating film (H01L 27/3258); Adaptations to avoid moisture penetration (nothing special with the encapsulation itself): H01L 51/5237

H01L 51/524

{Sealing arrangements having a self-supporting structure, e.g. containers}

**Definition statement**

*This place covers:*

Self-supporting structures used in the first encapsulation of the OLED device e.g. cap, glass covering substrate

Examples:
EP0859539:

H01L 51/5243
{the sealing arrangements being made of metallic material}

Definition statement
This place covers:
metallic sealing arrangements, often also used for electrical connection, e.g. metal cap

Examples:
WO2011064700:

EP1835555:

H01L 51/5243
31: IC driver; 38: PCB; 35 sealant; 32: metal cap; 34,37: conductive material

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>External connection to electrodes for matrix-type displays</th>
<th>H01L 27/3276, H01L 27/3288</th>
</tr>
</thead>
<tbody>
<tr>
<td>External connection to electrodes for non matrix-type displays</td>
<td>H01L 51/5203</td>
</tr>
</tbody>
</table>

H01L 51/5246

{characterised by the peripheral sealing arrangements, e.g. adhesives, sealants}

Definition statement

This place covers:

Adhesives, sealants to attach self-supporting structure to the OLED-substrate, e.g. frit.

Adhesives covering the OLED and in contact with the self-supporting structure; Resin fillers

Examples:

US6210815: Adhesives to attach self-supporting structure to OLED substrate

US2011108811:
170: sealant covering OLED: H01L 51/5246

160: protective buffer layer: classified in H01L 51/5253

US2011183575:

3: sealant; 4: resin filler: both are classified in H01L 51/5246

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Protective coatings | H01L 51/5253 |

H01L 51/525

{Vertical spacers, e.g. arranged between the sealing arrangement and the OLED}

Definition statement

This place covers:

Spacers in the sealant or in the gap between the electrode and the cover, normally to keep a certain distance between the OLED and the cover to avoid damage to the OLED.

Examples:

EP0899987:

4: spacer
WO2007008774:

24: spacer

H01L 51/5253

{Protective coatings}

**Definition statement**

*This place covers:*

Protective layers deposited on the OLED device

Examples:

US6198217:
US2011108811:

160: organic protection layer between OLED (120) and sealant (170) preventing penetration of moisture/oxygen from outside; 180: self-supporting structure

Protection layer 160 is classified in H01L 51/5253; Sealant 170 is classified in H01L 51/5246

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Adhesive layers between OLED and self-supporting structure | H01L 51/5246 |

**H01L 51/5256**

{having repetitive multilayer structures}

Definition statement

This place covers:

Repetitive multilayer structures on the (plastic) substrate and/or on the OLED.

Often an inorganic/organic layer stack is used.

Examples:
12a, 12a', 13a, 13a': organic layer; 12b, 12b', 13b, 13b': inorganic layer

110,130, 210,230, 290,310: ceramic barrier layer;
120,140, 220,240, 280,300: polymeric barrier

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

Layered products  B32B

H01L 51/5259
{including getter material or desiccant}

Definition statement
This place covers:
Including materials for absorbing or reacting with moisture or other undesired substances e.g. getters
Examples:

14: getter layer; 16: OLED

US2011012506:

180: getter material around the AMOLED
US2008136316:

34: desiccant; 50: moisture absorption layer

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Solid state devices in general including getters in the encapsulation structure | H01L 23/26 |

H01L 51/5262

{Arrangements for extracting light from the device}

Definition statement

This place covers:

Arrangements for the OLED that provide light extraction through scattering, reflection, refraction, resonant cavity (see sub-groups).

In the headgroup, other arrangements for extracting light are classified e.g. surface Plasmon interaction, removal of insulating layers under OLED to avoid multiple light interactions (e.g. in bottom-emitting AMOLED)

Examples:

US2005161680: Removal of insulating layers under OLED to avoid multiple light interactions.
References

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Nanooptics e.g. quantum optics, photonic crystals          | B82Y 20/00 |
| Surface Plasmon devices                                    | G02B 5/008 |
| Illuminating device for LCD including diffusing, scattering or light controlling member | G02F 1/133606 |

Special rules of classification

If the arrangements for light extraction are provided in the encapsulation, a class (or Indexing Code) is also given in H01L 51/5237 or subgroup

**H01L 51/5265**

{comprising a resonant cavity structure, e.g. Bragg reflector pair}

**Definition statement**

*This place covers:*

OLED structures in which the light emissive layer is sandwiched between a light reflective and a light semi-transparent material and the space there between is used as resonant cavity by adapting the optical path length.

Examples:

US2005161665:

11: semi-reflective electrode; 14: reflective electrode
EP1672962:

The sub-pixels each have an identical emissive layer, the optical distance of the resonant section between the reflectors is adjusted for the generation of RGB sub-pixels. The aspect of the resonant cavity is classified in H01L 51/5265 in combination with H01L 27/3206.

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Description</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multicolour display whereby a single emissive layer is used in combination with resonant cavity structures for the generation of the RGB sub-pixels</td>
<td>H01L 27/3206</td>
</tr>
<tr>
<td>Multicolour display whereby respectively R, G and B emissive layers are used for the sub-pixels; A resonant cavity can be used for colour purification</td>
<td>H01L 27/3211</td>
</tr>
</tbody>
</table>

**Special rules of classification**

If a multicolour display makes use of cavity structures, H01L 51/5265 is given in combination with an EC/Indexing Code for the relevant display group (H01L 27/3206 if an identical emissive layer is used for the sub-pixels, H01L 27/3211 if e.g. red, green and blue emissive layers are used for the sub-pixels, H01L 27/322 if a filter layer is further used for light purification)

**Glossary of terms**

In this place, the following terms or expressions are used with the meaning indicated:

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBR</td>
<td>Distributed Bragg Reflector</td>
</tr>
<tr>
<td>RC</td>
<td>Resonant Cavity</td>
</tr>
</tbody>
</table>
**H01L 51/5268**

**{Scattering means}**

**Definition statement**

This place covers:

Scattering means to scatter the light from the OLED in random directions e.g. by roughening the light extraction surface, by providing particles on the light extraction surface. A light scattering layer can be added to the OLED structure.

Examples:

WO2007008774:

22: scattering particles on the surface of the transparent electrode (18)

**References**

**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Surface treatment of glass by etching | C03C 15/00 |
| Diffusing elements                   | G02B 5/02  |
| Scattering dots in light guides      | G02B 6/004 |
| Illuminating device for LCD including diffusing, scattering or light controlling member | G02F 1/133606 |

**H01L 51/5271**

**{Reflective means}**

**Definition statement**

This place covers:

OLED with reflective means to change the path of the light

Examples:
170: reflective means consisting of metal material having low resistivity and reflecting light. They function as auxiliary electrodes at the same time.

US20030197466:

Light emitted from the organic compound layer 20 is reflected at the slope of the layers 18c and 18d of the first electrode to increase the total amount of light taken out in the direction indicated by the arrow (both classes H01L 51/5271 and H01L 51/5218 are given).

References

Limiting references

This place does not cover:

| Reflective anode having normal (flat) shape     | H01L 51/5218 |
| Reflective cathode having normal (flat) shape  | H01L 51/5221, H01L 51/5231 |

Informative references

Attention is drawn to the following places, which may be of interest for search:

| Mirrors in general                          | G02B 5/08 |
| Illuminating devices for LCD including specially adapted reflector | G02F 1/133605 |
H01L 51/5275
{Refractive means, e.g. lens}

Definition statement
This place covers:
Diffraction gratings, photonic crystals, prisms, birefringent materials, lenses integrated with the OLED or the package.

Example:
GB2464111:

![Diagram of a device showing a diffraction grating, microlens array, and encapsulant film.]

16: diffraction grating; 18: microlens array; 14: encapsulant film

References
Informative references
Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Topic</th>
<th>CPC class</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arrangements for contrast improvement</td>
<td>H01L 51/5012</td>
</tr>
<tr>
<td>Producing optical elements</td>
<td>B29D 11/00</td>
</tr>
<tr>
<td>Nanooptics e.g. quantum optics, photonic crystals</td>
<td>B82Y 20/00</td>
</tr>
<tr>
<td>Refractors for light sources</td>
<td>F21V 5/00</td>
</tr>
<tr>
<td>Lenses in general</td>
<td>G02B 3/00</td>
</tr>
<tr>
<td>Prism</td>
<td>G02B 5/04</td>
</tr>
<tr>
<td>Diffraction gratings in general</td>
<td>G02B 5/18</td>
</tr>
<tr>
<td>Photonic crystals in general</td>
<td>G02B 6/1225</td>
</tr>
</tbody>
</table>

H01L 51/5278
{comprising a repetitive electroluminescent unit between one set of electrodes}

Definition statement
This place covers:
Stack of OLED units characterized by the charge generation layer between the units; stack of OLED units emitting the same colour to improve the efficiency of the device (tandem OLED device)
Example:

US2005173700:

![Diagram of OLED structure]

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Assembly of OLEDs</th>
<th>H01L 25/048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multicolour OLED stack</td>
<td>H01L 27/3209</td>
</tr>
<tr>
<td>Stack of electroluminescent layers in contact e.g. for white light emission</td>
<td>H01L 51/5036</td>
</tr>
</tbody>
</table>

Special rules of classification

The connecting structure is classified in H01L 51/5278 also for multicolour stacked OLED devices. Then H01L 51/5278 is given in combination with H01L 27/3209 (or corresponding Indexing Code).

Glossary of terms

In this place, the following terms or expressions are used with the meaning indicated:

| CGL                  | Charge generation layer |

H01L 51/5281

{Arrangements for contrast improvement, e.g. preventing reflection of ambient light}

Definition statement

This place covers:

Arrangements for improving the contrast of the OLED, e.g. polarizer on top of OLED to reduce reflection of ambient light; textured structure to diffuse external light

Examples:
US2004051445:

24: OLED; 500: polarization separator; 600: polarizer plate; 700: phase plate

US2010171106:

650: rough capping layer to disperse reflected ambient light

References

Limiting references

This place does not cover:

Arrangements for polarized light emission forming part of the OLED device itself
**Informative references**

Attention is drawn to the following places, which may be of interest for search:

| Polarising elements in general | G02B 5/30 |

**H01L 51/5284**

{comprising a light absorbing layer, e.g. black layer}

**Definition statement**

This place covers:

Absorbing layers internal or external to the OLED to improve contrast.

Examples:

EP2187463:

BM: black matrix between colour filters (17R, 17G, 17B) to improve contrast
US2010148192:

195: light absorbing layer pattern to suppress external light reflection
190: pixel defining layer having black base colour (also classified in H01L 27/3246)

H01L 51/5287

{OLED having a fiber structure}

Definition statement

This place covers:
OLED structure whereby the constituting layers are concentric. The OLED fibres can be woven.

Example:
EP1180805:

References

Informative references

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D03D 15/00</td>
<td>Woven fabrics characterised by the material or construction of the yarn or other warp or weft elements used</td>
</tr>
</tbody>
</table>

H01L 51/529

{Arrangements for heating or cooling}

Definition statement

This place covers:

Arrangements for heating or cooling, mainly arrangements to improve heat dissipation. The arrangements can be incorporated into the package.

References

Limiting references

This place does not cover:

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01L 51/0026</td>
<td>Thermal treatment of active layer</td>
</tr>
</tbody>
</table>
H01L 51/5293
{Arrangements for polarized light emission (H01L 51/5281 takes precedence)}

Definition statement
This place covers:
Arrangements internal to the OLED for polarized light emission e.g. by aligning the emitting layers of the OLED, rubbing

Example:

References

Limiting references
This place does not cover:
Polarisers external to the OLED to improve contrast (avoid external reflection)  

Informative references
Attention is drawn to the following places, which may be of interest for search:
Illumination devices for LCD providing polarised light
**H01L 51/5296**

*{Light emitting organic transistors}*

**Definition statement**

*This place covers:*

Organic devices combining transistor function and light emitting function

**Example:**

WO2011110664:

![Diagram of an organic transistor](image)

**References**

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Organic transistors</th>
<th>H01L 51/0504</th>
</tr>
</thead>
</table>

**H01L 51/56**

*Processes or apparatus specially adapted for the manufacture or treatment of such devices or of parts thereof*

**Definition statement**

*This place covers:*

Multistep processes or apparatus specially adapted for the manufacturing of an OLED or OLED display (e.g. to reduce the number of masks in the manufacturing of AMOLED).

**References**

*Limiting references*

This place does not cover:

<table>
<thead>
<tr>
<th>Single step processes for the manufacturing of (part of) the OLED device</th>
<th>H01L 51/0001</th>
</tr>
</thead>
<tbody>
<tr>
<td>e.g. ink jet printing</td>
<td></td>
</tr>
</tbody>
</table>

*Informative references*

Attention is drawn to the following places, which may be of interest for search:

<table>
<thead>
<tr>
<th>Coating by vacuum evaporation, sputtering or by ion implantation of the coating forming material</th>
<th>C23C 14/00</th>
</tr>
</thead>
</table>
Special rules of classification

The general method of making part of an OLED device (e.g. HTL, EL layer, encapsulation, electrodes) is classified together with this device part.

If a special single step process is used in the manufacturing of a specific part of the OLED device, a subgroup in H01L 51/0001 is given in combination with the corresponding Indexing Code-code for that part of the OLED device (e.g. H01L 51/5048).

A single step process in the manufacturing of a display device is classified in a subgroup of H01L 51/0001 in combination with the corresponding EC/Indexing Code for the display device e.g. inkjet printing for RGB sub-pixel formation is classified in H01L 51/0005 and H01L 27/3211.